

# 

- -1 -> 1 --
- R A T, 120, 140, 150, 200, 250, 300
- JEDEC A P
  - . 32 , , H , C , , 0.600" DIP (P 300)
  - . 32 , H , C , , 0.400" SOJ (P 101)
- C,,I,M,,T R
- MIL-STD-883 C , D , A ,
- W, E 10,000 C
- , 25 C, 10 Y D R
- L P CMOSO

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, I		С	Ţ				
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TTL	С	1	I		0		

This product is subject to change without notice.

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NC	4	22	Maa
A16	1	32 31	Vcc WE#
A18 A15	3	30	NC
A15 A12	4	29	A14
A12 A7	5	29	A14 A13
A6	6	20	A13 A8
A0 A5	7	26	A0 A9
A3 A4	8	20	A9 A11
A4 A3	9	23	OE#
A3 A2	10	23	A10
A1	11	22	CS#
A0	12	21	I/07
1/00	13	20	I/O6
I/O1	14	19	I/O5
I/O2 [	15	18	I/O4
Vss [	16	17	] I/O3
	1		1

### 

	,
A0-16	Address Inputs
I/O0-7	Data Input/Output
CS#	Chip Selects
OE#	Output Enable
WE#	Write Enable
Vcc	+5.0v Power
Vss	Ground

### 2004

### R . 5 2004 R . 5

# White Electronic Designs

-0.6 to + 6.25

-0.6 to +13.5

V

V

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Pa a	β⊆́b	,	U.,
Operating Temperature	TA	-55 to +125	°C
Storage Temperature	Tstg	-65 to +150	°C

Vg

NOTE:

Signal Voltage Relative to GND

Voltage on OE# and A9

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MALLI AM	- (			
Pa a	j≩ b	M.	Ma	U,
Supply Voltage	Vcc	4.5	5.5	V
Input High Voltage	Vih	2.0	Vcc + 0.3	V
Input Low Voltage	VIL	-0.5	+0.8	V
Operating Temp. (Mil.)	TA	-55	+125	°C
Operating Temp. (Ind.)	TA	-40	+85	°C

	1, , , ,							
CS#	OE#	WE#	Μ.	Da a I/O				
Н	Х	Х	Standby	High Z				
L	L	Н	Read	Data Out				
L	Н	L	Write	Data In				
Х	Н	Х	Out Disable	High Z/Data Out				
Х	Х	Н	Write					
Х	L	Х	Inhibit					

TA=+25°C

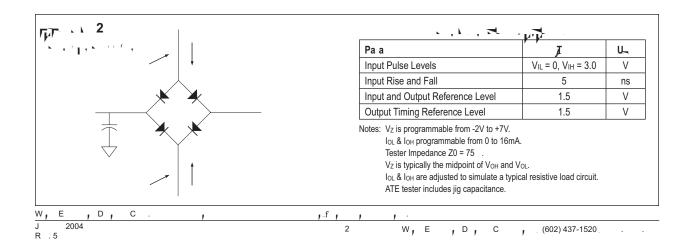
Pa a	j≩ b	C	Ма	U,
Input Capacitance	CIN	V <sub>IN</sub> = 0 V, f = 1MHz	20	pF
Output Capacitance	Соит	V <sub>I/O</sub> = 0 V, f = 1MHz	20	pF

This parameter is guaranteed by design but not tested.

 $V_{CC} = 5.0V. V_{SS} = 0V. -55^{\circ}C = T_{A} + 125^{\circ}C$ 

Pa a	j≨ b	C	H.	Ма	U,
Input Leakage Current	lu	$V_{CC} = 5.5$ , $V_{IN} = GND$ to $V_{CC}$		10	ĻА
Output Leakage Current	ILO	CS# = VIH, OE# = VIH, VOUT = GND to Vcc		10	ĻА
Operating Supply Current	lcc	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		80	mA
Standby Current	Isb	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		0.625	mA
Output Low Voltage	Vol	IoL = 2.1mA, Vcc = 4.5V		0.45	V
Output High Voltage	Vон	I <sub>OH</sub> = -400µA, V <sub>CC</sub> = 4.5V	2.4		V

NOTE: DC test conditions: VIH = Vcc -0.3V, VIL = 0.3V

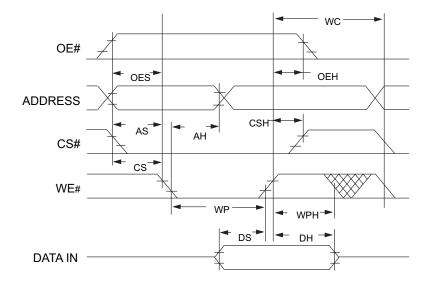


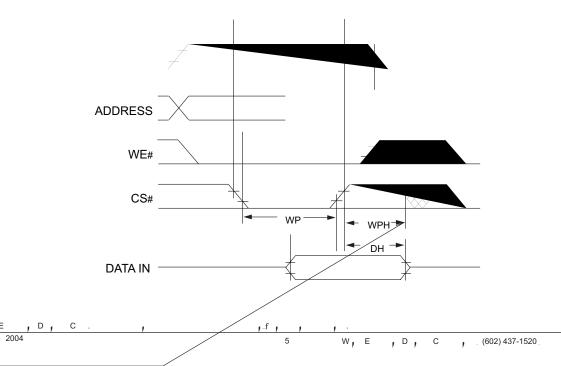
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4

# WHITE ELECTRONIC DESIGNS





W, E J R.5

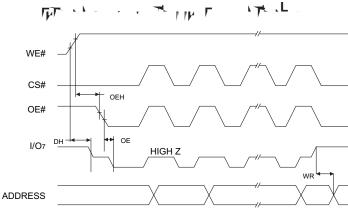
Е

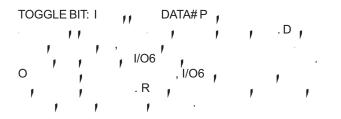
# WHITE ELECTRONIC DESIGNS \_



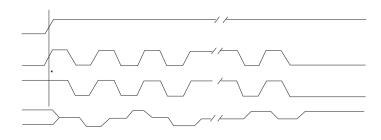
		Г •		۰.	N N 16 11 1	
	Vcc = 5.0V.	$V_{SS} = 0V.$	-55°C	TA	+125°C	

Pa a	ş b	M.	Ма	U,
Data Hold Time	tdh	10		ns
OE# Hold Time	toeh	10		ns
OE# To Output Valid	toe		55	ns
Write Recovery Time	twr	0		ns





7.	<b>FF</b> 11	<u>к к</u> . ч	μ <sup>* -</sup> (1)	
Ş⊑ b	Pa a	M.	Ма	U.,
tDH	Data Hold Time	10		ns
tOEH	OE Hold Time	10		ns
tOE	OE to Output Delay			ns
tOEHP	OE High Pulse	150		ns
tWR	Write Recovery Time	0		ns



#### NOTE:

- 1. Toggling either OE# or CS# or both OE# and CS# will operate toggle bit.
- 2. Beginning and ending state of I/O6 will vary

С

3. Any address location may be used but the address should not vary.

6

1-f 1

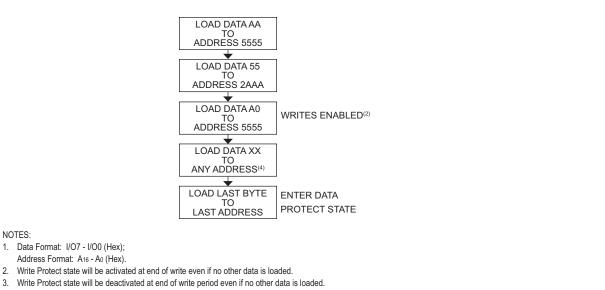


### L' L' L' L' L' L' 1

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	, , ,	.т',	,	, ,
	1 1		1	
Т	,	1		1,1-f

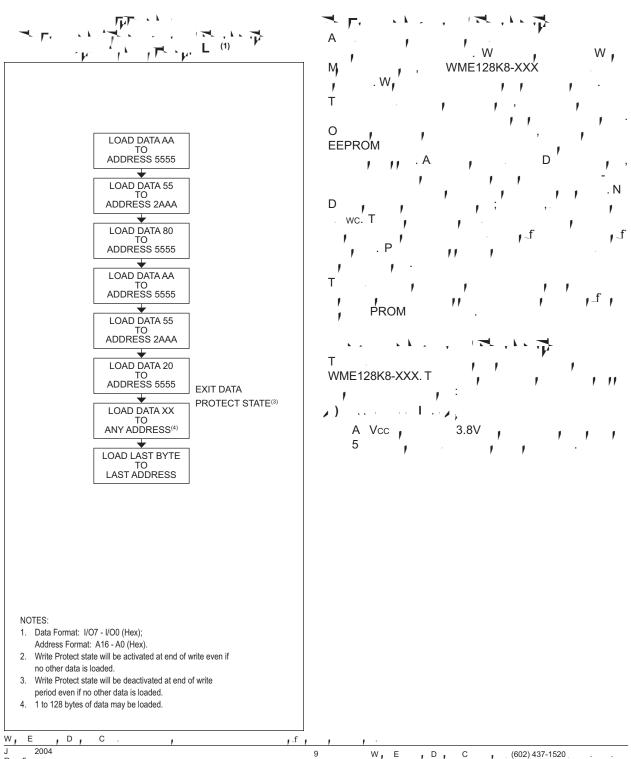
## WHITE ELECTRONIC DESIGNS \_\_\_\_\_ WME128K8-XXX

### $\overline{\mu}\overline{\mu} \rightarrow \overline{\mu} = \overline{\overline{\mu}} + \overline{\mu} +$



4. 1 to 128 bytes of data to be loaded.

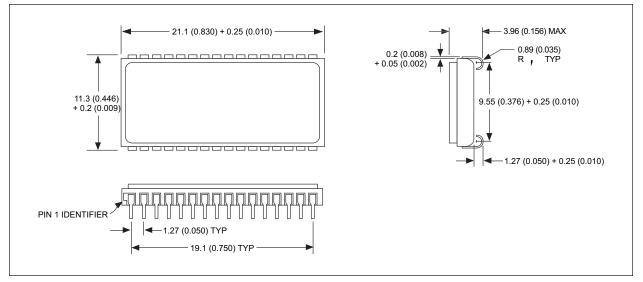
### White Electronic Designs \_\_\_\_\_



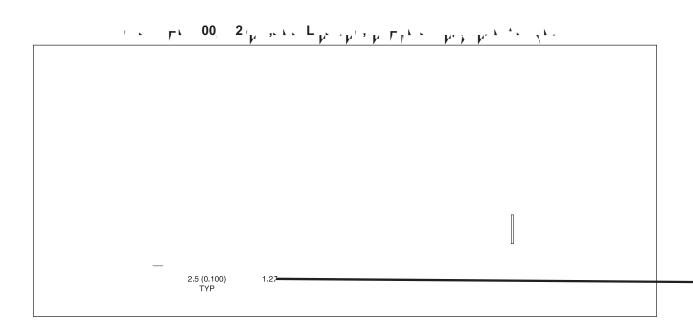
R.5

WHITE ELECTRONIC DESIGNS

 $F_{1}$  101  $2_{1}$   $F_{1}$   $L_{\gamma}$ 



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



## • White Electronic Designs

 $L \cdot 12 - -$  B = G A = S , M = ML-STD-883 C , C = C , 0 C +70 C , C = 32 P C' , DIP (P - 300) DE = 32 L CSOJ (P - 101)  $\dots \dots + L \cdot (1)$   $\dots + L \cdot (1)$ 

. X .	_= k ( k		_ (XX,	( . <b>.</b>	- <b>\</b>	L, .
128K	8 EEPROM M	, ,	300	32 , DIP (	C)	5962-96796 01HYX
128K	8 EEPROM M	11	250	32 , DIP (	C)	5962-96796 02HYX
128K	8 EEPROM M	, ,	200	32 , DIP (	C)	5962-96796 03HYX
128K	8 EEPROM M	11	150	32 , DIP (	C)	5962-96796 04HYX
128K	8 EEPROM M	, ,	140	32 , DIP (	C)	5962-96796 05HYX
128K	8 EEPROM M	11	120	32 , DIP (	C)	5962-96796 06HYX
128K	8 EEPROM M	, ,	300	32 SOJ	I (DE)	5962-96796 01HXX
128K	8 EEPROM M	11	250	32 SOJ	I (DE)	5962-96796 02HXX
128K	8 EEPROM M	, ,	200	32 SOJ	I (DE)	5962-96796 03HXX
128K	8 EEPROM M	11	150	32 SOJ	I (DE)	5962-96796 04HXX
128K	8 EEPROM M	, ,	140	32 SOJ	I (DE)	5962-96796 05HXX
128K	8 EEPROM M	11	120	32 SOJ	I (DE)	5962-96796 06HXX

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