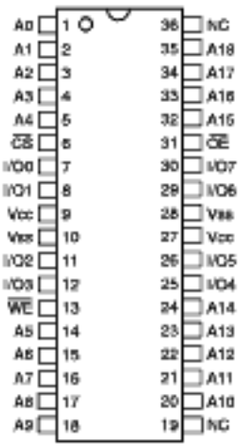
512Kx8 SRAM

*PRELIMINARY **

PIN CONFIGURATION
TOP VIEW



PIN DESCRIPTION

A_{0-18}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground
NC	No Connect

PLASTIC PLUS™ FEATURES

- Access Times of 15, 20, 25ns
- Standard Commercial Off-The-Shelf (COTS) Memory Devices for Extended Temperature Range
- JEDEC Standard 36 pin Plastic SOJ Package
- Electrical and Speed Characteristics for:
  - Military Temperature (-55°C to +125°C)
  - Industrial Temperature (-40°C to +85°C)
- Burn-in and Temperature Cycling Available
- Organized as 512K x 8
- Center Power/Ground Pins (Revolutionary)
- 5 Volt Power Supply
- Low Power ("L") Version Available
- Battery Back-Up Operation
- Reliability Test Data Available:
  - High Temperature Operating Life
  - High Temperature Storage
  - Pressure Cooker Test
  - Wet High Temperature Operating Life
  - Thermal Shock
  - Temperature Cycling

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

PLASTIC PLUS SRAM

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature (Mil.)	T_A	-55	+125	°C
Operating Temperature (Ind.)	T_A	-40	+85	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to Vss	V_G	-0.5	Vcc + 0.5	V
Supply Voltage	V_{CC}	-0.5	7.0	V

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Vcc Current
H	X	X	Power Down	High-Z	I_{SB}
L	H	H	Out Disable	High-Z	Icc
L	H	L	Read	D_{OUT}	Icc
L	L	X	Write	D_{IN}	Icc

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	Vcc + 0.5	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temperature (Mil.)	T_A	-55	+125	°C
Operating Temperature (Ind.)	T_A	-40	+85	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	8	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	Vcc = 5.5, V_{IN} = Vss to Vcc		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = Vss to Vcc		10	µA
Operating Supply Current	Icc	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		180	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		15	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA, Vcc = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, Vcc = 4.5	2.4		V

NOTE: DC test conditions: V_{IL} = 0.3V, V_{IH} = Vcc -0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Supply Voltage	V_{DR}	$\overline{CS}$ ≥ Vcc -0.2V	2.0		5.5	V
Data Retention Current	I_{CCDR1}	Vcc = 3V		0.5	8	mA
Low Power Data Retention (L)	I_{CCDR1}	Vcc = 3V		300	800	µA

AC CHARACTERISTICS

(VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Parameter Read Cycle	Symbol	-15*		-20		-25		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		20		25		ns
Address Access Time	t_{AA}		15		20		25	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns
Chip Select Access Time	t_{ACS}		15		20		25	ns
Output Enable to Output Valid	t_{OE}		8		10		12	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	3		3		3		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		7		8		10	ns
Output Disable to Output in High Z	t_{OHZ}[1]		7		8		10	ns

*15ns not available in the lower power option.

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS

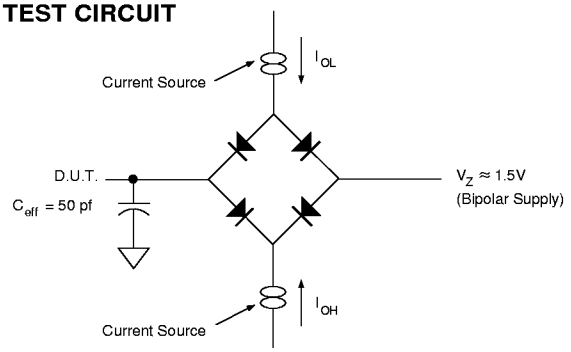
(VCC = 5.0V, TA = -55°C to +125°C)

Parameter Write Cycle	Symbol	-15*		-20		-25		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		20		25		ns
Chip Select to End of Write	t_{CW}	12		13		15		ns
Address Valid to End of Write	t_{AW}	12		13		15		ns
Data Valid to End of Write	t_{DW}	8		9		10		ns
Write Pulse Width	t_{WP}	12		13		15		ns
Address Setup Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		ns
Output Active from End of Write	t_{OW}[1]	0		0		0		ns
Write Enable to Output in High Z	t_{WHZ}[1]		8		8		10	ns
Data Hold Time	t_{DH}	0		0		0		ns

*15ns not available in the lower power option.

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT



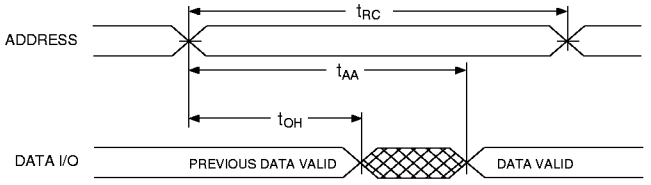
AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

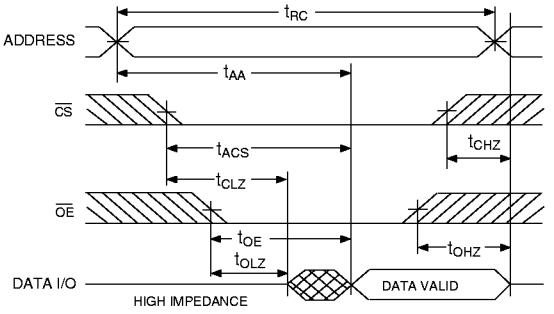
NOTES:

V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

TIMING WAVEFORM - READ CYCLE

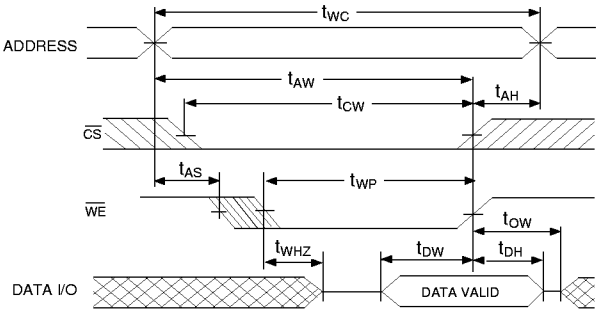


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



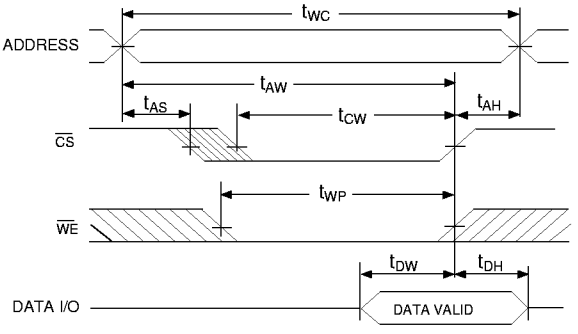
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

WRITE CYCLE - $\overline{WE}$ CONTROLLED



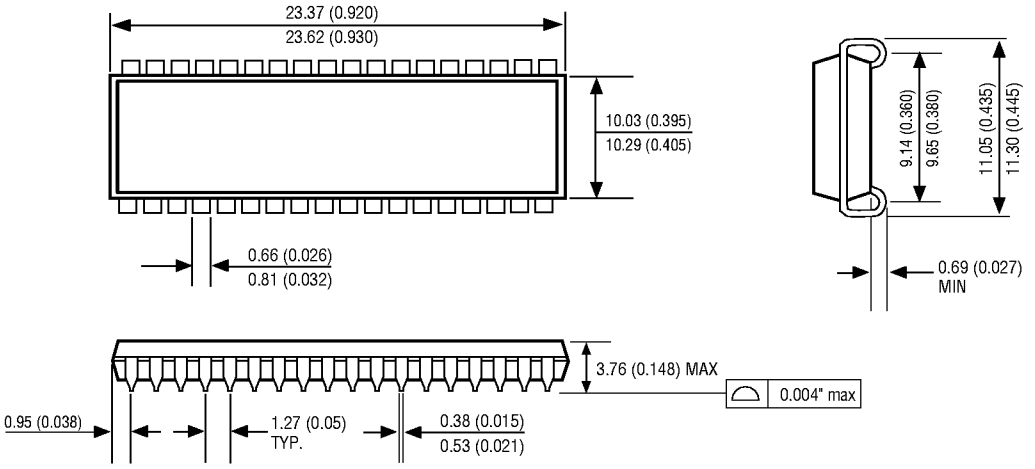
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

PACKAGE DIMENSION



DIMENSIONS IN MILLIMETERS AND (INCHES)

ORDERING INFORMATION

W P S 512K 8 X X - XXX RJ X X

SPECIAL PROCESS:
Blank = CMOS
B = Bi CMOS

DEVICE GRADE:
M = Military Temperature -55°C to +125°C
I = Industrial Temperature -40°C to +85°C

PACKAGE:
RJ = Revolutionary SOJ

ACCESS TIME (ns)

IMPROVEMENT MARK
B = Burn-in
T = Temperature Cycling
C = Burn-in and Temperature Cycle

Blank = Standard Power
L = Low Power

ORGANIZATION, 512K x 8

SRAM

PLASTIC PLUS™

WHITE MICROELECTRONICS