128Kx16 SRAM/EEPROM MODULE

*PRELIMINARY**

FEATURES

- Access Times of 35ns (SRAM) and 150ns (EEPROM)
- Access Times of 45ns (SRAM) and 120ns (EEPROM)
- Access Times of 70ns (SRAM) and 300ns (EEPROM)
- Packaging
  - 66 pin, PGA Type, 1.075" square HIP, Hermetic Ceramic HIP (H1) (Package 400)
  - 68 lead, Hermetic CQFP (G2T), 22mm (0.880") square (Package 509). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 2)
- 128Kx16 SRAM
- 128Kx16 EEPROM
- Organized as 128Kx16 of SRAM and 128Kx16 of EEPROM Memory with separate Data Buses
- Both blocks of memory are User Configurable as 256Kx8
- Low Power CMOS
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight - 13 grams typical

EEPROM MEMORY FEATURES

- Write Endurance 10,000 Cycles
- Data Retention at 25°C, 10 Years
- Low Power CMOS Operation
- Automatic Page Write Operation
- Page Write Cycle Time 10ms Max.
- Data Polling for End of Write Detection
- Hardware and Software Data Protection
- TTL Compatible Inputs and Outputs

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

FIG.1 PIN CONFIGURATION FOR WSE128K16-XH1X

TOP VIEW

1	12	23	34	45	56
SD8	$\overline{SWE_2}$	SD15	ED8	VCC	ED15
SD9	$\overline{SCS_2}$	SD14	ED9	$\overline{ECS_2}$	ED14
SD10	GND	SD13	ED10	$\overline{EWE_2}$	ED13
A13	SD11	SD12	A6	ED11	ED12
A14	A10	$\overline{OE}$	A7	A3	A0
A15	A11	NC	NC	A4	A1
A16	A12	$\overline{SWE_1}$	A8	A5	A2
NC	VCC	SD7	A9	$\overline{EWE_1}$	ED7
SD0	$\overline{SCS_1}$	SD6	ED0	$\overline{ECS_1}$	ED6
SD1	NC	SD5	ED1	GND	ED5
SD2	SD3	SD4	ED2	ED3	ED4
11	22	33	44	55	66

PIN DESCRIPTION

ED_{0-15}	EEPROM Data Inputs/Outputs
SD_{0-15}	SRAM Data Inputs/Outputs
A_{0-16}	Address Inputs
$\overline{SWE}_{1-2}$	SRAM Write Enable
$\overline{SCS}_{1-2}$	SRAM Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground
NC	Not Connected
$\overline{EWE}_{1-2}$	EEPROM Write Enable
$\overline{ECS}_{1-2}$	EEPROM Chip Select

BLOCK DIAGRAM

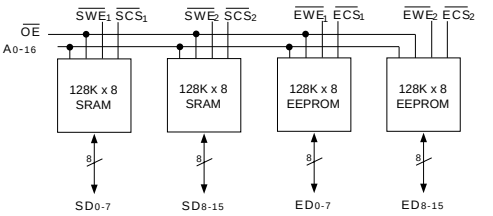
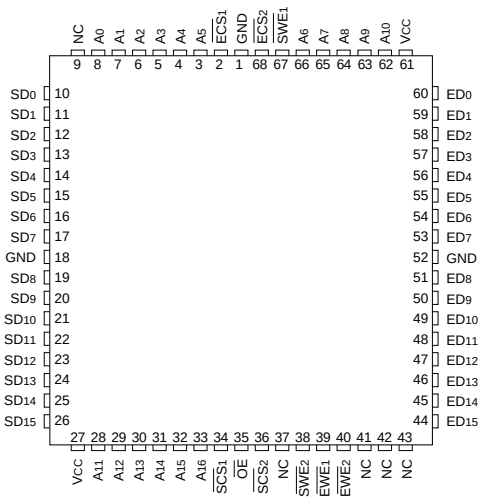
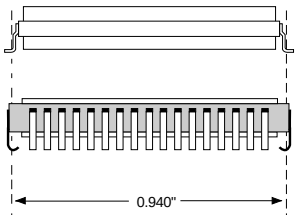


FIG. 2 PIN CONFIGURATION FOR WSE128K16-XG2TX

TOP VIEW



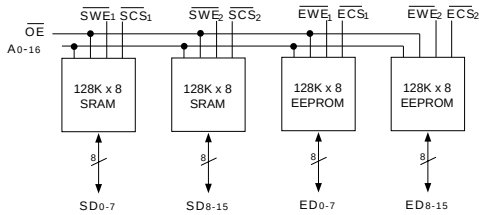


The WEDC 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

ED_{0-15}	EEPROM Data Inputs/Outputs
SD_{0-15}	SRAM Data Inputs/Outputs
A_{0-16}	Address Inputs
$\overline{SWE}_{1-2}$	SRAM Write Enable
$\overline{SCS}_{1-2}$	SRAM Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground
NC	Not Connected
$\overline{EWE}_{1-2}$	EEPROM Write Enable
$\overline{ECS}_{1-2}$	EEPROM Chip Select

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance HIP (PGA)	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
CQFP G2T			20	
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

EEPROM TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O
H	X	X	Standby	High Z
L	L	H	Read	Data Out
L	H	L	Write	Data In
X	H	X	Out Disable	High Z/Data Out
X	X	H	Write	
X	L	X	Inhibit	

SRAM TRUTH TABLE

$\overline{SCS}$	$\overline{OE}$	$\overline{SWE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Read	High Z	Active
L	X	L	Write	Data In	Active

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{SCS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
SRAM Operating Supply Current x 16 Mode	I_{CCx16}	$\overline{SCS}$ = V_{IL}, $\overline{OE}$ = $\overline{ECS}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		360	mA
Standby Current	I_{SB}	$\overline{ECS}$ = $\overline{SCS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		31.2	mA
SRAM Output Low Voltage (35 to 45ns)	V_{OL}	I_{OL} = 8.0mA, V_{CC} = 4.5		0.4	V
SRAM Output Low Voltage (70ns)	V_{OL}	I_{OL} = 2.1mA, V_{CC} = 4.5		0.4	V
SRAM Output High Voltage (35 to 45ns)	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		V
SRAM Output High Voltage (70ns)	V_{OH}	I_{OH} = -1mA, V_{CC} = 4.5	2.4		V
EEPROM Operating Supply Current x 16 Mode	I_{CC1}	$\overline{ECS}$ = V_{IL}, $\overline{OE}$ = $\overline{SCS}$ = V_{IH}		155	mA
EEPROM Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA, V_{CC} = 4.5V		0.45	V
EEPROM Output High Voltage	V_{OH1}	I_{OH} = 400 µA, V_{CC} = 4.5V	2.4		V

NOTES:

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 5 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

SRAM AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-35		-45		-70		Units
Read Cycle		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	35		45		70		ns
Address Access Time	t_{AA}		35		45		70	ns
Output Hold from Address Change	t_{OH}	0		0		3		ns
Chip Select Access Time	t_{ACS}		35		45		70	ns
Output Enable to Output Valid	t_{OE}		20		25		35	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	3		3		3		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		20		20		25	ns
Output Disable to Output in High Z	t_{OHZ}[1]		20		20		25	ns

1. This parameter is guaranteed by design but not tested.

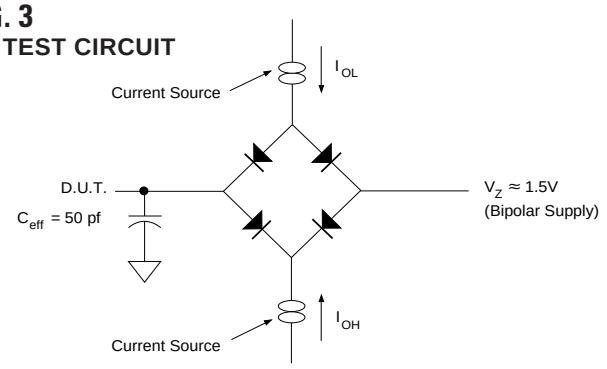
SRAM AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-35		-45		-70		Units
Write Cycle		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	35		45		70		ns
Chip Select to End of Write	t_{CW}	25		30		60		ns
Address Valid to End of Write	t_{AW}	25		30		60		ns
Data Valid to End of Write	t_{DW}	20		25		30		ns
Write Pulse Width	t_{WP}	25		30		50		ns
Address Setup Time	t_{AS}	0		0		5		ns
Address Hold Time	t_{AH}	0		0		5		ns
Output Active from End of Write	t_{OW}[1]	4		4		5		ns
Write Enable to Output in High Z	t_{WHZ}[1]		20		25		25	ns
Data Hold Time	t_{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 3
AC TEST CIRCUIT

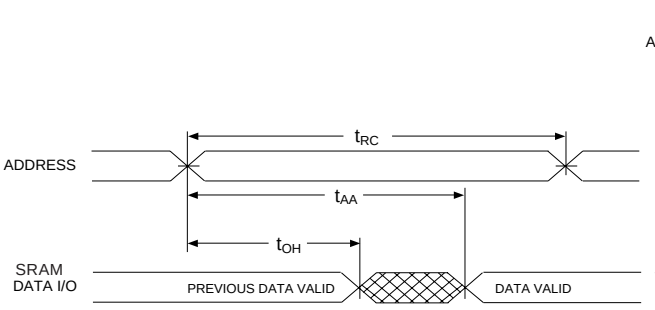


AC TEST CONDITIONS

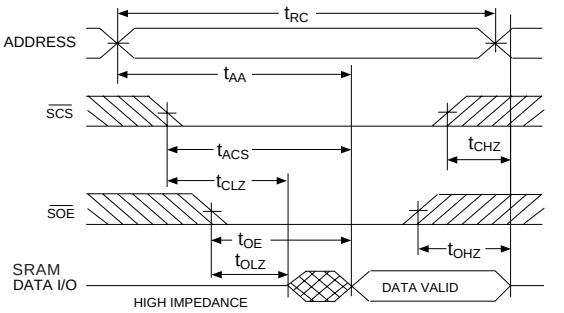
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 4 SRAM READ CYCLE

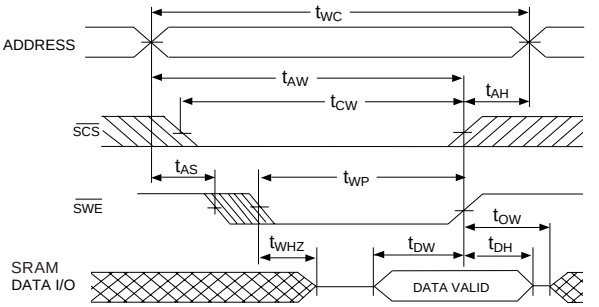


READ CYCLE 1, ($\overline{SCS}$ = $\overline{OE}$ = V_{IL}, $\overline{SWE}$ = V_{IH})



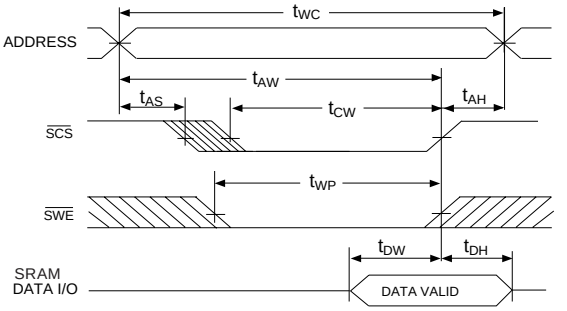
READ CYCLE 2, ($\overline{SWE}$ = V_{IH})

FIG. 5 SRAM WRITE CYCLE
$\overline{SWE}$ CONTROLLED



WRITE CYCLE 1, $\overline{SWE}$ CONTROLLED

FIG. 6 SRAM WRITE CYCLE
$\overline{SCS}$ CONTROLLED



WRITE CYCLE 2, $\overline{SCS}$ CONTROLLED

EEPROM WRITE

A write cycle is initiated when $\overline{OE}$ is high and a low pulse is on $\overline{EWE}$ or $\overline{ECS}$ with $\overline{ECS}$ or $\overline{EWE}$ low. The address is latched on the falling edge of $\overline{ECS}$ or $\overline{EWE}$ whichever occurs last. The data is latched by the rising edge of $\overline{ECS}$ or $\overline{EWE}$, whichever occurs first. A byte write operation will automatically continue to completion.

WRITE CYCLE TIMING

Figures 7 and 8 show the write cycle timing relationships. A write cycle begins with address application, write enable and chip select. Chip select is accomplished by placing the $\overline{ECS}$ line low. Write enable consists of setting the $\overline{EWE}$ line low. The write cycle begins when the last of either $\overline{ECS}$ or $\overline{EWE}$ goes low.

The $\overline{EWE}$ line transition from high to low also initiates an internal 150 µsec delay timer to permit page mode operation. Each subsequent $\overline{EWE}$ transition from high to low that occurs before the completion of the 150 µsec time out will restart the timer from zero. The operation of the timer is the same as a retriggerable one-shot.

EEPROM AC WRITE CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Write Cycle Parameter	Symbol	Min	Max	Unit
Write Cycle Time, TYP = 6ms	t_{WC}		10	ms
Address Set-up Time	t_{AS}	0		ns
Write Pulse Width ($\overline{EWE}$ or $\overline{ECS}$)	t_{WP}	150		ns
Chip Select Set-up Time	t_{CS}	0		ns
Address Hold Time	t_{AH}	100		ns
Data Hold Time	t_{DH}	10		ns
Chip Select Hold Time	t_{CSH}	0		ns
Data Set-up Time	t_{DS}	100		ns
Output Enable Set-up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
Write Pulse Width High	t_{WPH}	50		ns

FIG. 7 EEPROM WRITE WAVEFORMS
$\overline{EWE}$ CONTROLLED

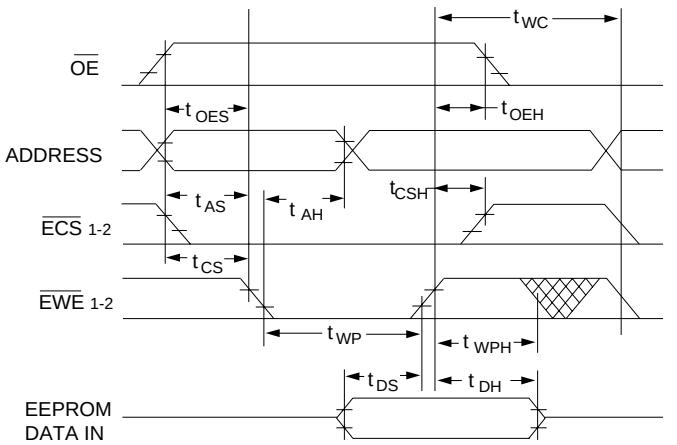
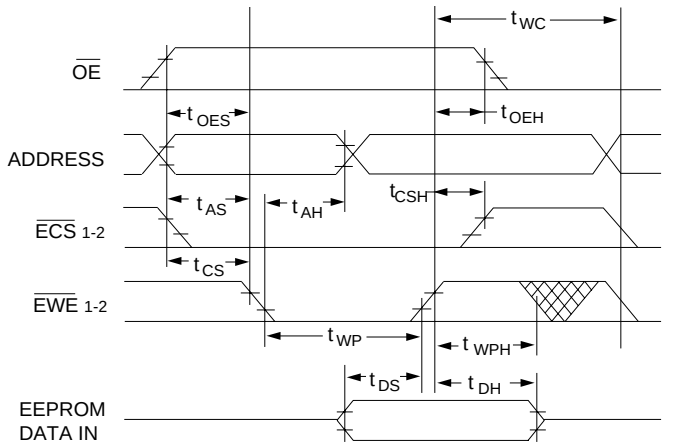


FIG. 8 EEPROM WRITE WAVEFORMS
$\overline{ECS}$ CONTROLLED



EEPROM READ

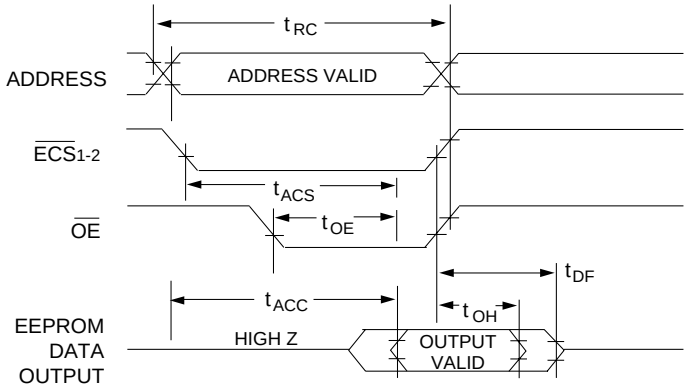
The WSE128K16-XXX EEPROM stores data at the memory location determined by the address pins. When $\overline{ECS}$ and $\overline{OE}$ are low and $\overline{EWE}$ is high, this data is present on the outputs. When $\overline{ECS}$ and $\overline{OE}$ are high, the outputs are in a high impedance state. This two line control prevents bus contention.

EEPROM AC READ CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Read Cycle Parameter	Symbol	-120		-150		-300		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		300		ns
Address Access Time	t_{ACC}		120		150		300	ns
Chip Select Access Time	t_{ACS}		120		150		300	ns
Output Hold from Add. Change, $\overline{OE}$ or $\overline{ECS}$	t_{OH}	0		0		0		ns
Output Enable to Output Valid	t_{OE}	0	50	0	55	0	85	ns
Chip Select or $\overline{OE}$ to High Z Output	t_{DF}		70		70		70	ns

FIG. 9 EEPROM READ WAVEFORMS



NOTES:
$\overline{OE}$ may be delayed up to t_{ACS} - t_{OE} after the falling edge of $\overline{ECS}$ without impact on t_{OE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.

EEPROM DATA POLLING

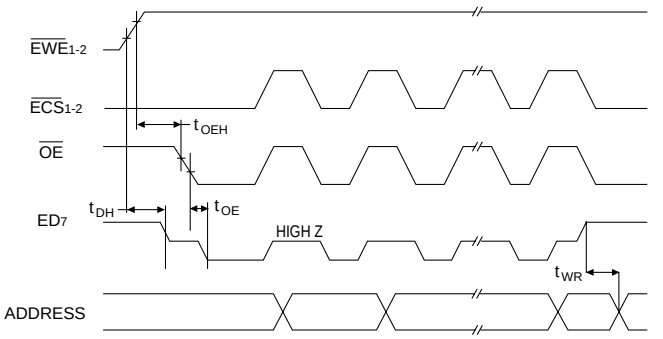
The WSE128K16-XXX offers a data polling feature for the EEPROM which allows a faster method of writing to the device. Figure 11 shows the timing diagram for this function. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data on D_7 (for each chip.) Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. Data polling may begin at any time during the write cycle.

EEPROM DATA POLLING CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Min	Max	Unit
Data Hold Time	t_{DH}	10		ns
$\overline{OE}$ Hold Time	t_{OEH}	10		ns
$\overline{OE}$ To Output Valid	t_{OE}		55	ns
Write Recovery Time	t_{WR}	0		ns

FIG. 10 EEPROM DATA POLLING WAVEFORMS



EEPROM PAGE WRITE OPERATION

The WSE128K16-XXX has a page write operation that allows one to 128 bytes of data to be written into the device and consecutively loads during the internal programming period. Successive bytes may be loaded in the same manner after the first data byte has been loaded. An internal timer begins a time out operation at each write cycle. If another write cycle is completed within 150µs or less, a new time out period begins. Each write cycle restarts the delay period. The write cycles can be continued as long as the interval is less than the time out period.

The usual procedure is to increment the least significant address lines from A0 through A6 at each write cycle. In this manner a page of up to 128 bytes can be loaded in to the EEPROM in a burst mode before beginning the relatively long interval programming cycle.

After the 150µs time out is completed, the EEPROM begins an internal write cycle. During this cycle the entire page of bytes will be written at the same time. The internal programming cycle is the same regardless of the number of bytes accessed.

EEPROM PAGE WRITE CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Page Mode Write Characteristics	Symbol			Unit
Parameter		**Min**	**Max**	
Write Cycle Time, TYP = 6ms	t_{WC}		10	ms
Address Set-up Time	t_{AS}	0		ns
Address Hold Time (1)	t_{AH}	100		ns
Data Set-up Time	t_{DS}	100		ns
Data Hold Time	t_{DH}	10		ns
Write Pulse Width	t_{WP}	150		ns
Byte Load Cycle Time	t_{BLC}		150	µs
Write Pulse Width High	t_{WPH}	50		ns

1. Page address must remain valid for duration of write cycle.

FIG. 11
EEPROM PAGE MODE WRITE WAVEFORMS

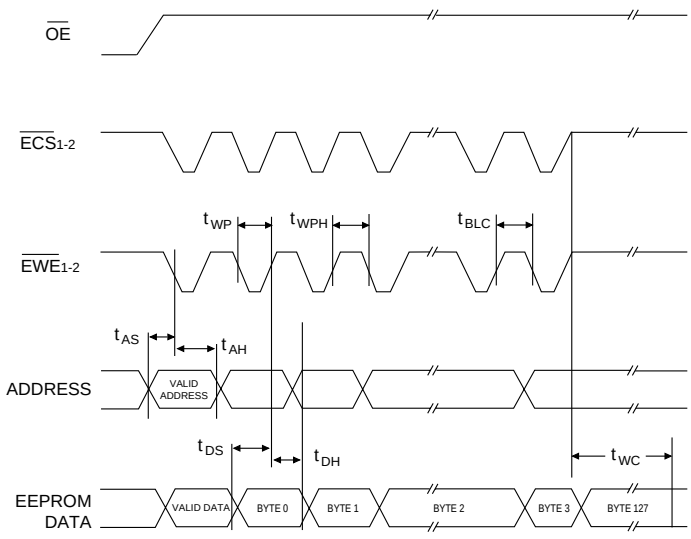
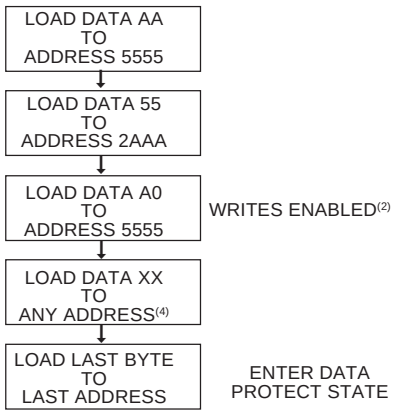
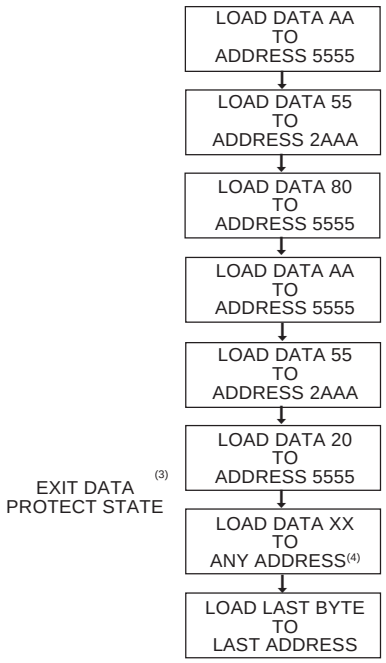


FIG. 12
EEPROM SOFTWARE DATA PROTECTION ENABLE ALGORITHM(1)



NOTES:
1. Data Format: ED_7 - ED_0 (Hex);
   Address Format: A_{16} - A_0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data may be loaded.

FIG. 13
EEPROM SOFTWARE DATA PROTECTION DISABLE ALGORITHM(1)



NOTES:
1. Data Format: ED_7 - ED_0 (Hex);
   Address Format: A_{16} - A_0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data may be loaded.

EEPROM SOFTWARE DATA PROTECTION

A software write protection feature may be enabled or disabled by the user. When shipped by WEDC, the WSE128K16-XXX has the feature disabled. Write access to the device is unrestricted.

To enable software write protection, the user writes three access code bytes to three special internal locations. Once write protection has been enabled, each write to the EEPROM must use the same three byte write sequence to permit writing. After setting software data protection, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device, however, for the duration of t_{WC}. The write protection feature can be disabled by a six byte write sequence of specific data to specific locations. Power transitions will not reset the software write protection.

Each 128K byte block of the EEPROM has independent write protection. One or more blocks may be enabled and the rest disabled in any combination. The software write protection guards against inadvertent writes during power transitions, or unauthorized modification using a PROM programmer.

EEPROM HARDWARE DATA PROTECTION

These features protect against inadvertent writes to the WSE128K16-XXX. These are included to improve reliability during normal operation:

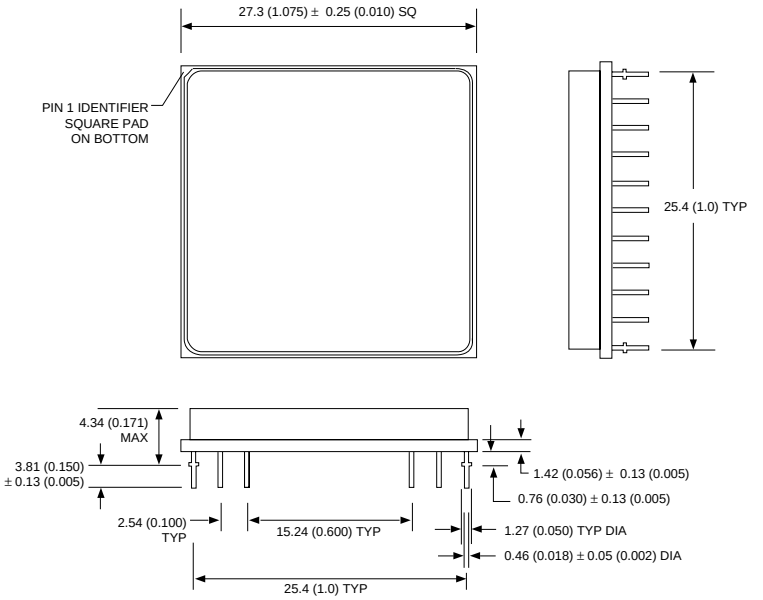
a) Vcc power on delay
As V_{CC} climbs past 3.8V typical the device will wait 5msec typical before allowing write cycles.

b) Vcc sense
While below 3.8V typical write cycles are inhibited.

c) Write inhibiting
Holding $\overline{OE}$ low and either $\overline{ECS}$ or $\overline{EWE}$ high inhibits write cycles.

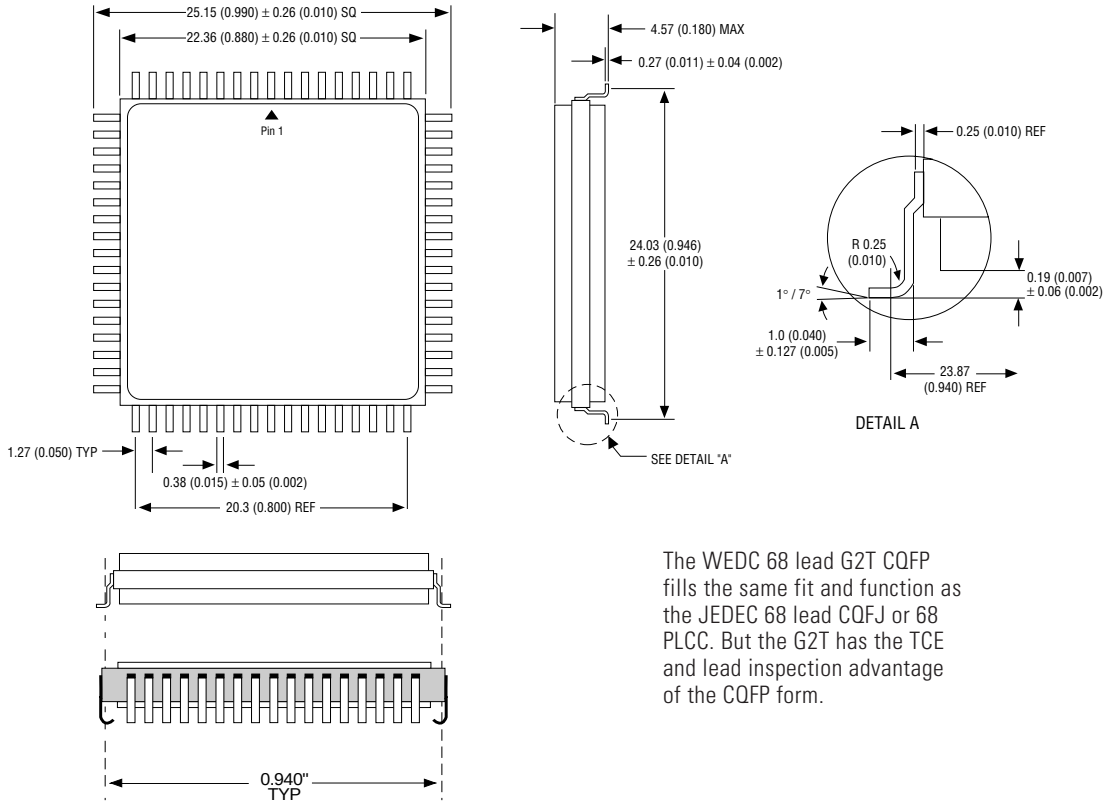
d) Noise filter
Pulses of <8ns (typ) on $\overline{EWE}$ or $\overline{ECS}$ will not initiate a write cycle.

PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)



The WEDC 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION