128Kx16 SRAM/FLASH MODULE, SMD 5962-96900

FEATURES

- Access Times of 35ns (SRAM) and 70ns (FLASH)
- Access Times of 70ns (SRAM) and 120ns (FLASH)
- Packaging
  - 66-pin, PGA Type, 1.075 inch square HIP, Hermetic Ceramic HIP (Package 400)
  - 66-pin, PGA Type, 1.185 inch square HIP, Hermetic Ceramic HIP (Package 401)
  - 68 lead, Hermetic CQFP (G1U), 22.4mm (0.880 inch) square (Package 519). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 2)
- 128Kx16 SRAM
- 128Kx16 5V FLASH
- Organized as 128Kx16 of SRAM and 128Kx16 of Flash Memory with separate Data Buses
- Both blocks of memory are User Configurable as 256Kx8
- Low Power CMOS
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  - WSF128K16-XHX - 13 grams typical
  - WSF128K16-H1X - 13 grams typical
  - WSF128K16-XG1UX - 5 grams typical

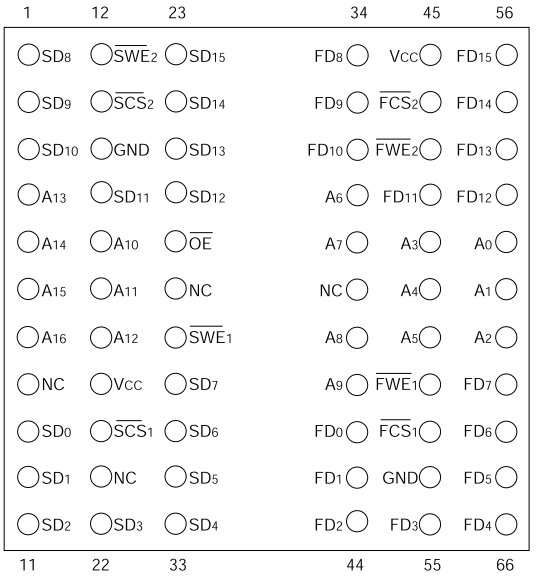
FLASH MEMORY FEATURES

- 10,000 Erase/Program Cycles
- Sector Architecture
  - 8 equal size sectors of 16K bytes each
  - Any combination of sectors can be concurrently erased.
    Also supports full chip erase
- 5 Volt Programming; 5V ± 10% Supply
- Embedded Erase and Program Algorithms
- Hardware Write Protection
- Page Program Operation and Internal Program Control Time.

Note: For programming information refer to Flash Programming 1M5 Application Note.

FIG. 1 PIN CONFIGURATION FOR WSF128K16-XHX AND WSF128K16-XH1X

TOP VIEW



PIN DESCRIPTION

FD0-15	Flash Data Inputs/Outputs
SD0-15	SRAM Data Inputs/Outputs
A0-16	Address Inputs
$\overline{SWE}_{1-2}$	SRAM Write Enable
$\overline{SCS}_{1-2}$	SRAM Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected
$\overline{FWE}_{1-2}$	Flash Write Enable
$\overline{FCS}_{1-2}$	Flash Chip Select

BLOCK DIAGRAM

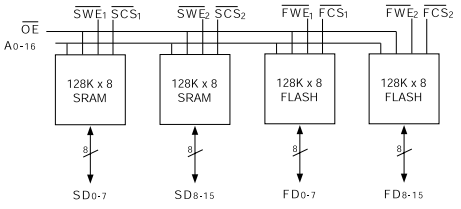
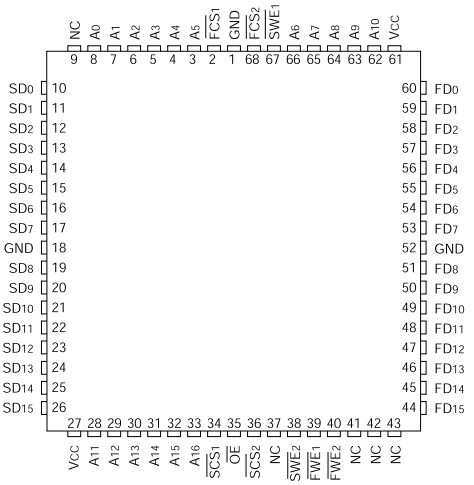
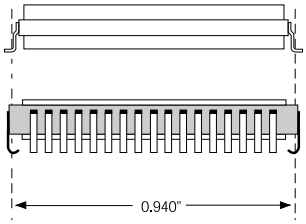


FIG. 2 PIN CONFIGURATION FOR WSF128K16-XG1UX

TOP VIEW



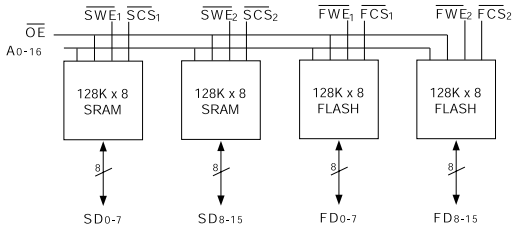


The WEDC 68 lead G1U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G1U has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

FD_{0-15}	Flash Data Inputs/Outputs
SD_{0-15}	SRAM Data Inputs/Outputs
A_{0-16}	Address Inputs
$\overline{SWE}_{1-2}$	SRAM Write Enable
$\overline{SCS}_{1-2}$	SRAM Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground
NC	Not Connected
$\overline{FWE}_{1-2}$	Flash Write Enable
$\overline{FCS}_{1-2}$	Flash Chip Select

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	7.0	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

Parameter	
Flash Data Retention	10 years
Flash Endurance (write/erase cycles)	10,000

NOTES:
1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

SRAM TRUTH TABLE

$\overline{SCS}$	$\overline{OE}$	$\overline{SWE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Read	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE
(TA = +25°C)

Test	Symbol	Condition	Max	Unit
$\overline{OE}$ Capacitance	C_{OE}	V_{IN} = 0V, f = 1.0MHz	50	pF
F/S $\overline{WE}$ 1-2 Capacitance	C_{WE}	V_{IN} = 0V, f = 1.0MHz	20	pF
F/S $\overline{CS}$ 1-2 Capacitance	C_{CS}	V_{IN} = 0V, f = 1.0MHz	20	pF
SD_{0-15}/FD_{0-15} Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1.0MHz	20	pF
A_0 - A_{16} Capacitance	C_{AD}	V_{IN} = 0V, f = 1.0MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS
(VCC = 5.0V, VSS = 0V, TA = -55°C TO +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{SCS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
SRAM Operating Supply Current x 16 Mode	I_{CCx16}	$\overline{SCS}$ = V_{IL}, $\overline{OE}$ = $\overline{FCS}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		360	mA
Standby Current	I_{SB}	$\overline{FCS}$ = $\overline{SCS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		40	mA
SRAM Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, V_{CC} = 4.5		0.4	V
SRAM Output High Voltage	V_{OH}	I_{OH} = -1.0mA, V_{CC} = 4.5	2.4		V
Flash V_{CC} Active Current for Read (1)	I_{CC1}	$\overline{FCS}$ = V_{IL}, $\overline{OE}$ = $\overline{SCS}$ = V_{IH}		100	mA
Flash V_{CC} Active Current for Program or Erase (2)	I_{CC2}	$\overline{FCS}$ = V_{IL}, $\overline{OE}$ = $\overline{SCS}$ = V_{IH}		130	mA
Flash Output Low Voltage	V_{OL}	I_{OL} = 8.0mA, V_{CC} = 4.5		0.45	V
Flash Output High Voltage	V_{OH1}	I_{OH} = -2.5 mA, V_{CC} = 4.5	0.85 x V_{CC}		V
Flash Output High Voltage	V_{OH2}	I_{OH} = -100 µA, V_{CC} = 4.5	V_{CC} -0.4		V
Flash Low V_{CC} Lock Out Voltage	V_{LKO}		3.2		V

NOTES:
1. The ICC current listed includes both the DC operating current and the frequency dependent component (@ 5 MHz).
The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at VIH.
2. ICC active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: VIL = 0.3V, VIH = VCC - 0.3V

SRAM AC CHARACTERISTICS
(VCC = 5.0V, TA = -55°C TO +125°C)

Parameter Read Cycle	Symbol	-35 Min	-35 Max	-70 Min	-70 Max	Unit
Read Cycle Time	t_{RC}	35		70		ns
Address Access Time	t_{AA}		35		70	ns
Output Hold from Address Change	t_{OH}	0		3		ns
Chip Select Access Time	t_{ACS}		35		70	ns
Output Enable to Output Valid	t_{OE}		20		35	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	3		3		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		20		25	ns
Output Disable to Output in High Z	t_{OHZ}[1]		20		25	ns

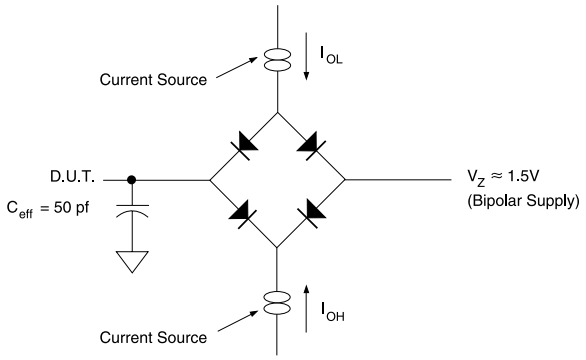
1. This parameter is guaranteed by design but not tested.

SRAM AC CHARACTERISTICS
(VCC = 5.0V, TA = -55°C TO +125°C)

Parameter Write Cycle	Symbol	-35 Min	-35 Max	-70 Min	-70 Max	Unit
Write Cycle Time	t_{WC}	35		70		ns
Chip Select to End of Write	t_{CW}	25		60		ns
Address Valid to End of Write	t_{AW}	25		60		ns
Data Valid to End of Write	t_{DW}	20		30		ns
Write Pulse Width	t_{WP}	25		50		ns
Address Setup Time	t_{AS}	0		5		ns
Address Hold Time	t_{AH}	0		5		ns
Output Active from End of Write	t_{OW}[1]	4		5		ns
Write Enable to Output in High Z	t_{WHZ}[1]		20		25	ns
Data Hold from Write Time	t_{DH}	0		0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 3 AC TEST CIRCUIT

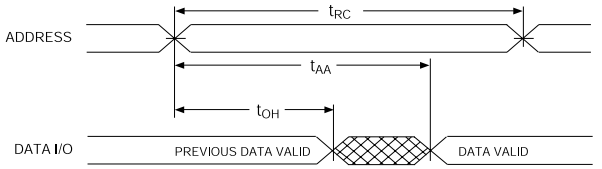


AC TEST CONDITIONS

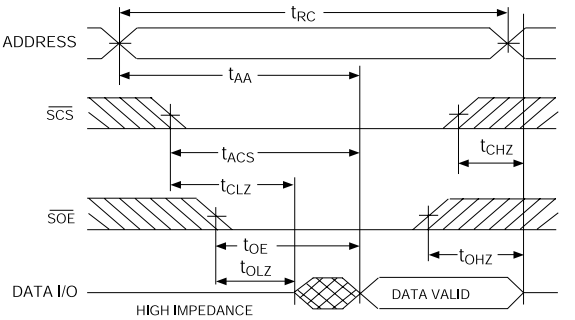
Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
VZ is programmable from -2V to +7V.
IOL & IOH programmable from 0 to 16mA.
Tester Impedance Z0 = 75Ω.
VZ is typically the midpoint of VOH and VOL.
IOL & IOH are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 4 SRAM TIMING WAVEFORM – READ CYCLE

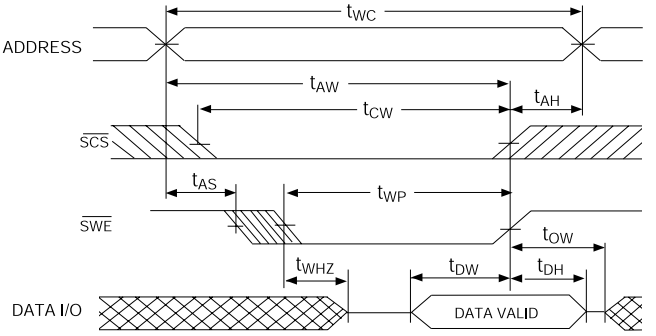


READ CYCLE 1, ($\overline{SCS}$ = $\overline{OE}$ = V_{IL}, $\overline{SWE}$ = V_{IH})



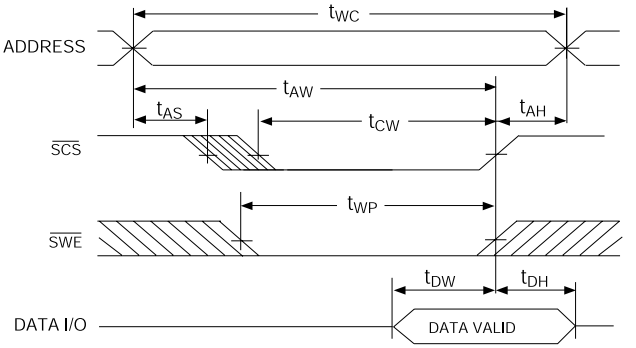
READ CYCLE 2, ($\overline{SWE}$ = V_{IH})

FIG. 5 SRAM WRITE CYCLE – $\overline{SWE}$ CONTROLLED



WRITE CYCLE 1, $\overline{SWE}$ CONTROLLED

FIG. 6 SRAM WRITE CYCLE – $\overline{SCS}$ CONTROLLED



WRITE CYCLE 2, $\overline{SCS}$ CONTROLLED

FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{FWE}$ CONTROLLED
(VCC = 5.0V, TA = -55°C TO +125°C)

Parameter	Symbol		-70		-120		Unit
			Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	70		120		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	35		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	30		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		50		ns
Chip Select Hold Time	t_{WHEH}	t_{CH}	0		0		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		ns
Duration of Byte Programming Operation (min)	t_{WHWH1}		14		14		µs
Chip and Sector Erase Time	t_{WHWH2}		2.2	60	2.2	60	sec
Read Recovery Time Before Write	t_{GHWL}		0		0		µs
V_{CC} Set-up Time		t_{VCS}	50		50		µs
Chip Programming Time				12.5		12.5	sec
Output Enable Setup Time		t_{OES}	0		0		ns
Output Enable Hold Time (1)		t_{OEH}	10		10		ns

1. For Toggle and $\overline{Data}$ Polling.

FLASH AC CHARACTERISTICS – READ ONLY OPERATIONS
(VCC = 5.0V, TA = -55°C TO +125°C)

Parameter	Symbol		-70		-120		Unit
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	70		120		ns
Address Access Time	t_{AVQV}	t_{ACC}		70		120	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		70		120	ns
$\overline{OE}$ to Output Valid	t_{GLQV}	t_{OE}		35		50	ns
Chip Select to Output High Z (1)	t_{EHQZ}	t_{DF}		20		30	ns
$\overline{OE}$ High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		30	ns
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$ Change, whichever is first	t_{AXQX}	t_{OH}	0		0		ns

1. Guaranteed by design, not tested.

FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{FCS}$ CONTROLLED
(VCC = 5.0V, TA = -55°C TO +125°C)

Parameter	Symbol		-70		-120		Unit
			Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	70		120		ns
$\overline{FWE}$ Setup Time	t_{WLEL}	t_{WS}	0		0		ns
$\overline{FCS}$ Pulse Width	t_{ELEH}	t_{CP}	35		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	30		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		50		ns
$\overline{FWE}$ Hold from $\overline{FWE}$ High	t_{EHWH}	t_{WH}	0		0		ns
$\overline{FCS}$ Pulse Width High	t_{EHEL}	t_{CPH}	20		20		ns
Duration of Programming Operation	t_{WHWH1}		14		14		µs
Duration of Erase Operation	t_{WHWH2}		2.2	60	2.2	60	sec
Read Recovery before Write	t_{GHEL}		0		0		ns
Chip Programming Time				12.5		12.5	sec

FIG. 7 AC WAVEFORMS FOR FLASH MEMORY READ OPERATIONS

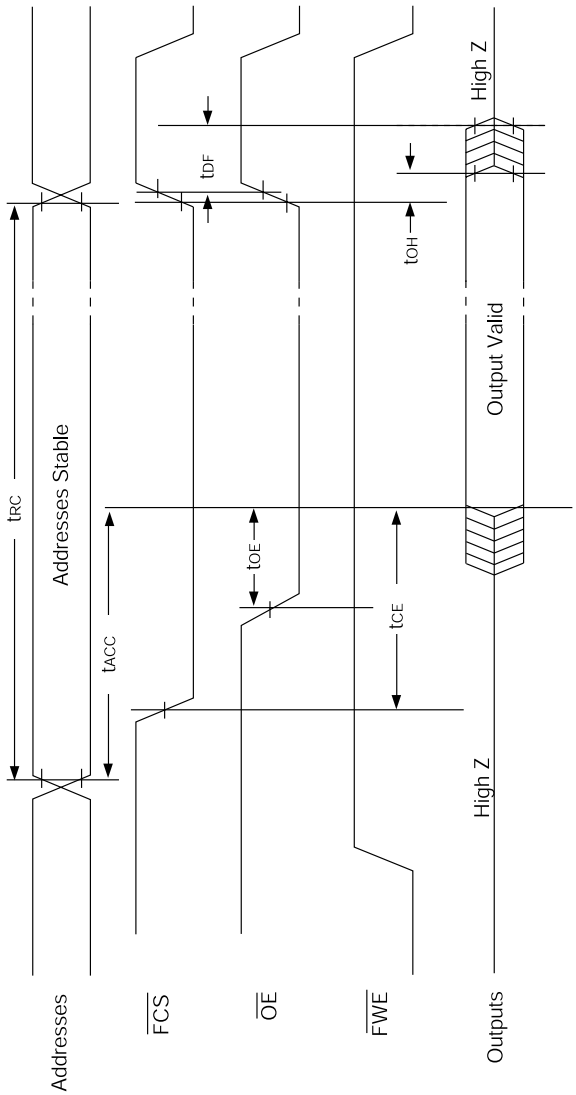
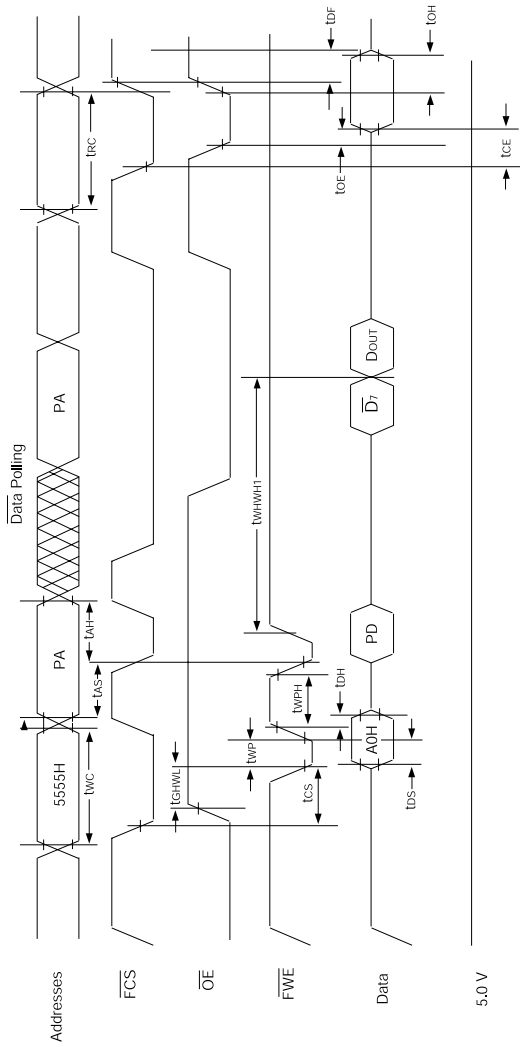
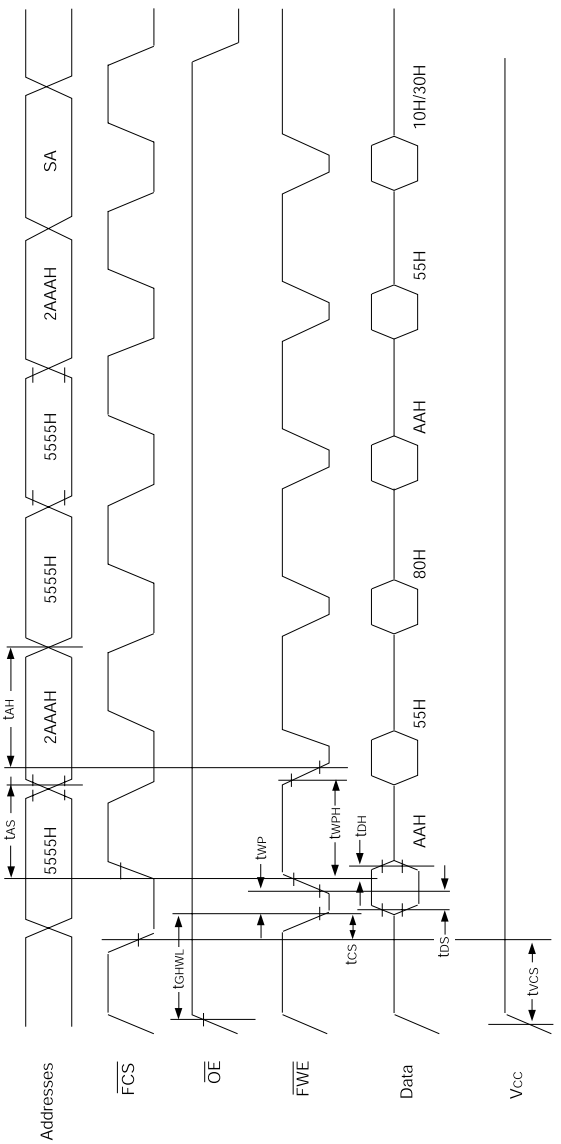


FIG. 8 WRITE/ERASE/PROGRAM OPERATION, FLASH MEMORY $\overline{FWE}$ CONTROLLED



NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

FIG. 9 AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS FOR FLASH MEMORY



Notes:
1. SA is the sector address for Sector Erase.

FIG. 10 AC WAVEFORMS FOR $\overline{\text{DATA}}$ POLLING DURING EMBEDDED ALGORITHM OPERATIONS FOR FLASH MEMORY

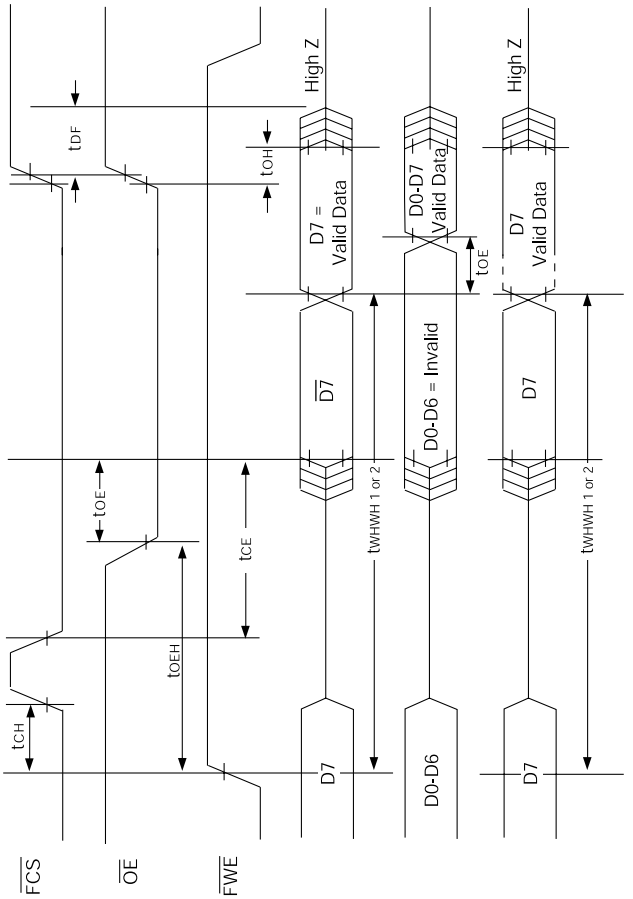
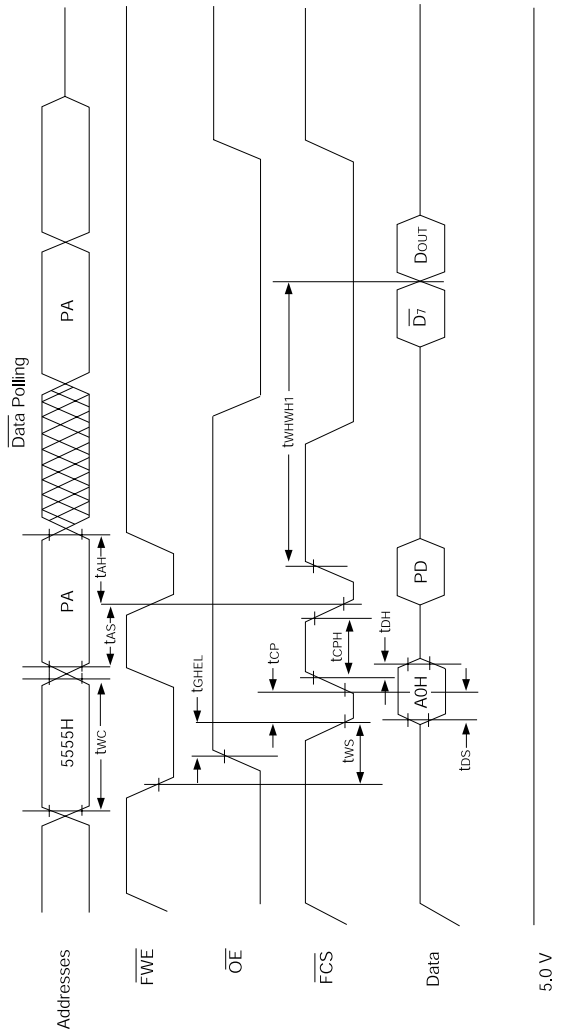


FIG. 11 WRITE/ERASE/PROGRAM OPERATION FOR FLASH MEMORY, $\overline{CS}$ CONTROLLED



NOTES:

1. PA represents the address of the memory location to be programmed.
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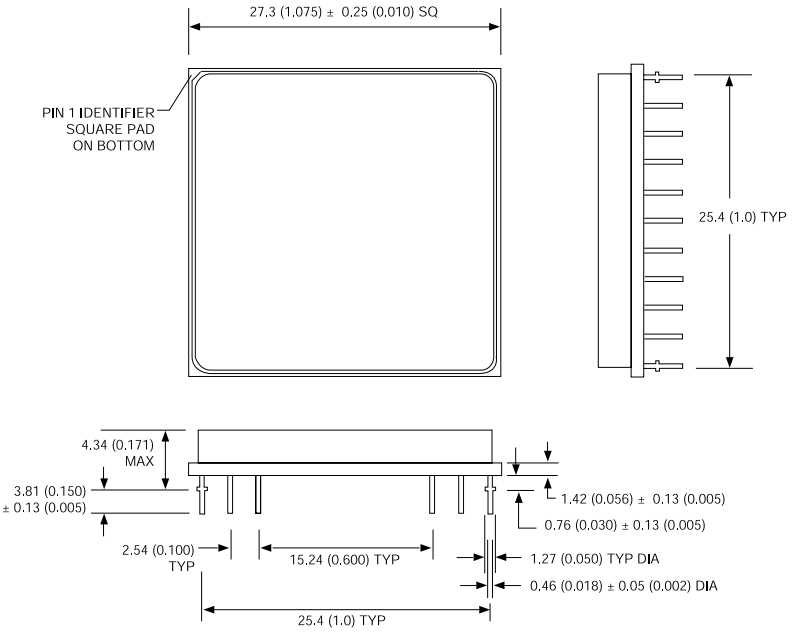
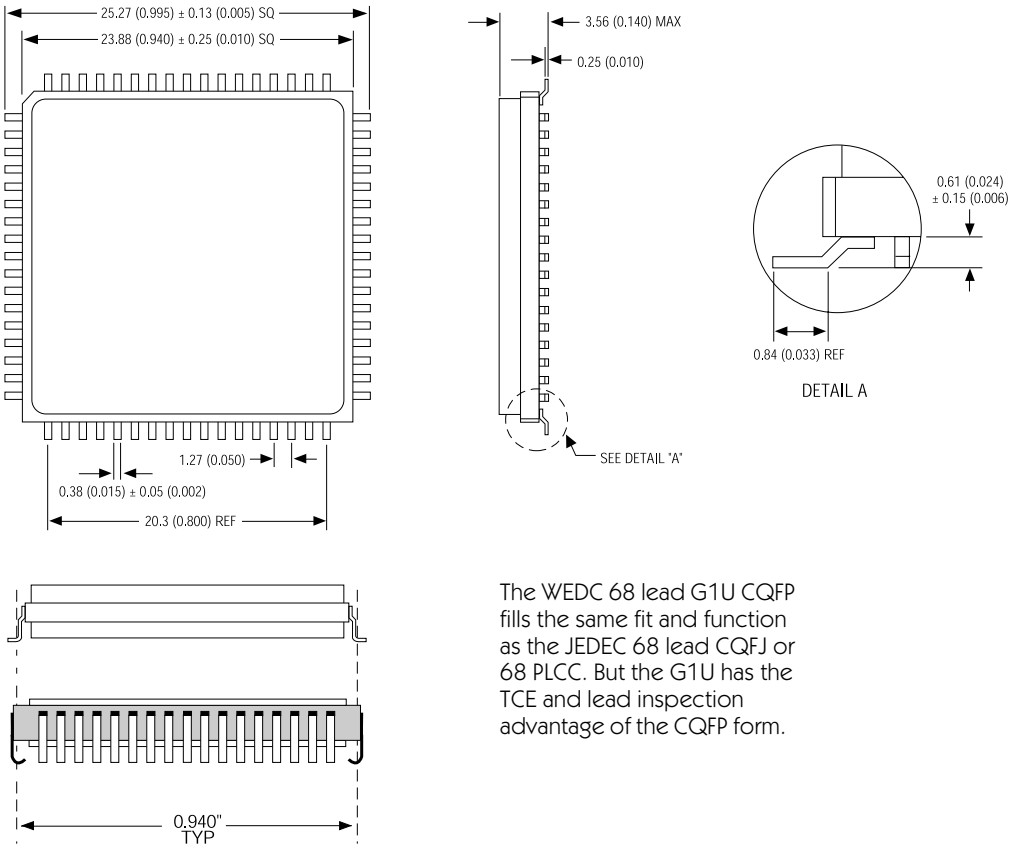
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 519: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G1U)



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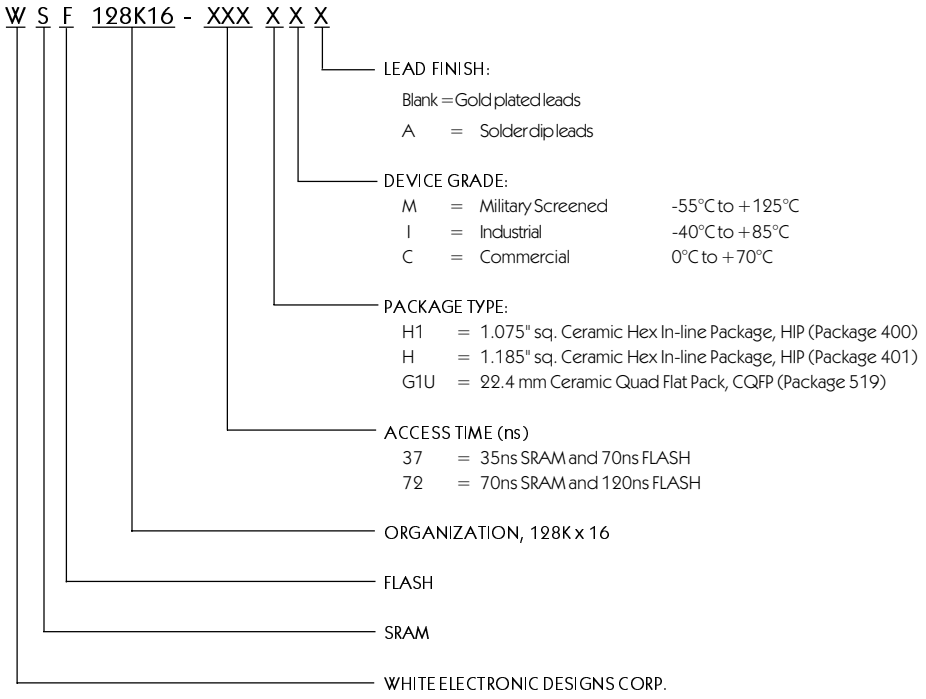
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION



DEVICE TYPE	SRAM SPEED	FLASH SPEED	PACKAGE	SMD NO.
128K x 16 Mixed Module	70ns	120ns	66 pin HIP (H)	5962-96900 01HXX
128K x 16 Mixed Module	70ns	120ns	66 pin HIP (H1)	5962-96900 01HYX
128K x 16 Mixed Module	35ns	70ns	66 pin HIP (H)	5962-96900 02HXX
128K x 16 Mixed Module	35ns	70ns	66 pin HIP (H1)	5962-96900 02HYX
128K x 16 Mixed Module	70ns	120ns	68 lead CQFP/J (G1U)	5962-96900 01HX*
128K x 16 Mixed Module	35ns	70ns	68 lead CQFP/J (G1U)	5962-96900 02HX*

SMD Pending