512MB – 64Mx72 DDR2 SDRAM REGISTERED DIMM, w/PLL

FEATURES

- Registered 240-pin, dual in-line memory module
- Fast data transfer rates: PC2-6400*, PC2-5300*, PC2-4200 and PC2-3200
- Utilizes 800*, 667*, 533 and 400 MT/s DDR2 SDRAM components
- $V_{CC} = V_{CCQ} = 1.8V \pm 0.1V$
- $V_{CCSPD} = 1.7V$ to $3.6V$
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Write Latency = Read Latency 1^{tck}
- Programmable CAS# latency (CL): 3, 4, 5* and 6*
- Adjustable data-output drive strength
- On-die termination (ODT)
- 7.8µs average periodic refresh interval
- Posted CAS# latency: 0, 1, 2, 3 and 4
- Serial Presence Detect (SPD) with EEPROM
- Auto & Self Refresh (8k/64ms refresh)
- Gold edge contacts
- RoHS compliant
- Package option
  - 240 Pin DIMM
  - PCB – 30.00mm (1.181") TYP

DESCRIPTION

The WV3HG64M72EER is a 64Mx72 Double Data Rate DDR2 SDRAM high density module. This memory module consists of nine 64Mx8 bit with 4 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 240-pin DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:
- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-3200	PC2-4200	PC2-5300*	PC2-6400*
Clock Speed	200MHz	266MHz	333MHz	400MHz
CL-t_{RCD}-t_{RP}	3-3-3	4-4-4	5-5-5	6-6-6

* Consult factory for availability

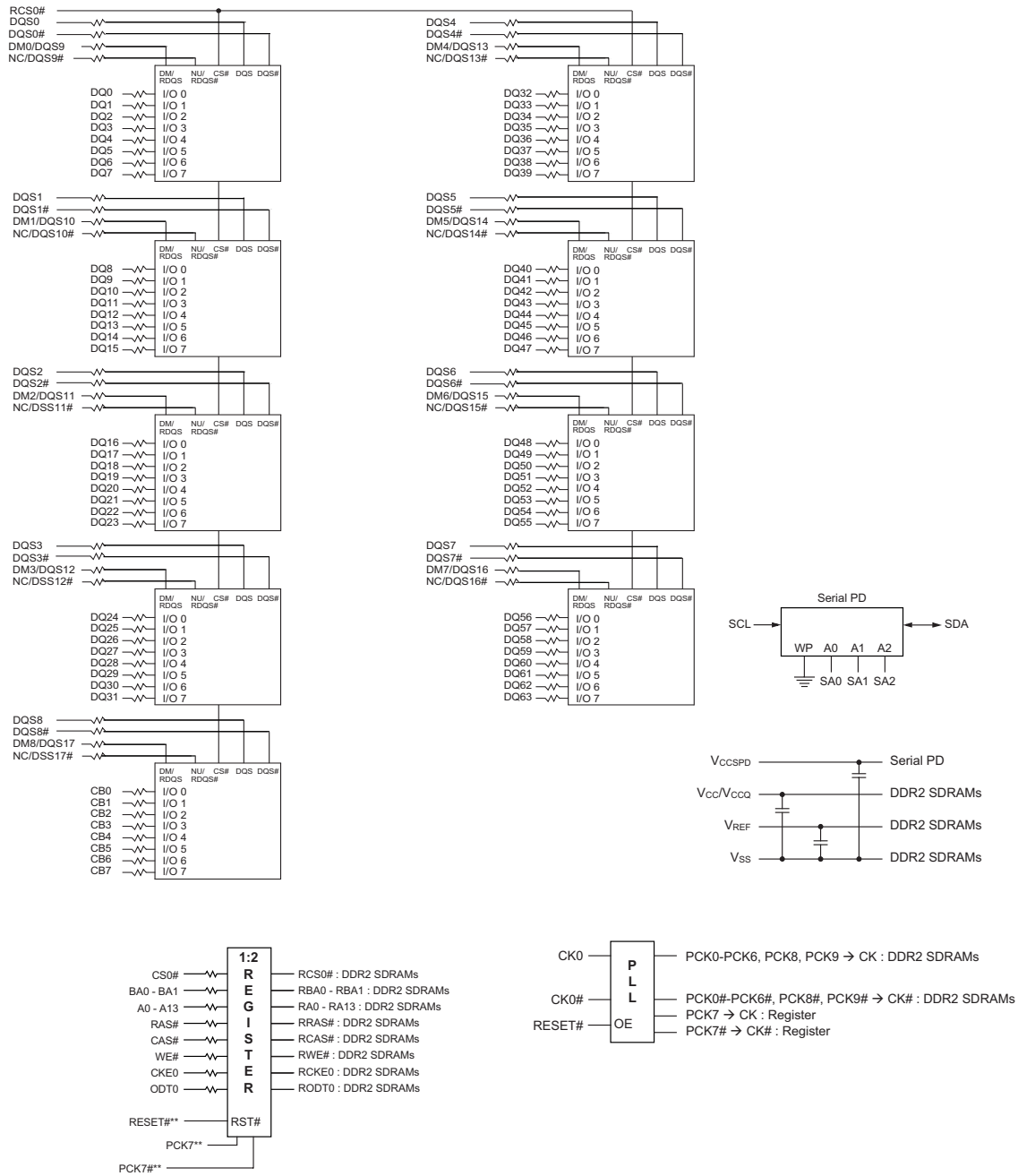
PIN CONFIGURATION

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	V_{REF}	61	A4	121	V_{SS}	181	V_{CC}
2	V_{SS}	62	V_{CC}	122	DQ4	182	A3
3	DQ0	63	A2	123	DQ5	183	A1
4	DQ1	64	V_{CC}	124	V_{SS}	184	V_{CC}
5	V_{SS}	65	V_{SS}	125	DM0/DQS9	185	CK0
6	DQS0#	66	V_{SS}	126	NC/DQS9#	186	CK0#
7	DQS0	67	V_{CC}	127	V_{SS}	187	V_{CC}
8	V_{SS}	68	NC	128	DQ6	188	A0
9	DQ2	69	V_{CC}	129	DQ7	189	V_{CC}
10	DQ3	70	A10/AP	130	V_{SS}	190	BA1
11	V_{SS}	71	BA0	131	DQ12	191	V_{CC}
12	DQ8	72	V_{CC}	132	DQ13	192	RAS#
13	DQ9	73	WE#	133	V_{SS}	193	CS0#
14	V_{SS}	74	CAS#	134	DM1/DQS10	194	V_{CC}
15	DQS1#	75	V_{CC}	135	NC/DQS10#	195	ODT0
16	DQS1	76	NC	136	V_{SS}	196	A13
17	V_{SS}	77	NC	137	NC	197	V_{CC}
18	RESET#	78	V_{CC}	138	NC	198	V_{SS}
19	NC	79	V_{SS}	139	V_{SS}	199	DQ36
20	V_{SS}	80	DQ32	140	DQ14	200	DQ37
21	DQ10	81	DQ33	141	DQ15	201	V_{SS}
22	DQ11	82	V_{SS}	142	V_{SS}	202	DM4/DQS13
23	V_{SS}	83	DQS4#	143	DQ20	203	NC/DQS13#
24	DQ16	84	DQS4	144	DQ21	204	V_{SS}
25	DQ17	85	V_{SS}	145	V_{SS}	205	DQ38
26	V_{SS}	86	DQ34	146	DM2/DQS11	206	DQ39
27	DQS2#	87	DQ35	147	NC/DQS11#	207	V_{SS}
28	DQS2	88	V_{SS}	148	V_{SS}	208	DQ44
29	V_{SS}	89	DQ40	149	DQ22	209	DQ45
30	DQ18	90	DQ41	150	DQ23	210	V_{SS}
31	DQ19	91	V_{SS}	151	V_{SS}	211	DM5/DQS14
32	V_{SS}	92	DQS5#	152	DQ28	212	NC/DQS14#
33	DQ24	93	DQS5	153	DQ29	213	V_{SS}
34	DQ25	94	V_{SS}	154	V_{SS}	214	DQ46
35	V_{SS}	95	DQ42	155	DM3/DQS12	215	DQ47
36	DQS3#	96	DQ43	156	NC/DQS12#	216	V_{SS}
37	DQS3	97	V_{SS}	157	V_{SS}	217	DQ52
38	V_{SS}	98	DQ48	158	DQ30	218	DQ53
39	DQ26	99	DQ49	159	DQ31	219	V_{SS}
40	DQ27	100	V_{SS}	160	V_{SS}	220	NC
41	V_{SS}	101	SA2	161	CB4	221	NC
42	CB0	102	NC	162	CB5	222	V_{SS}
43	CB1	103	V_{SS}	163	V_{SS}	223	DM6/DQS15
44	V_{SS}	104	DQS6#	164	DM8/DQS17	224	NC/DQS15#
45	DQS8#	105	DQS6	165	NC/DQS17#	225	V_{SS}
46	DQS8	106	V_{SS}	166	V_{SS}	226	DQ54
47	V_{SS}	107	DQ50	167	CB6	227	DQ55
48	CB2	108	DQ51	168	CB7	228	V_{SS}
49	CB3	109	V_{SS}	169	V_{SS}	229	DQ60
50	V_{SS}	110	DQ56	170	V_{CC}	230	DQ61
51	V_{CC}	111	DQ57	171	NC	231	V_{SS}
52	CKE0	112	V_{SS}	172	V_{CC}	232	DM7/DQS16
53	V_{CC}	113	DQS7#	173	NC	233	NC/DQS16#
54	NC	114	DQS7	174	NC	234	V_{SS}
55	NC	115	V_{SS}	175	V_{CC}	235	DQ62
56	V_{CC}	116	DQ58	176	A12	236	DQ63
57	A11	117	DQ59	177	A9	237	V_{SS}
58	A7	118	V_{SS}	178	V_{CC}	238	V_{CC}SPD
59	V_{CC}	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

PIN NAMES

Pin Name	Function
A0-A13	Address Inputs
BA0,BA1	SDRAM Bank Addresses
DQ0-DQ63	Data Input/Output
CB0-CB7	Check Bits
DQS0-DQS17	Data strobes
DQS0#-DQS17#	Data strobes complement
DM0 - DM8	Data Masks
ODT0	On-die termination control
CK0,CK0#	Clock Inputs
CKE0	Clock Enable
CS0#	Chip Select
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
RESET#	Register Reset Input/PLL OE
V_{CC}	Core and I/O Power (1.8V)
V_{SS}	Ground
SA0-SA2	SPD address
SDA	SPD Data Input/Output
SCL	Serial Presence Detect(SPD) Clock Input
V_{REF}	Input/Output Reference Voltage
V_{CC}SPD	SPD Power
NC	Spare pins, No connect

FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor values are 22 ohms unless otherwise specified.

**RESET#, PCK7 and RCK7# connects both registers. Other signals connect to one of two registers.

DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply Voltage	V_{CC}	1.7	1.8	1.9	V	3
I/O Reference Voltage	V_{REF}	0.49 x V_{CC}	0.50 x V_{CC}	0.51 x V_{CC}	V	1
I/O Termination Voltage	V_{TT}	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	2
SPD Supply Voltage	V_{CCSPD}	1.7	-	3.6	V	

Notes:

1 V_{REF} is expected to equal $V_{CC/2}$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed +/-2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.

2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

3. V_{CCQ} of all IC's are tied to V_{CC}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Units
V_{CC}	Voltage on V_{CC} pin relative to V_{SS}		-0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		- 0.5	2.3	V
T_{STG}	Storage Temperature		-55	100	°C
I_L	Input leakage current: Any input 0V<VIN<V_{CC}; V_{REF} input 0V<VIN<0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#, CS#, CKE	-5	5	µA
		CK, CK#	-10	10	
		DM	-5	5	
I_{OZ}	Output leakage current; 0V<VOUT<V_{CC}; DQs and ODT are disable	DQ, DQS, DQS#	-5	5	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = Valid V_{REF} level		-18	18	µA

CAPACITANCE

T_A = 25°C, f = 100MHz

Parameter	Symbol	Min	Max	Units
Input Capacitance: (A0~A13, BA0~BA1, RAS#, CAS#, WE#)	CIN_1	11	12	pF
Input Capacitance: (CKE0), (ODT0)	CIN_2	11	12	pF
Input Capacitance: (CS0#)	CIN_3	11	12	pF
Input Capacitance: (CK0, CK0#)	CIN_4	10	11	pF
Input Capacitance: (DM0~DM8), DQS0~DQS17)	CIN_5	6.5	8	pF
Input/Output Capacitance: (DQ0 ~ DQ63), (CB0 ~CB7)	$COUT_1$	6.5	8	pF

OPERATING TEMPERATURE CONDITION

Parameter	Symbol	Rating	Units	Notes
Operating Case Temperature (Commercial)	TOPER	0 to +85°C	°C	1, 2

NOTE:

1. Operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51.2
2. At 0 to +85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF} + 0.125	V_{CC} + 0.300	V
Input Low (Logic 0) Voltage	V_{IL}(DC)	- 0.300	VREF - 0.125	V

INPUT AC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
AC Input High (Logic 1) Voltage DDR2-400 & DDR2-533	V_{IH}(AC)	V_{REF} + 0.250	-	V
AC Input High (Logic 1) Voltage DDR2-667	V_{IH}(AC)	V_{REF} + 0.200	-	V
AC Input High (Logic 0) Voltage DDR2-400 & DDR2-533	V_{IL}(AC)	-	V_{REF} - 0.250	V
AC Input High (Logic 0) Voltage DDR2-667	V_{IL}(AC)	-	V_{REF} - 0.200	V

DDR2 I_{CC} SPECIFICATIONS AND CONDITIONS

Includes DDR2 SDRAM components only

Symbol	Proposed Conditions		806	665	534	403	Units
I_{CC0}*	Operating one bank active-precharge current; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RAS} = t_{RAS}min(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	TBD	1,120	1,120	mA
I_{CC1}*	Operating one bank active-read-precharge current; I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RAS} = t_{RAS}min(I_{CC})$, $t_{RCD} = t_{RCD}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{CC}4W		TBD	TBD	1,255	1,255	mA
I_{CC2P}*	Precharge power-down current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		TBD	TBD	472	472	mA
I_{CC2Q}**	Precharge quiet standby current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		TBD	TBD	670	670	mA
I_{CC2N}**	Precharge standby current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	TBD	715	715	mA
I_{CC3P}**	Active power-down current; All banks open; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	TBD	TBD	670	670	mA
		Slow PDN Exit MRS(12) = 1	TBD	TBD	508	508	mA
I_{CC3N}**	Active standby current; All banks open; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}max(I_{CC})$, $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	TBD	850	850	mA
I_{CC4W}*	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}max(I_{CC})$, $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	TBD	1,480	1,390	mA
I_{CC4R}*	Operating burst read current; All banks open, Continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}max(I_{CC})$, $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{CC}4W		TBD	TBD	1,525	1,390	mA
I_{CC5B}**	Burst auto refresh current; $t_{CK} = t_{CK}(I_{CC})$; Refresh command at every $t_{RFC}(I_{CC})$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	TBD	1,160	1,660	mA
I_{CC6}**	Self refresh current; CK and CK\ at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	TBD	TBD	72	72	mA
I_{CC7}*	Operating bank interleave read current; All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = $t_{RC}D(I_{CC})$-1*$t_{CK}(I_{CC})$; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RRD} = t_{RRD}(I_{CC})$, t_{RCD} = 1*$t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.		TBD	TBD	2,380	2,380	mA

Note: I_{CC} specification is based on SAMSUNG components. Other DRAM Manufacturers specification may be different.

*: Value calculated as one module rank in this operating condition, and all other module ranks in I_{CC2P} (CKE LOW) mode.

**: Value calculated reflects all module ranks in this operating condition.

AC TIMING PARAMETERS & SPECIFICATIONS

AC CHARACTERISTICS				806		665		534		403		
PARAMETER			SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Clock	Clock cycle time	CL = 6	$t_{CK\ (6)}$	TBD	TBD							ps
		CL = 5	$t_{CK\ (5)}$	TBD	TBD	3,000	8,000					ps
		CL = 4	$t_{CK\ (4)}$	TBD	TBD	3,750	8,000	3,750	8,000	5,000	8,000	ps
		CL = 3	$t_{CK\ (3)}$	TBD	TBD	5,000	8,000	5,000	8,000	5,000	8,000	ps
	CK high-level width		t_{CH}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
	CK low-level width		t_{CL}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
	Half clock period		t_{HP}	TBD	TBD	$_{MIN}(t_{CH},t_{CL})$		$_{MIN}(t_{CH},t_{CL})$		$_{MIN}(t_{CH},t_{CL})$		ps
	Clock jitter		t_{JIT}	TBD	TBD	-125	125	-125	125	-125	125	ps
Data	DQ output access time from CK/CK#		t_{AC}	TBD	TBD	-450	+450	-500	+500	-600	+600	ps
	Data-out high-impedance window from CK/CK#		t_{HZ}	TBD	TBD		$t_{AC(MAX)}$		$t_{AC(MAX)}$		$t_{AC(MAX)}$	ps
	Data-out low-impedance window from CK/CK#		t_{LZ}	TBD	TBD	$t_{AC(MIN)}$	$t_{AC(MAX)}$	$t_{AC(MIN)}$	$t_{AC(MAX)}$	$t_{AC(MIN)}$	$t_{AC(MAX)}$	ps
	DQ and DM input setup time relative to DQS		t_{DS}	TBD	TBD	100		100		150		
	DQ and DM input hold time relative to DQS		t_{DH}	TBD	TBD	225		225		275		
	DQ and DM input pulse width (for each input)		t_{DIPW}	TBD	TBD	0.35		0.35		0.35		t_{CK}
	Data hold skew factor		t_{QHS}	TBD	TBD		340		400		450	ps
	DQ…DQS hold, DQS to first DQ to go nonvalid, per access		t_{QH}	TBD	TBD	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ps
	Data valid output window (DVW)		t_{DVW}	TBD	TBD	t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		ns
Data Strobe	DQS input high pulse width		t_{DQSH}	TBD	TBD	0.35		0.35		0.35		t_{CK}
	DQS input low pulse width		t_{DQSL}	TBD	TBD	0.35		0.35		0.35		t_{CK}
	DQS output access time from CK/CK#		t_{DQSCK}	TBD	TBD	-400	+400	-450	+450	-500	+500	ps
	DQS falling edge to CK rising … setup time		t_{DSS}	TBD	TBD	0.2		0.2		0.2		t_{CK}
	DQS falling edge from CK rising … hold time		t_{DSH}	TBD	TBD	0.2		0.2		0.2		t_{CK}
	DQS…DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}	TBD	TBD		240		300		350	ps
	DQS read preamble		t_{RPRE}	TBD	TBD	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
	DQS read postamble		t_{RPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
	DQS write preamble setup time		t_{WPRES}	TBD	TBD	0		0		0		ps
	DQS write preamble		t_{WPRE}	TBD	TBD	0.35		0.35		0.35		t_{CK}
	DQS write postamble		t_{WPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
	Write command to first DQS latching transition		t_{DQSS}	TBD	TBD	WL-0.25	WL+0.25	WL-0.25	WL+0.25	WL-0.25	WL+0.25	t_{CK}
	Address and control input pulse width for each input		t_{IPW}	TBD	TBD	0.6		0.6		0.6		t_{CK}
	Address and control input setup time		t_{IS}	TBD	TBD	200		250		250		ps
	Address and control input hold time		t_{IH}	TBD	TBD	275		375		475		ps
	Address and control input hold time		t_{CCD}	TBD	TBD	2		2		2		t_{CK}

* AC specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.

Continued on next page

AC TIMING PARAMETERS (cont'd)

AC CHARACTERISTICS			806		665		534		403		
	PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Command and Address	ACTIVE to ACTIVE (same bank) command	t_{RC}	TBD	TBD	55		55		55		ns
	ACTIVE bank a to ACTIVE bank b command	t_{RRD}	TBD	TBD	7.5		7.5		7.5		ns
	ACTIVE to READ or WRITE delay	t_{RCD}	TBD	TBD	15		15		15		ns
	Four Bank Activate period	t_{FAW}	TBD	TBD	37.5	37.5	37.5	37.5	37.5	37.5	ns
	ACTIVE to PRECHARGE command	t_{RAS}	TBD	TBD	40	70,000	40	70,000	40	70,000	ns
	Internal READ to precharge command delay	t_{RTP}	TBD	TBD	7.5		7.5		7.5		ns
	Write recovery time	t_{WR}	TBD	TBD	15		15		15		ns
	Auto precharge write recovery + precharge time	t_{DAL}	TBD	TBD	$t_{WR}+t_{RP}$		$t_{WR}+t_{RP}$		$t_{WR}+t_{RP}$		ns
	Internal WRITE to READ command delay	t_{WTR}	TBD	TBD	7.5		7.5		7.5		ns
	PRECHARGE command period	t_{RP}	TBD	TBD	15		15		15		ns
	PRECHARGE ALL command period	t_{RPA}	TBD	TBD	$t_{RP}+t_{CK}$		$t_{RP}+t_{CK}$		$t_{RP}+t_{CK}$		ns
	LOAD MODE command cycle time	t_{MRD}	TBD	TBD	2		2		2		t_{CK}
	CKE low to CK,CK# uncertainty	t_{DELAY}	TBD	TBD	$t_{IS}+t_{CK}$ t_{IH}		$t_{IS}+t_{CK}$ t_{IH}		$t_{IS}+t_{CK}$ t_{IH}		ns
Self Refresh	REFRESH to Active of Refresh to Refresh command interfal	t_{RFC}	TBD	TBD	127.5	70,000	127.5	70,000	127.5	70,000	ns
	Average periodic refresh interval	t_{REFI}	TBD	TBD		7.8		7.8		7.8	µs
	Exit self refresh to non-READ command	t_{XSNR}	TBD	TBD	$t_{RFC(MIN)}$ +10		$t_{RFC(MIN)}$ +10		$t_{RFC(MIN)}$ +10		ns
	Exit self refresh to READ command	t_{XSRD}	TBD	TBD	200		200		200		t_{CK}
	Exit self refresh timing reference	t_{ISXR}	TBD	TBD	t_{IS}		t_{IS}		t_{IS}		ps
ODT	ODT turn-on delay	t_{AOND}	TBD	TBD	2	2	2	2	2	2	t_{CK}
	ODT turn-on	t_{AON}	TBD	TBD	$t_{AC(MIN)}$	$t_{AC(MAX)}$ +1000	$t_{AC(MIN)}$	$t_{AC(MAX)}$ +1000	$t_{AC(MIN)}$	$t_{AC(MAX)}$ +1000	ps
	ODT turn-off delay	t_{AOFD}	TBD	TBD	2.5	2.5	2.5	2.5	2.5	2.5	t_{CK}
	ODT turn-off	t_{AOF}	TBD	TBD	$t_{AC(MIN)}$	$t_{AC(MAX)}$ +600	$t_{AC(MIN)}$	$t_{AC(MAX)}$ +600	$t_{AC(MIN)}$	$t_{AC(MAX)}$ +600	ps
	ODT turn-on (power-down mode)	t_{AONPD}	TBD	TBD	$t_{AC(MIN)}$ +2000	2 x t_{CK}+ $t_{AC(MAX)}$ +1000	$t_{AC(MIN)}$ +2000	2 x t_{CK}+ $t_{AC(MAX)}$ +1000	$t_{AC(MIN)}$ +2000	2 x t_{CK}+ $t_{AC(MAX)}$ +1000	ps
	ODT turn-off (power-down mode)	t_{AOFPD}	TBD	TBD	$t_{AC(MIN)}$ +2000	2.5 x t_{CK}+ $t_{AC(MAX)}$ +1000	$t_{AC(MIN)}$ +2000	2.5 x t_{CK}+ $t_{AC(MAX)}$ +1000	$t_{AC(MIN)}$ +2000	2.5 x t_{CK}+ $t_{AC(MAX)}$ +1000	ps
	ODT to power-down entry latency	t_{ANPD}	TBD	TBD	3		3		3		t_{CK}
	ODT power-down exit latency	t_{AXPD}	TBD	TBD	8		8		8		t_{CK}
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	TBD	TBD	2		2		2		t_{CK}
	Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	TBD	TBD	7-AL		6-AL		6-AL		t_{CK}
	A Exit precharge power-down to any non-READ command.	t_{XP}	TBD	TBD	2		2		2		t_{CK}
	CKE minimum high/low time	t_{CKE}	TBD	TBD	3		3		3		t_{CK}

* AC specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.

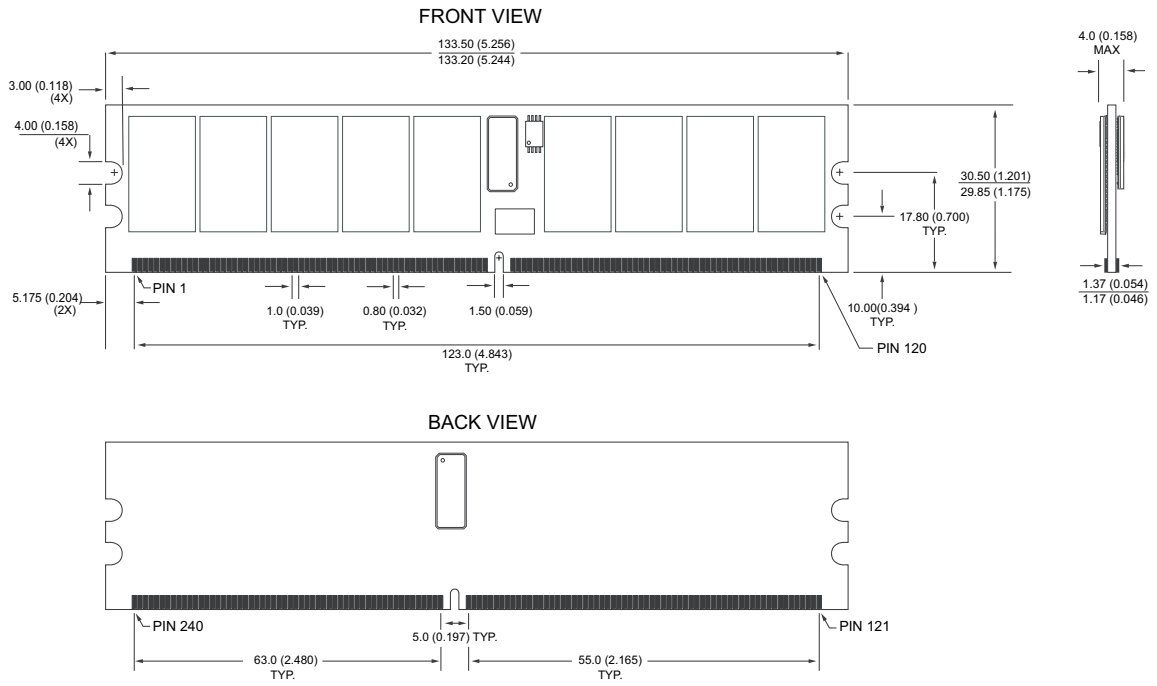
ORDERING INFORMATION FOR D6

Part Number	Speed	CAS Latency	t_{RCD}	t_{RP}	Height*
WV3HG64M72EER806D6	400MHz/800Mb/s	6	6	6	30.00mm (1.181") TYP
WV3HG64M72EER665D6	333MHz/667Mb/s	5	5	5	30.00mm (1.181") TYP
WV3HG64M72EER534D6	266MHz/533Mb/s	4	4	4	30.00mm (1.181") TYP
WV3HG64M72EER403D6	200MHz/400Mb/s	3	3	3	30.00mm (1.181") TYP

NOTES:

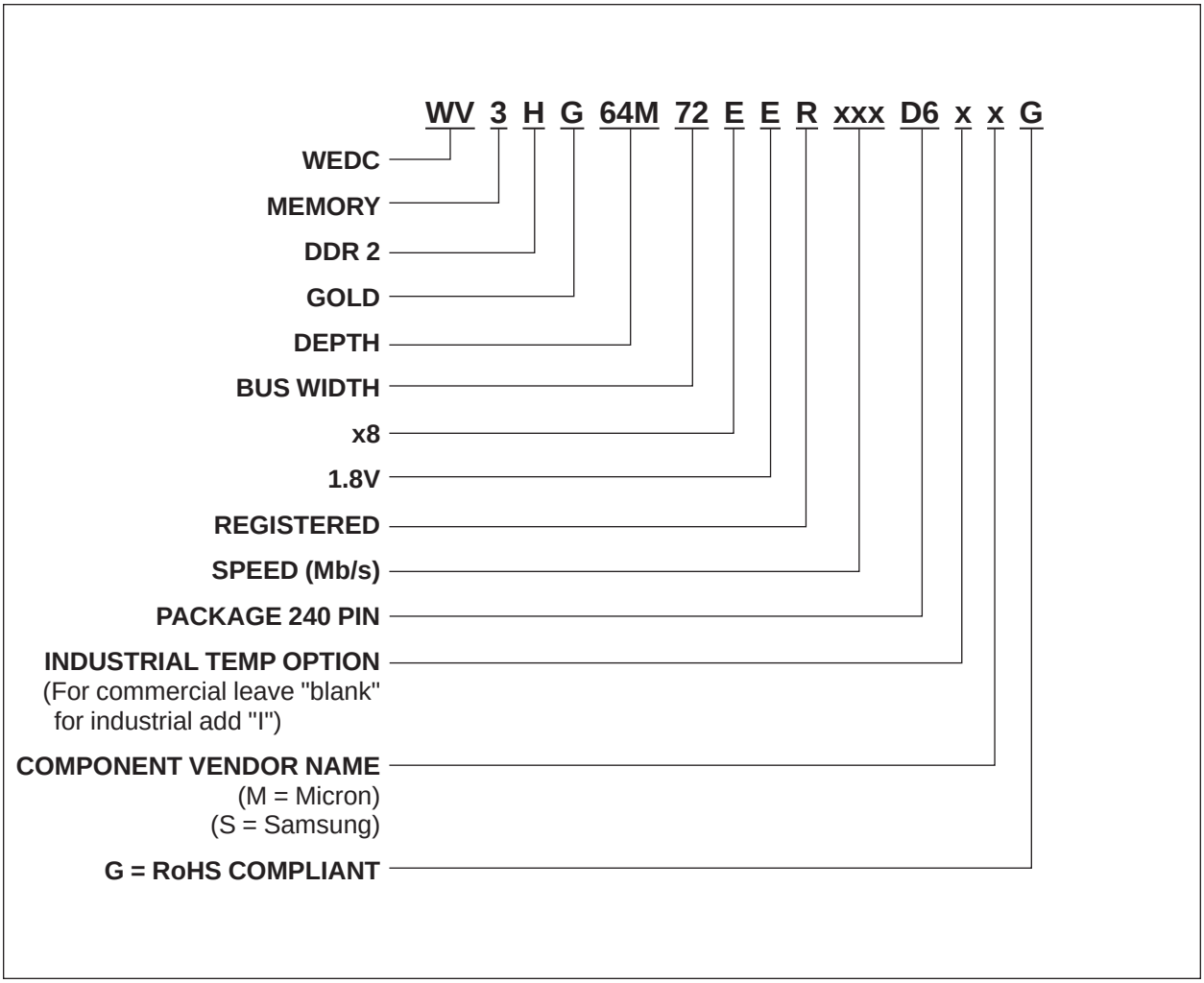
- RoHS products. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D6



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE



Document Title

512MB – 64Mx72 DDR2 SDRAM REGISTERED, w/PLL

DRAM DIE OPTIONS:

- SAMSUNG: C-Die, will move to E-Die Q2'06
- MICRON: U37: B-Die

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	August 2006	Concept
Rev 1	1.0 Moved to Advanced	August 14 2006	Advanced