Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
R _{ANA IN}	ANA IN Input Resistance	2.3	3	5	KΩ	
A _{PRE 1}	Preamp Gain 1	21	24	26	dB	AGC = 0.0 V
A _{PRE2}	Preamp Gain 2		-15	5	dB	AGC = 2.5 V
A _{AUX}	AUX IN/SP+ Gain		0,98	1.0	V/V	
A _{ARP}	ANA IN to SP+/- Gain	21	23	26	dB	
R _{AGC}	AGC Output Resistance	2,5	5	9.5	ΚΩ	

- **1.** Typical values @ $I_A = 25^{\circ}C$ and 5.0 V.
- 2. All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.
- **3.** V_{CCA} and V_{CCD} connected together.
- 4. XCLK pin only.

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteris	stic	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
F _S	Sampling Frequency	ISD2560 ISD2575 ISD2590 ISD25120		8.0 6.4 5.3 4.0		KHz KHz KHz KHz	(7) (7) (7) (7)
F _{CF}	Filter Pass Band	ISD2560 ISD2575 ISD2590 ISD25120		3.4 2.7 2.3 1.7		KHz KHz KHz KHz	3 dB Roll-Off Point (3) (8) 3 dB Roll-Off Point (3) (8) 3 dB Roll-Off Point (3) (8) 3 dB Roll-Off Point (3) (8)
T _{REC}	Record Duration	ISD2560 ISD2560 ISD2575 ISD2575 ISD2590 ISD25120	58.1 56.5 72.6 70.7 87.1 116.1	60.0 60.0 75.0 75.0 90.0	62.0 63.8 77.5 79.7 93.0 123.9	sec sec sec sec sec	Commercial Operation ⁽⁷⁾ Industrial Operation ⁽⁷⁾ Commercial Operation ⁽⁷⁾ Industrial Operation ⁽⁷⁾ Commercial Operation ⁽⁷⁾ Commercial Operation ⁽⁷⁾
T _{PLAY}	Playback Duration	ISD2560 ISD2560 ISD2575 ISD2575 ISD2590 ISD25120	58.1 56.5 72.6 70.7 87.1 116.1	60.0 60.0 75.0 75.0 90.0	62.0 63.8 77.5 79.7 93.0 123.9	sec sec sec sec sec	Commercial Operation Industrial Operation Commercial Operation Industrial Operation Commercial Operation Commercial Operation
T _{CE}	CE Pulse Width			100		nsec	
T _{SET}	Control/Address Setup Time			300		nsec	
T _{HOLD}	Control/Address Hole	d Time		0		nsec	

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteris	stic	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
T _{PUD}	Power-Up Delay	ISD2560 ISD2560 ISD2575 ISD2575 ISD2590 ISD25120	24.1 23.5 30.2 29.3 36.2 48.2	25.0 31.3 31.3 37.5 50.0	27.8 28.5 34.3 35.2 40.8 53.6	msec msec msec msec msec msec	Commercial Operation Industrial Operation Commercial Operation Industrial Operation Commercial Operation Commercial Operation
T _{PDR}	PD Pulse Width Record	ISD2560 ISD2575 ISD2590 ISD25120		25 31.25 37.5 50.0		msec msec msec msec	
T _{PDP}	PD Pulse Width Play	ISD2560 ISD2575 ISD2590 ISD25120		12.5 15.625 18.75 25.0		msec msec msec msec	
T _{PDS}	PD Pulse Width Static	:		100		nsec	(6)
T _{PDH}	Power Down Hold			0		nsec	
T _{EOM}	EOM Pulse Width	ISD2560 ISD2575 ISD2590 ISD25120		12.5 15.625 18.75 25.0		msec msec msec msec	
T _{OVF}	Overflow Pulse Width			6,5		μsec	
THD	Total Harmonic Disto	rtion		1	2	%	@ 1 KHz
P _{OUT}	Speaker Output Pow	er		12.2	50	mW	$R_{EXT} = 16 \Omega^{(4)}$
V _{OUT}	Voltage Across Spec	ıker Pins			2,5	V р-р	$R_{\text{EXT}} = 600 \Omega$
V _{IN1}	MIC Input Voltage				20	m۷	Peak-to-Peak ⁽⁵⁾
V _{IN2}	ANA IN Input Voltage)			50	m۷	Peak-to-Peak
V _{IN3}	Aux Input Voltage				1,25	V	Peak-to-Peak; $R_{\text{EXT}}=16~\Omega$

- **1.** Typical values @ $I_A = 25^{\circ}C$ and 5.0 V.
- 2. All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.
- 3. Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions).
- **4.** From AUX IN; if ANA IN is driven at 50 mV p-p, the $P_{OUT} = 12.2$ mW, typical.
- **5.** With 5.1 K Ω series resistor at ANA IN.
- **6.** T_{PDS} is required during a static condition, typically overflow.
- 7. Sampling Frequency and playback Duration can vary as much as ±2.25 percent over the commercial temperature range and voltage range and ±5 percent over the industrial temperature and voltage range. For greater stability, an external clock can be utilized (see Pin Descriptions).
- **8.** Filter specification applies to both the antialiasing filter and the smoothing filter. Therefore, from input to output, expect a 6 dB drop by nature of passing through both filters.

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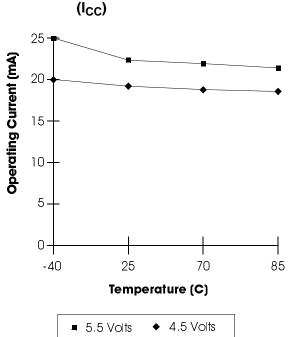
TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (PACKAGED PARTS)

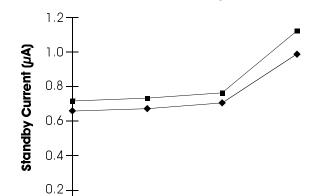
Chart 3:

0-

-40

Chart 1: Record Mode Operating Current





Standby Current (I_{SB})

■ 5.5 Volts ◆ 4.5 Volts

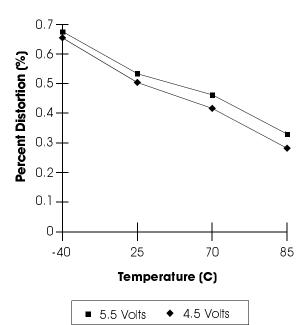
Temperature (C)

25

70

85

Chart 2: Total Harmonic Distortion





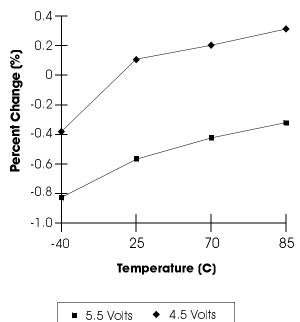


Table 8: Absolute Maximum Ratings (Die)⁽¹⁾

Condition	Value
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pad	$(V_{SS} - 0.3 \text{ V}) \text{ to}$ $(V_{CC} + 0.3 \text{ V})$
Voltage applied to any pad (Input current limited to ±20 mA)	$(V_{SS} - 1.0 \text{ V}) \text{ to}$ $(V_{CC} + 1.0 \text{ V})$
V _{CC} - V _{SS}	-0.3 V to +7.0 V

Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

Table 9: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range	0°C to +50°C
Supply voltage (V _{CC}) ⁽¹⁾	+4.5 V to +6.5 V
Ground voltage (V _{SS}) ⁽²⁾	0 V

- 1. $V_{CC} = V_{CCA} = V_{CCD}$.
- $2. \quad V_{SS} = V_{SSA} = V_{SSD}.$

Table 10: DC Parameters (Die)

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
V _{IL}	Input Low Voltage			0.8	٧	
V _{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 4.0 \text{ mA}$
V _{OH}	Output High Voltage	V _{CC} - 0.4			V	$I_{OH} = -10 \mu\text{A}$
V _{OH 1}	OVF Output High Voltage	2.4			V	$I_{OH} = -1.6 \text{ mA}$
V _{OH2}	EOM Output High Voltage	V _{CC} - 1,0	V _{CC} - 0.8		V	$I_{OH} = -3.2 \text{ mA}$
l _{CC}	V _{CC} Current (Operating)		25	30	mA	$R_{EXT} = \infty$ (3)
I _{SB}	V _{CC} Current (Standby)		1	10	μΑ	(2)
I _{IL}	Input Leakage Current			±1	μΑ	
I _{ILPD}	Input Current HIGH with Pull Down			130	μΑ	Force V _{CC} ⁽⁴⁾
R _{EXT}	Output Load Impedance	16			Ω	Speaker Load
R _{MIC}	Preamp In Input Resistance	4	9	15	ΚΩ	MIC and MIC REF Pads
R _{AUX}	AUX INput Resistance	5	11	20	ΚΩ	
R _{ANA IN}	ANA IN Input Resistance	2,3	3	5	ΚΩ	
A _{PRE1}	Preamp Gain 1	21	24	26	dB	AGC = 0.0 V

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Table 10: DC Parameters (Die)

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
A _{PRE2}	Preamp Gain 2		-15	5	dB	AGC = 2.5 V
A _{AUX}	AUX IN/SP+ Gain		0,98	1.0	V/V	
A _{ARP}	ANA IN to SP+/- Gain	21	23	26	dB	
R _{AGC}	AGC Output Resistance	2.5	5	9,5	ΚΩ	

- **1.** Typical values @ $T_A = 25^{\circ}C$ and 5.0 V.
- 2. All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.
- **3.** V_{CCA} and V_{CCD} connected together.
- 4. XCLK pad only.

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
F _S	Sampling Frequency	ISD2560 ISD2575 ISD2590 ISD25120		8.0 6.4 5.3 4.0		KHz KHz KHz KHz	(7) (7) (7) (7)
F _{CF}	Filter Pass Band	ISD2560 ISD2575 ISD2590 ISD25120		3.4 2.7 2.3 1.7		KHz KHz KHz KHz	3 dB Roll-Off Point (3) (8) 3 dB Roll-Off Point (3) (8) 3 dB Roll-Off Point (3) (8) 3 dB Roll-Off Point (3) (8)
T _{REC}	Record Duration	ISD2560 ISD2575 ISD2590 ISD25120	58.1 72.6 87.1 116.1	60.0 75.0 90.0 120.0	62.0 77.5 93.0 123.9	sec sec sec sec	Commercial Operation ⁽⁷⁾ Commercial Operation ⁽⁷⁾ Commercial Operation ⁽⁷⁾ Commercial Operation ⁽⁷⁾
T _{PLAY}	Playback Duration	ISD2560 ISD2575 ISD2590 ISD25120	58.1 72.6 87.1 116.1	60.0 75.0 90.0 120.0	62.0 77.5 93.0 123.9	sec sec sec sec	Commercial Operation ⁽⁷⁾ Commercial Operation ⁽⁷⁾ Commercial Operation ⁽⁷⁾ Commercial Operation ⁽⁷⁾
T _{CE}	CE Pulse Width			100		nsec	
T _{SET}	Control/Address Setu	up Time		300		nsec	
T _{HOLD}	Control/Address Hold Time			0		nsec	
T _{PUD}	Power-Up Delay	ISD2560 ISD2575 ISD2590 ISD25120	24.1 30.2 36.2 48.2	25.0 31.3 37.5 50.0	27.8 34.3 40.8 53.6	msec msec msec msec	Commercial Operation Commercial Operation Commercial Operation Commercial Operation

Table 11: AC Parameters (Die)

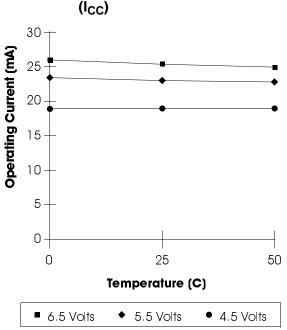
Symbol	Characteris	stic	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
T _{PDR}	PD Pulse Width Record	SD2560 SD2575 SD2590 SD25120		25 31.25 37.5 50.0		msec msec msec msec	
T _{PDP}	PD Pulse Width Play	ISD2560 ISD2575 ISD2590 ISD25120		12.5 15.625 18.75 25.0		msec msec msec msec	
T _{PDS}	PD Pulse Width Static			100		nsec	(6)
T _{PDH}	Power Down Hold			0		nsec	
T _{EOM}	EOM Pulse Width	ISD2560 ISD2575 ISD2590 ISD25120		12.5 15.625 18.75 25.0		msec msec msec msec	
T _{OVF}	Overflow Pulse Width			6,5		μsec	
THD	Total Harmonic Disto	rtion		1	3	%	@ 1 KHz
P _{OUT}	Speaker Output Pow	er er		12.2	50	mW	$R_{EXT} = 16 \Omega^{(4)}$
V _{OUT}	Voltage Across Spea	ker Pins			2.5	V p-p	$R_{EXT} = 600 \Omega$
V _{IN 1}	MIC Input Voltage				20	m۷	Peak-to-Peak ⁽⁵⁾
V _{IN2}	ANA IN Input Voltage	,			50	m۷	Peak-to-Peak
V _{IN3}	Aux Input Voltage				1,25	V	Peak-to-Peak; $R_{EXT}=16 \Omega$

- **1.** Typical values @ $I_A = 25$ °C and 5.0 V.
- 2. All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.
- 3. Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions).
- **4.** From AUX IN; if ANA IN is driven at 50 mV p-p, the $P_{OUI} = 12.2$ mW, typical.
- **5.** With 5.1 $K\Omega$ series resistor at ANA IN.
- **6.** T_{PDS} is required during a static condition, typically overflow.
- 7. Sampling Frequency and playback Duration can vary as much as ± 2.25 percent over the commercial temperature range and voltage range. For greater stability, an external clock can be utilized (see Pin Descriptions).
- 8. Filter specification applies to the antialiasing filter and the smoothing filter.

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TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (DIE)

Chart 5: Record Mode Operating Current (I_{CC})



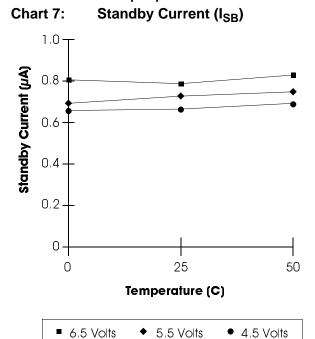
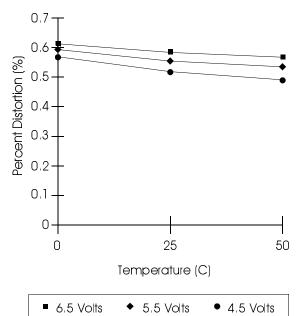
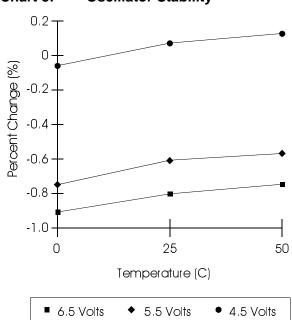


Chart 6: Total Harmonic Distortion







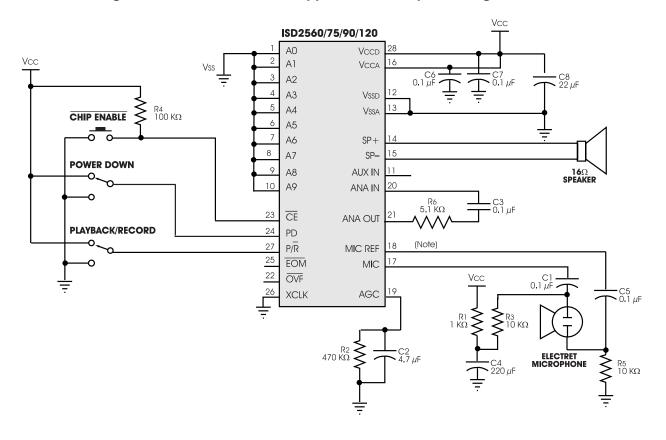


Figure 4: ISD2560/75/90/120 Application Example—Design Schematic

NOTE: If desired, pin 18 (PDIP package) may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 18 must not be tied to any other signal or voltage. Additional design example schematics are provided in the Application Notes in this book.

Table 12: Application Example—Basic Device Control

Control Step	Function	Action
1	Power up chip and select record/playback mode	(1.) PD = LOW, (2.) P/\overline{R} = As desired
2	Set message address for record/playback	Set addresses A0–A9
3A	Begin playback	$P/\overline{R} = HIGH$, $\overline{CE} = Pulsed LOW$
3B	Begin record	$P/R = LOW, \overline{CE} = LOW$
4A 4B	End playback End record	Automatic PD or $\overline{\text{CE}} = \text{HIGH}$

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Table 13: Application Example—Passive Component Functions

Part	Function	Comments
R1	Microphone power supply decoupling	Reduces power supply noise
R2	Release time constant	Sets release time for AGC
R3, R5	Microphone biasing resistors	Provides biasing for microphone operation
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages.
R6	Series limiting resistor	Reduces level to high supply voltages
C1, C5	Microphone DC-blocking capacitor Low-frequency cutoff	Decouples microphone bias from chip, Provides single- pole low-frequency cutoff and common mode noise rejection.
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff
C4	Microphone power supply decoupling	Reduces power supply noise
C6, C7, C8	Power supply capacitors	Filter and bypass of power supply

EXPLANATION

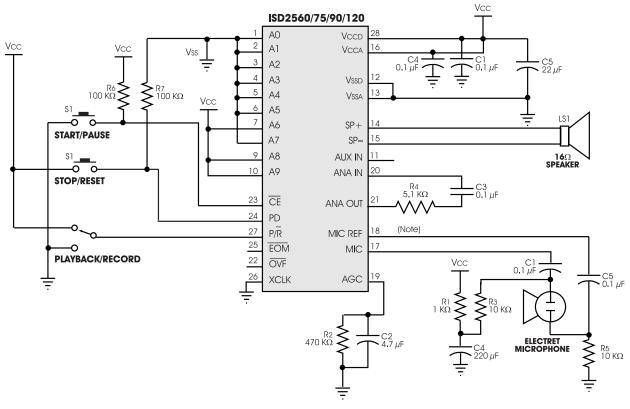
In this simplified block diagram of a microcontroller application, the Push-Button mode and message cueing are used. The microcontroller is a 16-pin version with enough port pins for buttons, an LED, and the ISD2500 series device. The software can be written to use three buttons: one each for play and record, and one for message selection. Because the microcontroller is interpreting the buttons and commanding the ISD2500 device, software can be written for any functions desired in a particular application.

NOTE ISD does not recommend connecting address lines directly to a microprocessor bus. Address lines should be externally latched.

D₁ RUN • RECORD Q PLAY o MSG# MC68HC705K1A ISD2560/75/90/120 OSC1 OSC2 $V_{\rm CCD}$ PB1 16 A1 V_{CCA} R₁ TBD RESET PAO Α2 IRQ PA1 АЗ V_{SSD} PA2 V_{SSA} U₁ PA3 Α5 SP+ V_{DD} PA4 Α6 15 U₂ PA5 SP-Α7 11 AUX IN Α8 PA6 V_{SS} 20 10 ANA IN Α9 PA7 CE ANA OUT 24 PD P/R MIC REF 17 EOM MIC 22 OVF 26 **XCLK** AGC

Figure 5: ISD2560/75/90/120 Application Example—Microcontroller/ISD2500 Interface

Figure 6: ISD2500 Application Example—Push-Button



NOTE: Please refer to Application Information.

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