APPLICATION NOTE
A V A I L A B L E
Application Brief

iAPX88/188, MCS 196, MCS51 Compatible*

64K X88064 8192 x 8 Bit

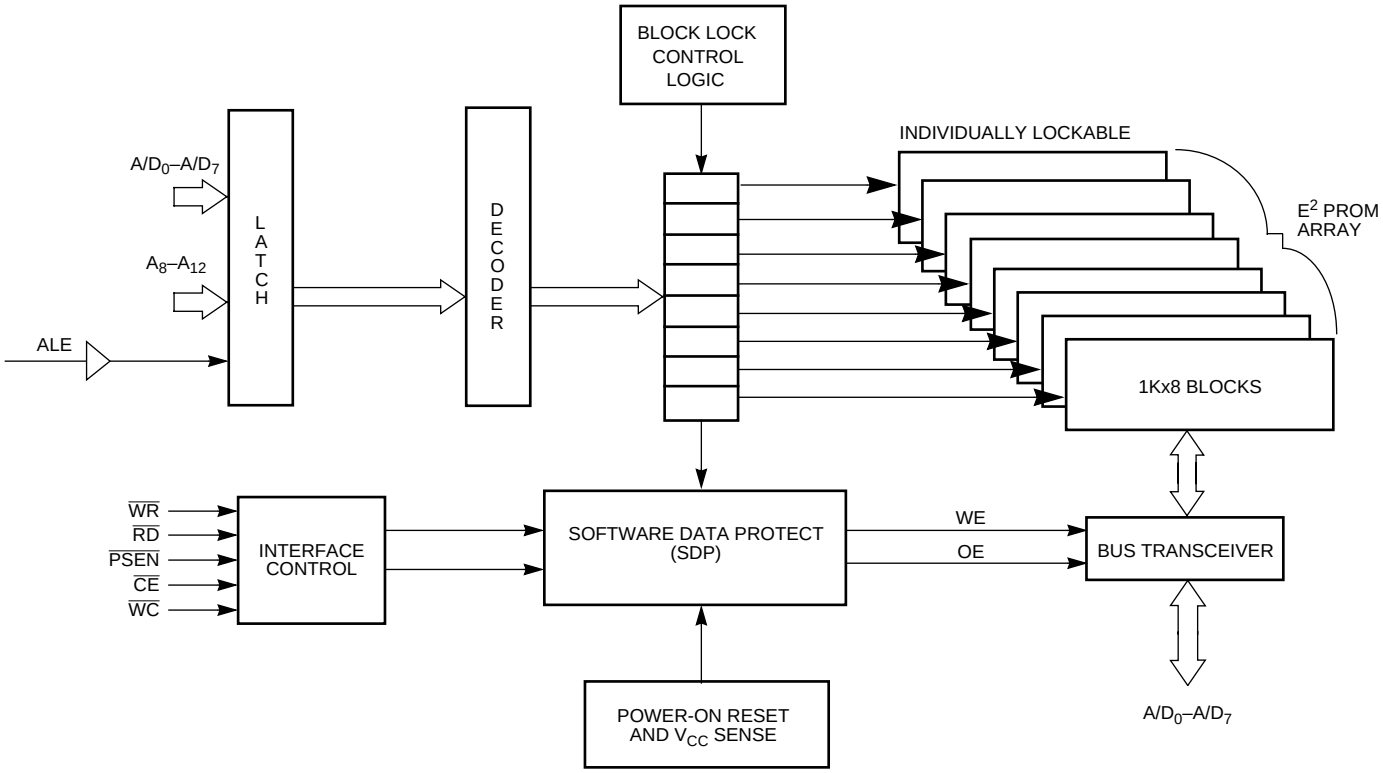
E^2 Microcontroller Peripheral

- **Block Lock Write Control**
  - **—Eight 1K Byte Blocks**
    - **Lockable Independently or in Combination**
- **Multiplexed Address/Data Bus**
  - **—Direct Interface to Popular Microcontrollers**
- **High Performance CMOS**
  - **—Fast Access Times, 60ns and 80 ns**
  - **—Low Power**
    - **30mA Active Maximum**
    - **150µA Standby Maximum**
- **Software Data Protection**
- **Toggle Bit Polling**
  - **—Early End of Write Detection**
- **Page Mode Write**
  - **—Allows up to 32 Bytes to be Written in One Write Cycle**

DESCRIPTION

The X88064 is a high speed byte wide microperipheral device with eight 1K byte blocks of E^2PROM and can be directly connected to industry standard high performance microprocessors. This peripheral provides two levels of memory write control, the standard Software Data Program (SDP) control and Block Lock.

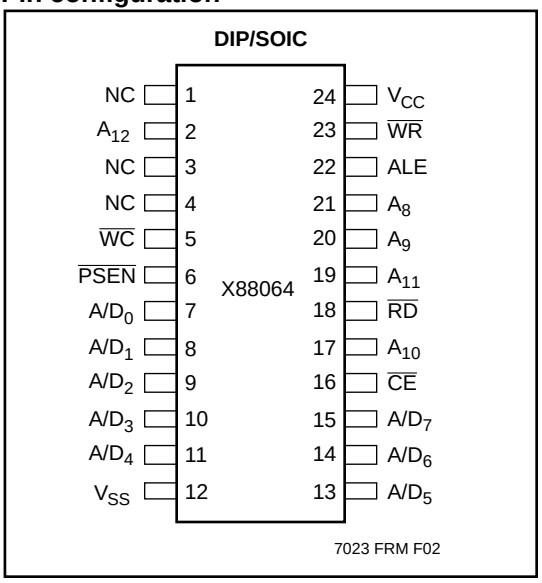
Block Lock provides a higher level of memory write control above SDP. This allows the software developer to partition any or all of the eight 1K byte blocks as In-Circuit Programmable ROM (ICPROM). Once locked, a block of memory must first be unlocked before being written. Not even a write operation using the SDP sequence will change the contents of a locked block. Since a distinct, 6 byte, software command sequence locks and unlocks the memory, the software developer has complete control of the memory contents.



7023-2.3 1/29/97 T0/C2/D0 SH

Software Data Program Control provides a lower level of memory write management. SDP controls write operations to the entire memory. When enabled, the host microprocessor must send a special 3 byte command sequence before any byte or page writes to unlocked locations in the memory.

Pin configuration



PIN NAMES

PIN NAME	I/O	DESCRIPTION
$\overline{PSEN}$	I	Content of E^2 memory can be read by lowering the $\overline{PSEN}$ and holding both $\overline{RD}$ and $\overline{WR}$ HIGH. The device then places on the data bus (AD_0–AD_7) the contents of E^2 memory at the latched address.
A_8–A_{12}	I	Non-multiplexed high-order Address Bus inputs for the upper byte of the address.
AD_0–AD_7	I/O	Multiplexed low-order Address and Data Bus. The addresses are latched when ALE makes a HIGH to LOW transition.
$\overline{WR}$	I	During a byte/page write cycle $\overline{WR}$ is brought LOW while $\overline{RD}$ is held HIGH and the data is placed on the bus. The rising edge of $\overline{WR}$ latches data into the device.
$\overline{RD}$	I	The $\overline{RD}$ input is active LOW and is used to read content of the E^2 memory at the latched address. Both $\overline{PSEN}$ an $\overline{WR}$ signals must be held HIGH during $\overline{RD}$ controlled read operation.
$\overline{WC}$	I	$\overline{WC}$ input has to be held LOW during a write cycle. It can be permanently tied HIGH in order to disable write to the E^2 memory. Taking $\overline{WC}$ HIGH prior to t_{BLC} (100ns, the time delay from the last write cycle to the start of internal programming cycle) will inhibit the write operation.
$\overline{CE}$	I	The device select ($\overline{CE}$) is an active LOW input. This signal has to be asserted prior to ALE HIGH to LOW transition in order to generate a valid internal device select signal. Holding this pin HIGH and ALE LOW will place the device in standby mode.
ALE	I	Address Latch Enable input is used to latch the addresses present on the address lines A_8–A_{12} and AD_0–AD_7 into the device. The addresses are latched when ALE transitions from HIGH to LOW.

PRINCIPLES OF OPERATION

The X88064 is a highly integrated peripheral device for a wide variety of single-chip microcontrollers. The X88064 provides 8K bytes of E²PROM which can be used either for Program Storage, Data Storage, or a combination of both, in systems based upon Harvard (80XX) architectures. The X88064 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the Address/Data bus to provide a "Seamless" interface.

The interface inputs on the X88064 are configured such that it is possible to directly connect them to the proper interface signals of the appropriate single-chip microcontroller. In the Harvard type system, the reading of data from the chip is controlled either by the $\overline{PSEN}$ or the $\overline{RD}$ signal, which essentially maps the X88064 into both the Program and the Data Memory address map.

The X88064 also features an advanced implementation of the Software Data Protection scheme, called Block Lock, which allows the device to be broken into 8 independent sections of 1K bytes. Each of these sections can be independently enabled for write operations; thereby allowing certain sections of the device to be secured so that updates can only occur in a controlled environment (e.g. in an automotive application, only at an authorized service center). The desired set-up configuration is stored in a nonvolatile register, ensuring the configuration data will be maintained after the device is powered down.

The X88064 also features a Write Control input ($\overline{WC}$), which serves as an external control over the completion of a previously initiated page load cycle.

The X88064 also features the industry standard E²PROM characteristics such as byte or page mode write and Toggle Bit Polling.

DEVICE OPERATION MODES

Mixed Program/Data Memory

By properly assigning the address space, a single X88064 can be used as both the Program and Data Memory. This would be accomplished by connecting all of the Microcontroller control outputs to the corresponding inputs of the X88064.

The Data Storage can be fully protected by enabling Block Lock Control.

Program Memory Mode

This mode of operation is read-only. The $\overline{PSEN}$ and $\overline{ALE}$ inputs of the X88064 are tied directly to the $\overline{PSEN}$ and ALE outputs of the microcontroller. The $\overline{RD}$ and $\overline{WR}$ inputs are tied HIGH.

When ALE is HIGH, the A/D_0–A/D_7 and A_8–A_{12} addresses flow into the device. The addresses, both low and high order, are latched when ALE transitions LOW (V_{IL}). $\overline{PSEN}$ will then go LOW and after t_{PLDV}, valid data is presented on the A/D_0–A/D_7 pins. $\overline{CE}$ must be LOW during the entire operation.

Data Memory Mode

This mode of operation allows both read and write functions. The $\overline{PSEN}$ input is tied to V_{IH} or to V_{CC} through a pull-up resistor. The ALE, $\overline{RD}$, and $\overline{WR}$ inputs are tied directly to the microcontroller's ALE, $\overline{RD}$, and $\overline{WR}$ outputs.

Read

This operation is quite similar to the Program Memory read. A HIGH to LOW transition on ALE latches the addresses and the data will be output on the A/D pins after $\overline{RD}$ goes LOW (t_{RLDV}).

Write

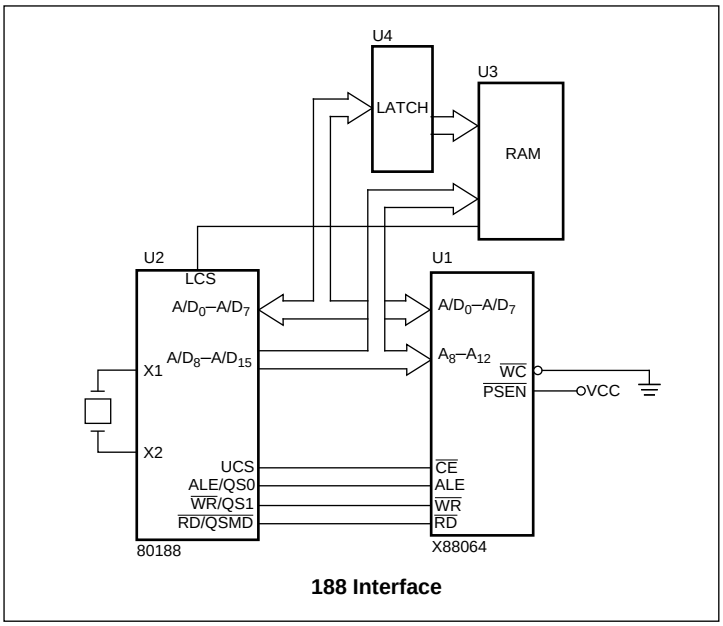
A write is performed by latching the addresses on the falling edge of ALE. Then $\overline{WR}$ is strobed LOW followed by valid data being presented at the A/D_0–A/D_7 pins. The data will be latched into the X88064 on the rising edge of $\overline{WR}$. To write to the X88064, with the SDP feature enabled, a three-byte command sequence must precede the byte(s) being written. (See Software Data Protection.)

MODE SELECTION

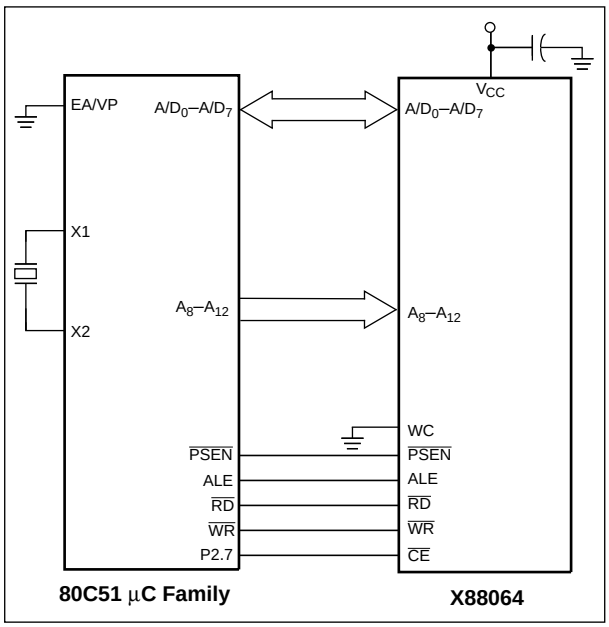
$\overline{CE}$	$\overline{PSEN}$	$\overline{RD}$	$\overline{WR}$	Mode	I/O	Power
V_{CC}	X	X	X	Standby	High Z	Standby (CMOS)
HIGH	X	X	X	Standby	High Z	Standby (TTL)
LOW	LOW	HIGH	HIGH	Program Fetch	D_{OUT}	Active
LOW	HIGH	LOW	HIGH	Data Read	D_{OUT}	Active
LOW	HIGH	HIGH	⎍	Write	D_{IN}	Active

7023 FRM T02

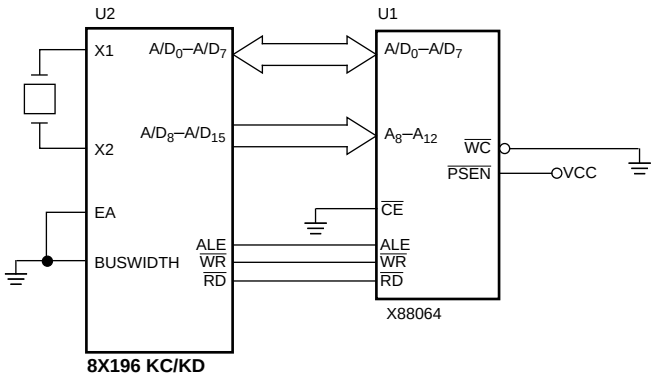
TYPICAL APPLICATIONS



188 Interface



80C51 µC Family **X88064**



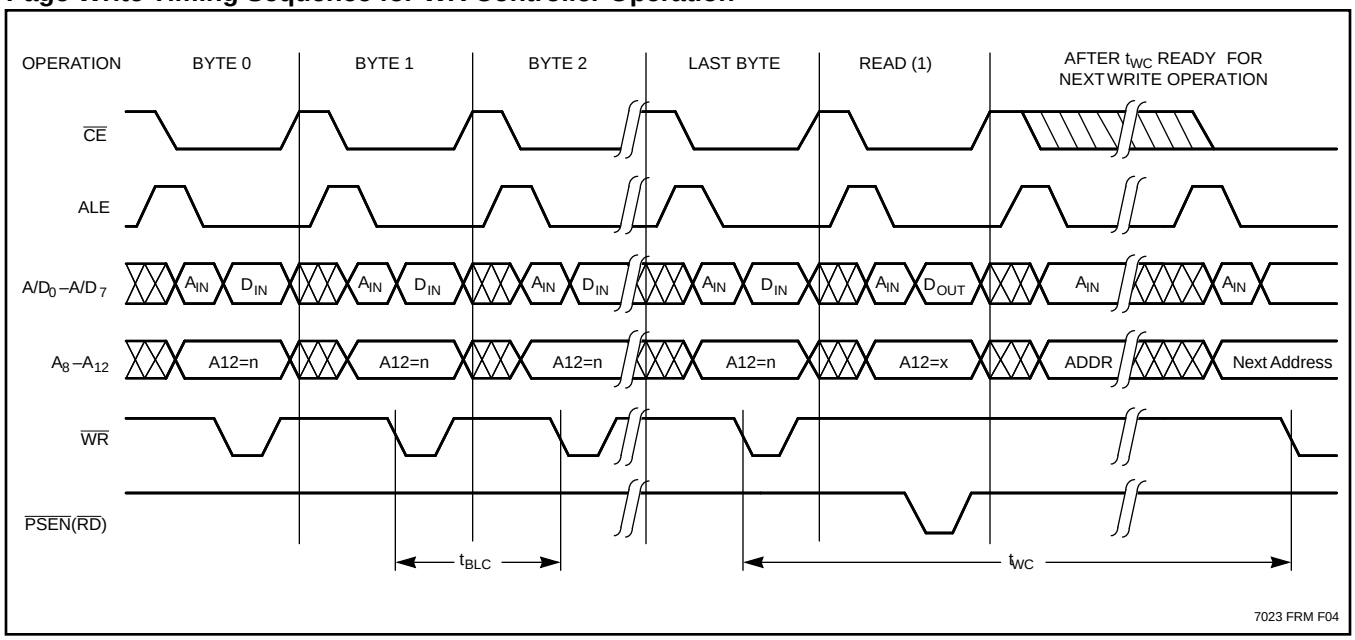
196 Interface

7023 FRM F03

PAGE WRITE OPERATION

Regardless of the microcontroller employed, the X88064 supports page mode write operations. This allows the microcontroller to write from one to thirty-two bytes of data to the X88064. Each individual write within a page write operation must conform to the byte write timing requirements. The falling edge of $\overline{WR}$ starts a timer delaying the internal programming cycle 100µs. Therefore, each successive write operation must begin within 100µs of the last byte written. The following waveforms illustrate the sequence and timing requirements.

Page Write Timing Sequence for $\overline{WR}$ Controller Operation

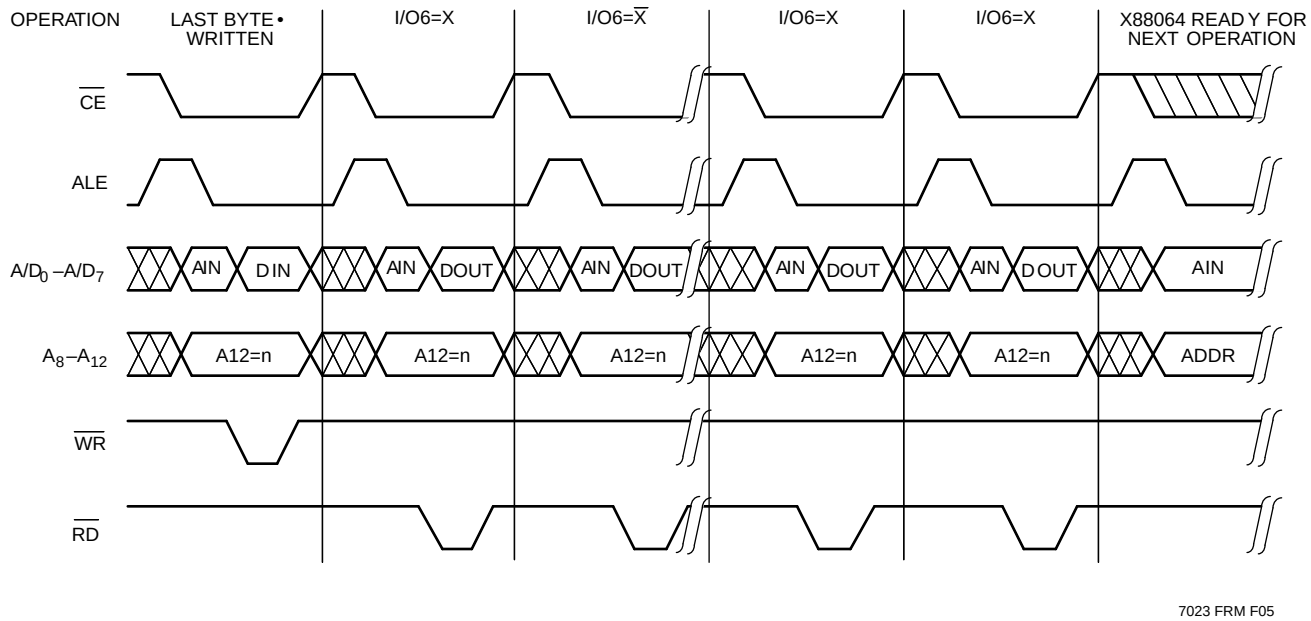


Notes: (1) For each successive write within a page write cycle $A_5–A_{12}$ must be the same.

TOGGLE BIT POLLING

Because the X88064 typical nonvolatile write cycle time is less than the specified 5ms, Toggle Bit Polling has been provided to determine the early completion of write. During the internal programming cycle I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete, the toggling will cease and the device will be accessible for additional read or write operations.

Toggle Bit Polling RD/WR Control



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

DATA PROTECTION

The X88064 provides two levels of data protection through software control. There is a global software data protection feature similar to the industry standard for E²PROMs and a new Block Lock Control providing a secondary level of data security.

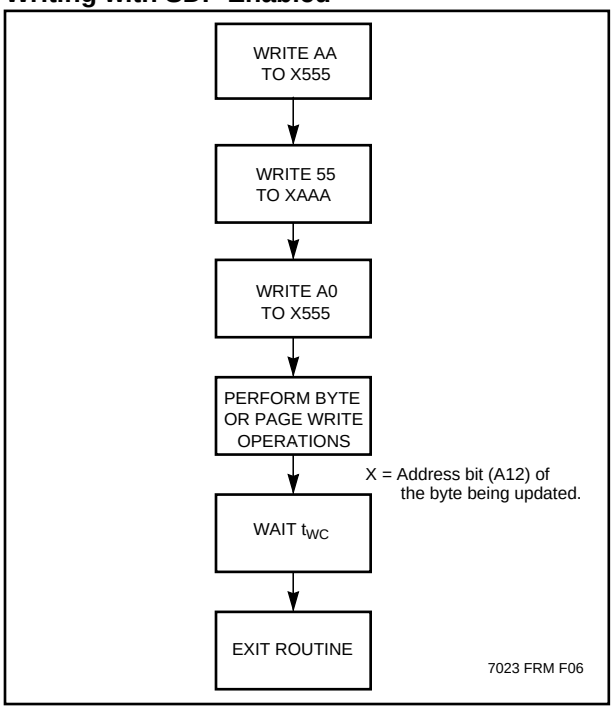
SOFTWARE DATA PROTECTION

The X88064 offers a software controlled data protection feature. The X88064 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/down operations through the use of external circuits. The host then has open read and write access of the device once V_{CC} is stable.

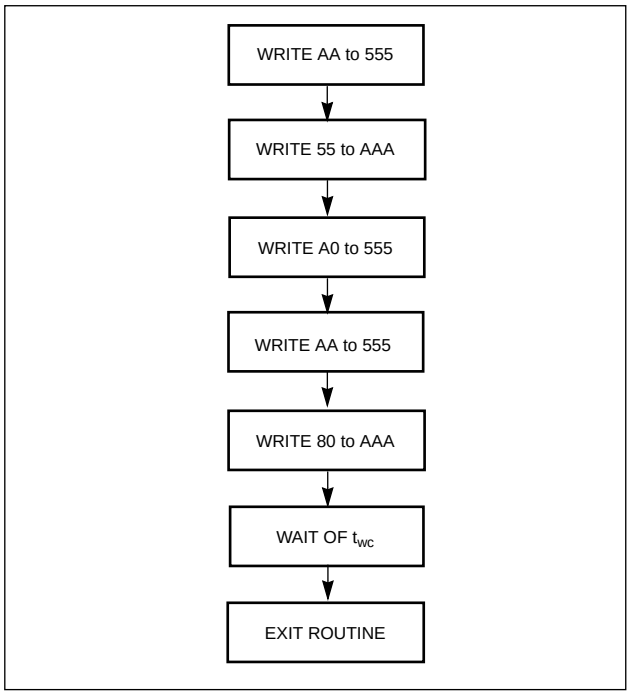
The X88064 can be automatically protected during power-up/down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the SDP deactivation command is issued.

Once the software protection is enabled, the X88064 is also protected from inadvertent and accidental writes in the powered-up state. That is, the SDP software algorithm must be issued prior to writing additional data to the device.

Writing with SDP Enabled



SEQUENCE TO DEACTIVATE SOFTWARE DATA PROTECTION

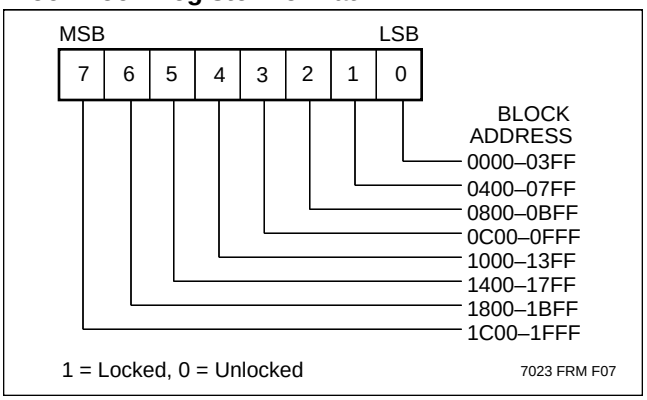


Block Lock Write Control

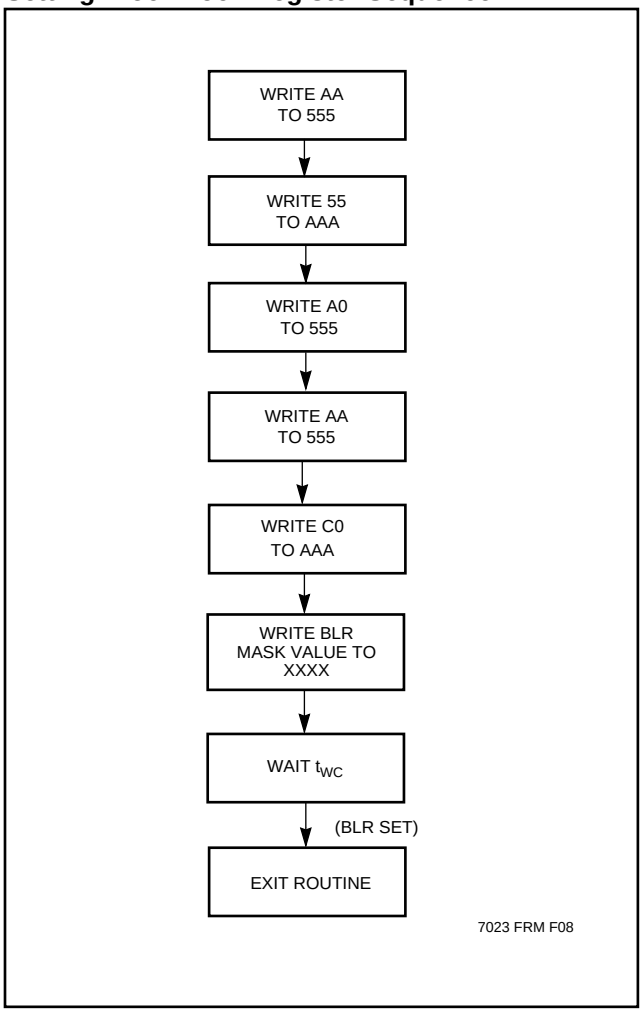
The X88064 provides a secondary level of data security referred to as Block Lock Control. This is accessed through an extension of the SDP command sequence. Block Lock allows the user to inhibit writes to any 1K x 8 blocks of memory. Unlike SDP which prevents inadvertent writes, but still allows easy system access to writing the memory, Block Lock will inhibit all attempts unless it is specifically disabled by the host. This could be used to set a higher level of protection in a system where a portion of the memory is used for Program Storage and another portion is used as Data Storage.

Setting write lockout is accomplished by writing a five-byte command sequence, opening access to the Block Lock Register (BLR). After the fifth byte is written, the user writes to the BLR, selecting which blocks to protect or unprotect. All write operations, both the command sequence and writing the data to the BLR, must conform to the page write timing requirements.

Block Lock Register Format



Setting Block Lock Register Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias.....–65°C to +135°C
Storage Temperature .....–65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current.....5 mA
Lead Temperature
(Soldering, 10 seconds)300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

7023 FRM T03

Supply Voltage	Limits
X88064	5V ±10%
X88064-60	5V ±10%

7023 FRM T04

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I_{CC}	V_{CC} Current (Active)		30	mA	$\overline{CE}$ = $\overline{RD}$ = V_{IL}, All I/O's = Open, Other Inputs = V_{CC}
$I_{SB1(CMOS)}$	V_{CC} Current (Standby)		150	µA	$\overline{CE}$ = V_{CC} – 0.3V, All I/O's = Open, Other Inputs = V_{CC} – 0.3V, ALE = V_{IL}
$I_{SB2(TTL)}$	V_{CC} Current (Standby)		2.5	mA	$\overline{CE}$ = V_{IH}, All I/O's = Open, Other Inputs = V_{IH}, ALE = V_{IL}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{RD}$ = V_{IH} = $\overline{PSEN}$
V_{IL}(3)	Input LOW Voltage	–1	0.8	V	
V_{IH}(3)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –400 µA

7023 FRM T05

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance	6	pF	V_{IN} = 0V

7023 FRM T06

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(4)	Power-Up to Read	1	ms
t_{PUW}(4)	Power-Up to Write	5	ms

7032 FRM T07

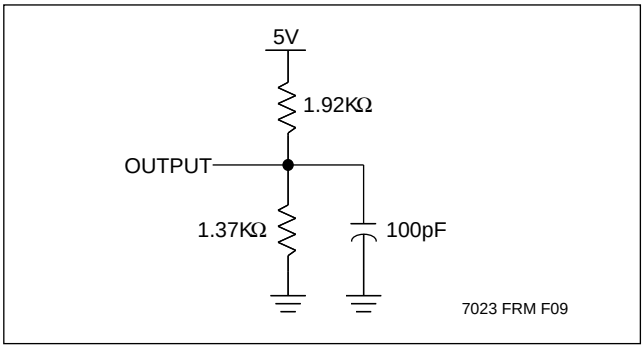
Notes: (3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

7023 FRM T08

EQUIVALENT A.C. TEST CIRCUIT

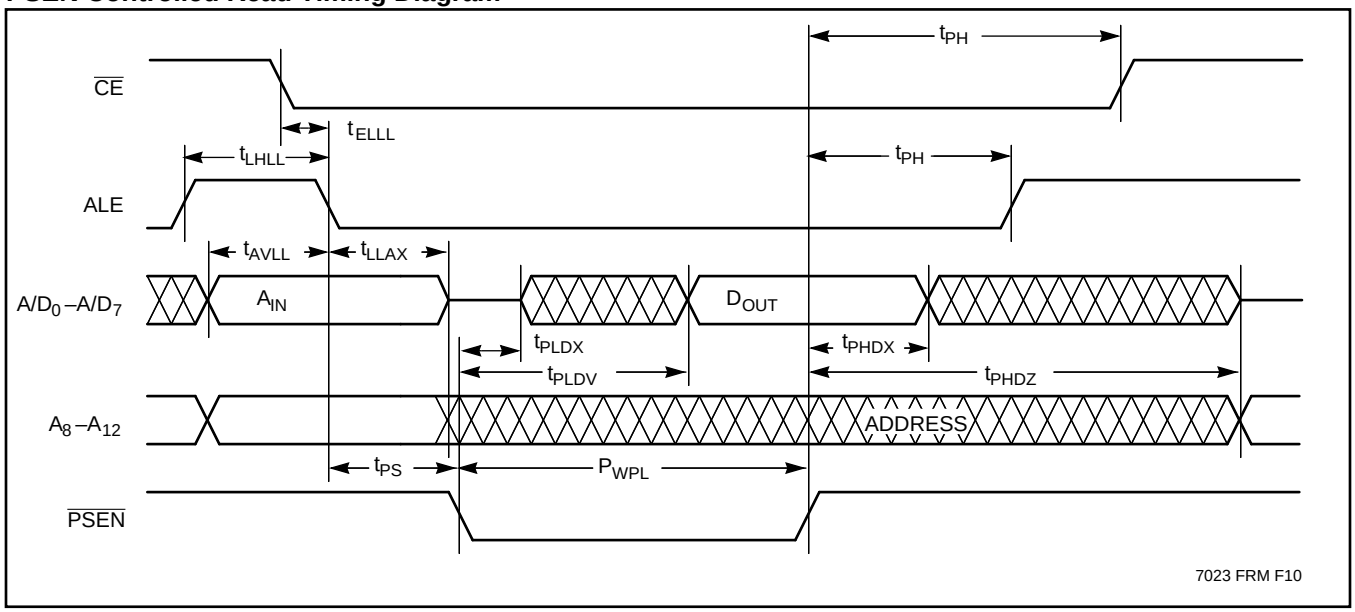


$\overline{PSEN}$ Controlled Read Cycle

Symbol	Parameter	X88064 – 60		X88064		Units
		Min.	Max.	Min.	Max.	
t_{LHLL}	ALE Pulse Width	60		80		ns
t_{AVLL}	Address Setup Time	10		10		ns
t_{LLAX}	Address Hold Time	20		20		ns
t_{PLDV}	$\overline{PSEN}$ Read Access Time		45		80	ns
t_{PHDX}	Data Hold Time	0		0		ns
t_{ELLL}	Chip Enable Setup Time	7		7		ns
PW_{PL}	$\overline{PSEN}$ Pulse Width	100		140		ns
t_{PS}	$\overline{PSEN}$ Setup Time	20		30		ns
t_{PH}	$\overline{PSEN}$ Hold Time	20		20		ns
t_{PHDZ} (5)	$\overline{PSEN}$ Disable to Output in High Z		20		30	ns
t_{PLDX} (5)	$\overline{PSEN}$ to Output in Low Z	10		10		ns

7023 FRM T09

$\overline{PSEN}$ Controlled Read Timing Diagram

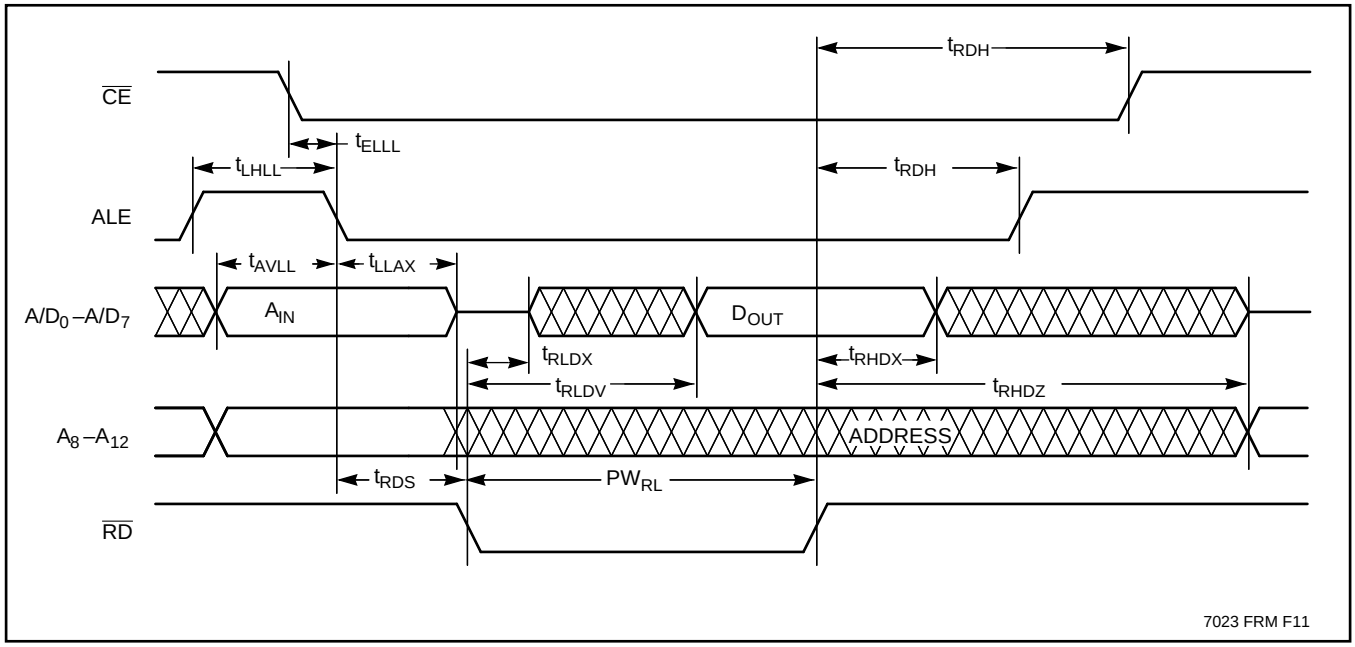


$\overline{RD}$ Controlled Read Cycle

Symbol	Parameter	X88064 – 60		X88064		Units
		Min.	Max.	Min.	Max.	
t_{LHLL}	ALE Pulse Width	60		80		ns
t_{AVLL}	Address Setup Time	10		10		ns
t_{LLAX}	Address Hold Time	20		20		ns
t_{RLDV}	$\overline{RD}$ Read Access Time		60		80	ns
t_{RHDX}	Data Hold Time	0		0		ns
t_{ELLL}	Chip Enable Setup Time	7		7		ns
PW_{RL}	$\overline{RD}$ Pulse Width	120		150		ns
t_{RDS}	$\overline{RD}$ Setup Time	20		30		ns
t_{RDH}	$\overline{RD}$ Hold Time	20		20		ns
t_{RHDZ} (6)	$\overline{RD}$ Disable to Output in High Z		20		30	ns
t_{RLDX} (6)	$\overline{RD}$ to Output in Low Z	0		0		ns

7023 FRM T10

$\overline{RD}$ Controlled Read Timing Diagram



7023 FRM F11

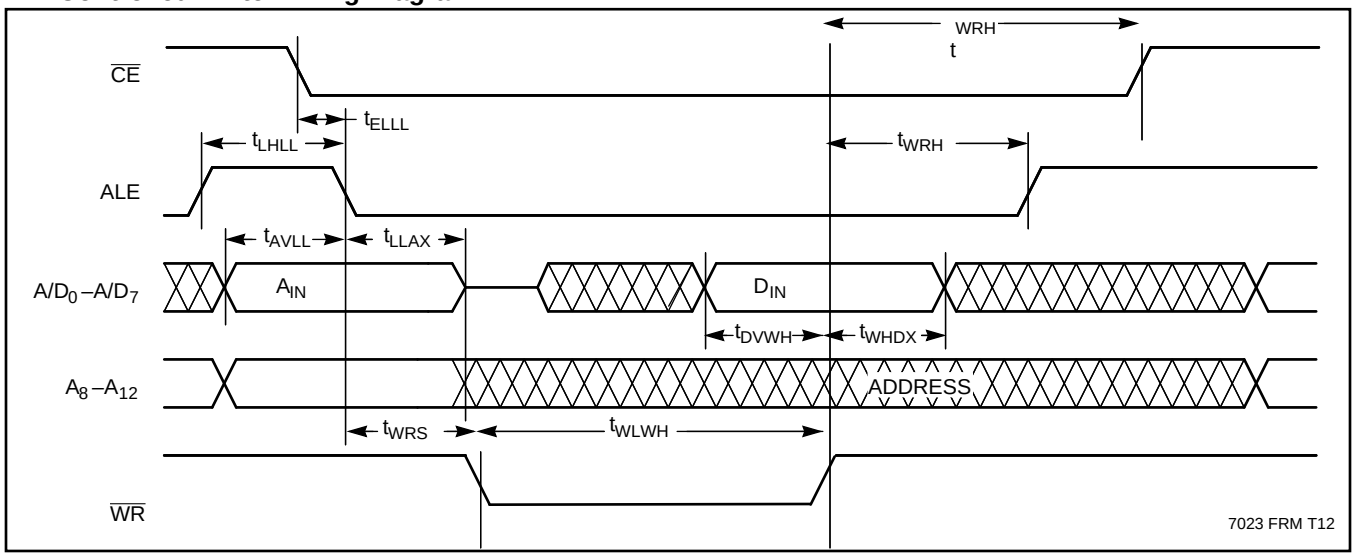
Notes: (6) This parameter is periodically sampled and not 100% tested.

$\overline{WR}$ Controlled Write Cycle

Symbol	Parameter	X88064 – 60		X88064		Units
		Min.	Max.	Min.	Max.	
t_{LHLL}	ALE Pulse Width	60		80		ns
t_{AVLL}	Address Setup Time	10		10		ns
t_{LLAX}	Address Hold Time	20		20		ns
t_{DVWH}	Data Setup Time	50		50		ns
t_{WHDX}	Data Hold Time	30		30		ns
t_{ELLL}	Chip Enable Setup Time	7		7		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	100		120		ns
t_{WRS}	$\overline{WR}$ Setup Time	20		30		ns
t_{WRH}	$\overline{WR}$ Hold Time	20		20		ns
t_{BLC}	Byte Load Time (Page Write)	0.5	100	0.5	100	µs
t_{WC} (7)	Write Cycle Time		5		5	ms

7023 FRM T11

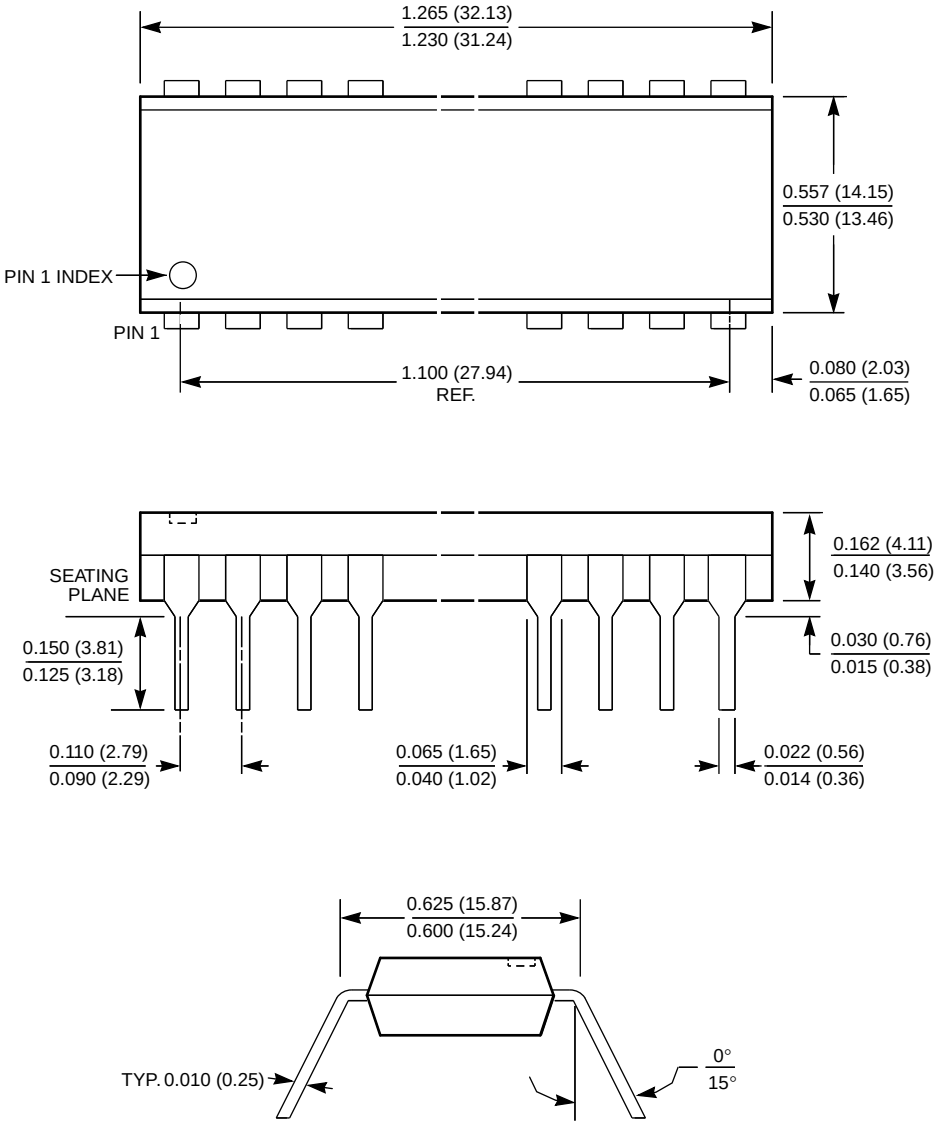
$\overline{WR}$ Controlled Write Timing Diagram



Notes: (7) TWC is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

PACKAGING INFORMATION

24-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

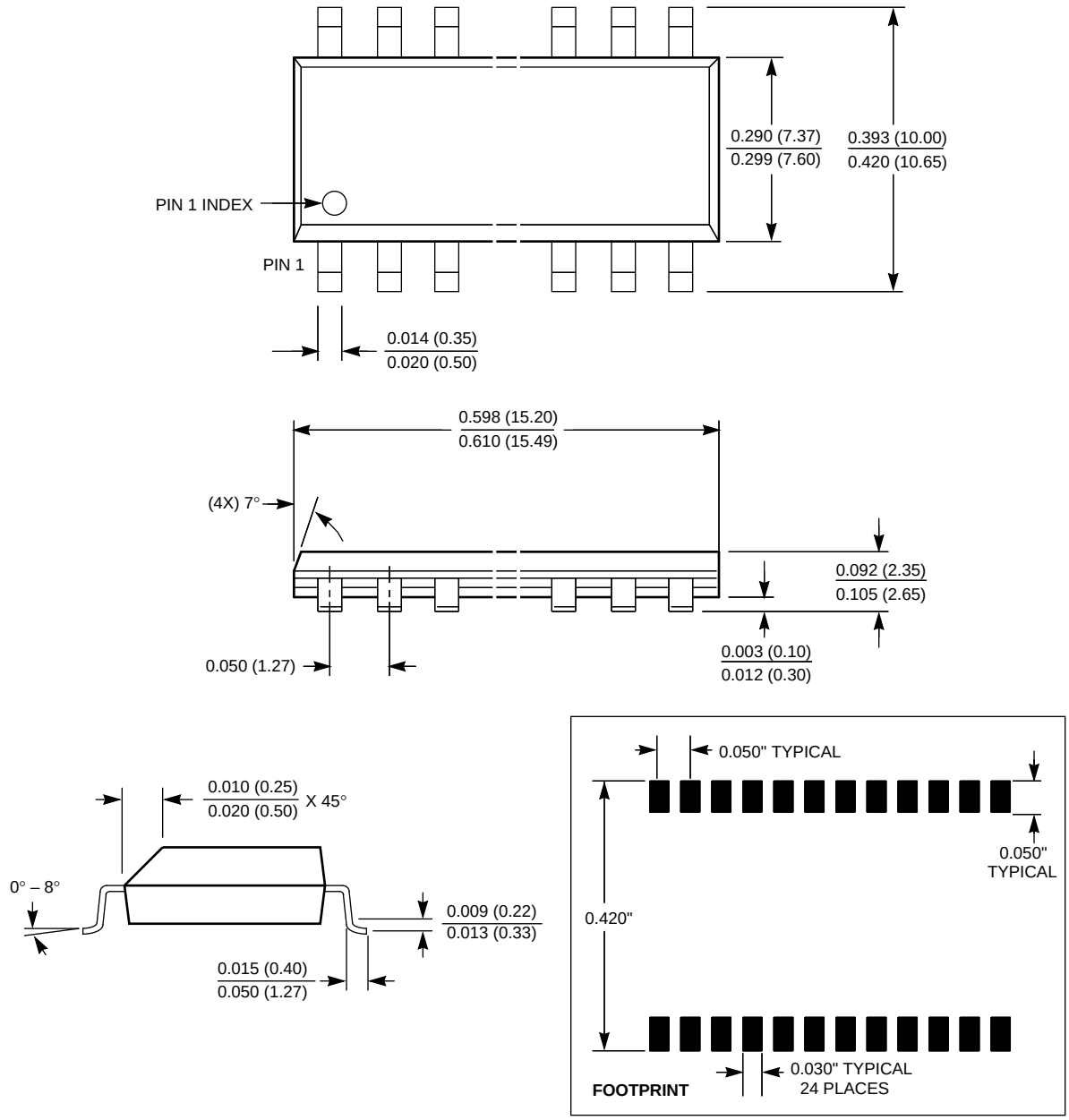


NOTE:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

7023 FRM F13

PACKAGING INFORMATION

24-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

7023 FRM F14

ORDERING INFORMATION