ZL40800 and ZL40802

6 GHz Fixed Modulus Prescalers ÷ 8 and ÷ 16

Data Sheet

July 2003

Features

- 3.45V Single Supply Operation
- Low Power Dissipation: 190mW typ
- Broadband: DC to 6GHz
- SSB Phase Noise (–153dBc/Hz @ 10KHz)
- Pout 3dBm

Prescaler Modulus

- ZL40800 – Divide by 8
- ZL40802 – Divide by 16

Applications

- DC to 6 GHz PLL applications
- HyperLan
- LMDS
- Instrumentation
- Satellite Communications
- Fibre Optic Communications; OC48, OC192
- Ultra Low Jitter Clock Systems

Ordering Information

ZL40800/DCA (tubes)	8 pin SOIC
ZL40800/DCB (tape and reel)	8 pin SOIC
ZL40802/DCA (tubes)	8 pin SOIC
ZL40802/DCB (tape and reel)	8 pin SOIC

-40°C to 85°C

Description

The ZL40800 and ZL40802 are Bipolar 3.45V supply, very low power prescalers for professional applications with a fixed modulus of 8 or 16. The ultra low close in (1KHz offset) SSB phase noise performance is ideal for narrow band communications systems or systems with ultra low jitter budgets such as next generation fibre optic communications. The devices are broadband from DC to 6GHz.

See Figure 1 and Application Note for RF Prescalers for more details.

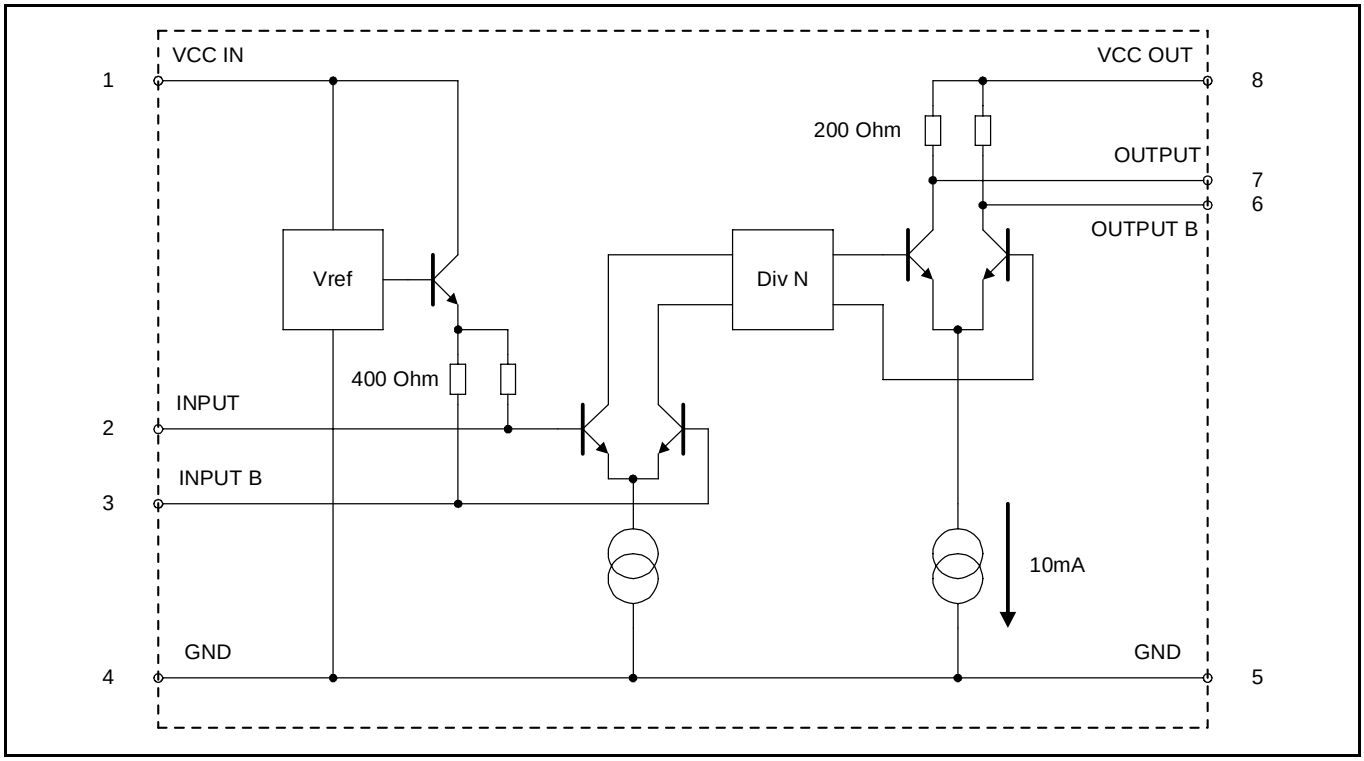


Figure 1 - Block Diagram

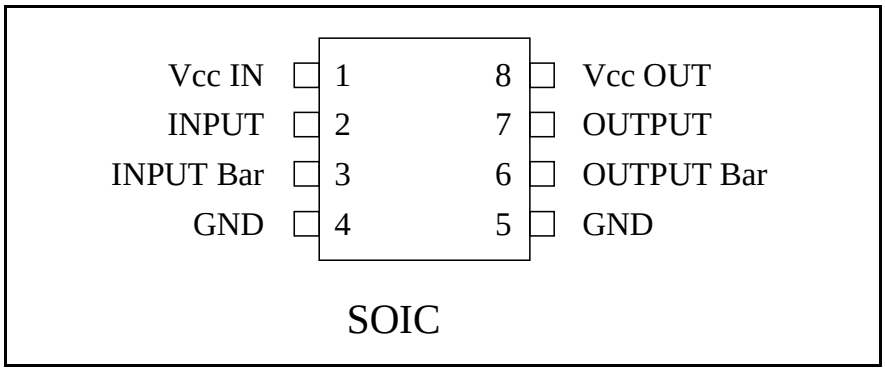


Figure 2 - Pin Connections - Top View

Application Configuration

Figure 3 shows a recommended application configuration. This example shows the device set up for single ended operation.

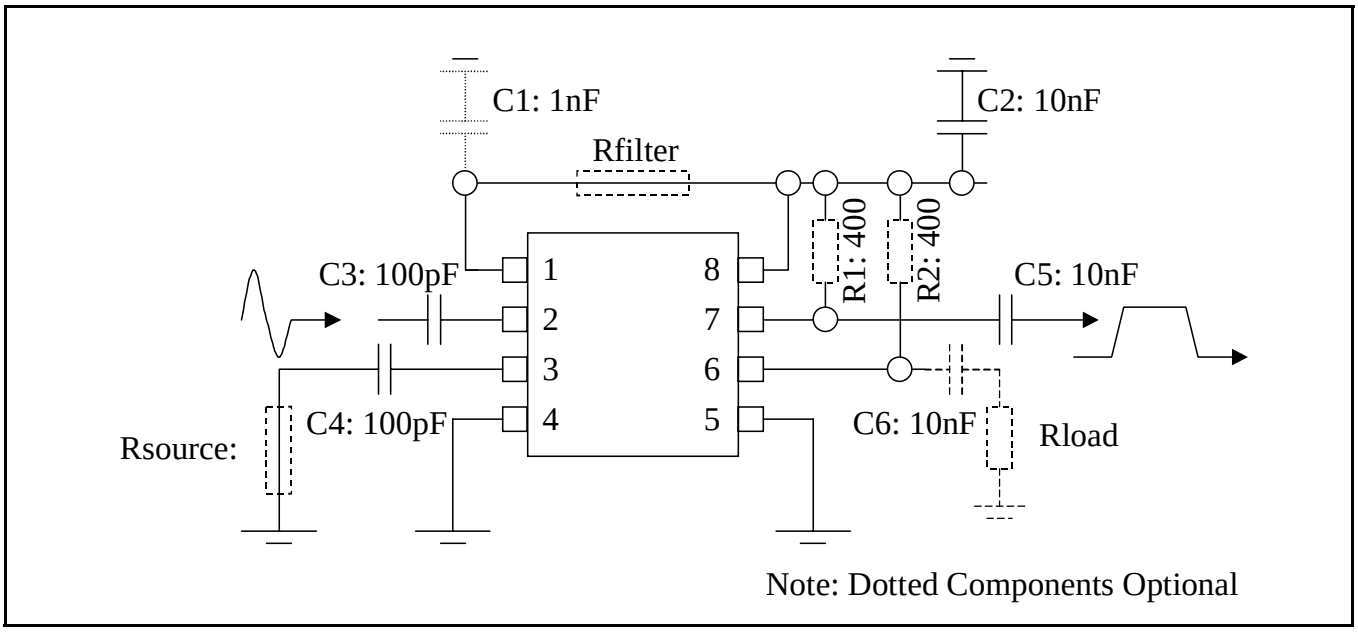


Figure 3 - Recommended circuit configuration

This represents the circuit used to complete characterisation. The tabulated Electrical performance is guaranteed using this application circuit.

Unpopulated evaluation boards are available, type No. ZLE40008. Fully populated evaluation boards are also available, type Nos. ZLE40800 and ZLE40802.

Circuit Options

The application circuit includes some optional components that may be required to improve tolerance of system noise present in the application.

Dummy R source may be added to the inverting input to provide a better matched source impedance at the input. This will improve the rejection of common mode noise present within the system.

Dummy R load may be added to the inverting output to provide better matched load at the output. This will reduce the radiated EMI at the output and reduce the Output Noise present on the supply rail.

R1 and R2 400 Ohm Pull ups are added to increase the headroom present at the amplifier output. This enhances the operation at maximum supply and temperature. An alternative is to provide an inductive choke in place of R1 and R2.

These components provide a parallel DC Path to Vcc increasing the bandwidth of the output stage and providing a virtually flat output power across frequency. See Fig 12 and 13.

Rfilter can be inserted between the Vcc in and the Vcc_out to provide additional filtering to the input Vcc. The input Vcc powers the input bias reference only and can be a sensitive point to system noise. The nominal input current at Vcc_IN s 0.35mA. An alternative would be to use an inductive choke.

C1 is additional Supply Filtering and should be added with Rfilter. The IC includes 10pF of on Chip Supply Filtering.

Input and Output Circuit

Figure 4 shows the equivalent input and output circuit.

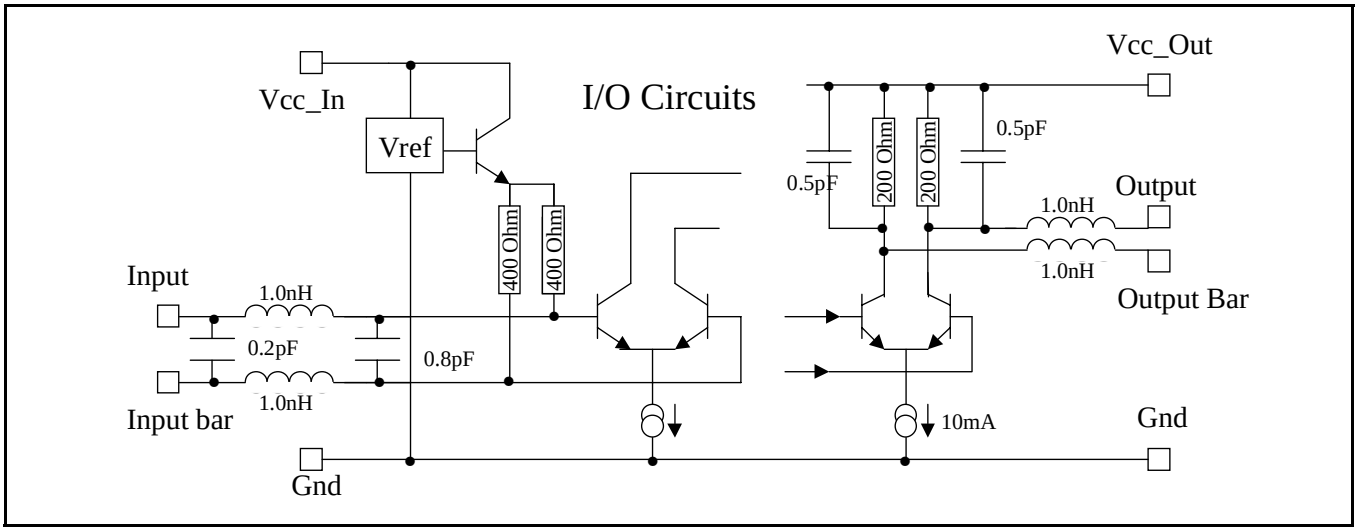


Figure 4 - Input and Output Equivalent Circuit

Increase Output Power Output Match and Narrow Band Operating Range

The device has been characterised with a mismatch at the output. This is a broadband configuration. 3dB more output power is available if the application matches the load to the output impedance.

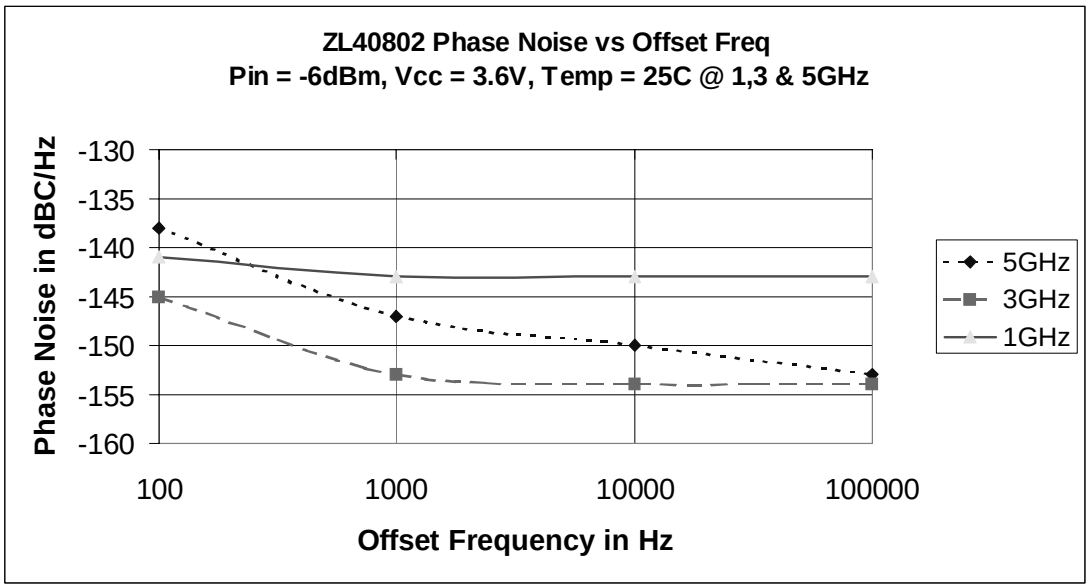


Figure 5 - ZL40802 Typical Phase Noise

Absolute Maximum Ratings

	Parameter	Symbol	Min	Max	Units
1	Supply voltage	Vcc	-0.5	6	V
2	RFin			12	dBm
3	All I/O ports		-0.5	+0.5	V
4	ESD protection		2k		V Mil-std 883B / 3015 cat1
5	Storage temperature		-55	+150	°C

Operating Ranage

	Parameter	Symbol	Min	Max	Units
1	Supply voltage	Vcc	3.3	3.6	V
2	RFin Frequency Range		0.1	6	GHz
3	Operating Junction Temperature		-40	125	°C
4	Junc'n to Amb't resistance	Rth (j-a)	150		°C/W 4 layer FR4 Board
5	Junc'n to Amb't resistance	Rth (j-c)	60		°C/W 4 layer FR4 Board

AC/DC Electrical Characteristics

Electrical Characteristics†

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Icc_in (Supply current)	1		0.35		mA	ZL40800 Div8 & ZL40802 Div16
Icc_out (Supply current)	8	29	52	86	mA	ZL40800 Div8
Icc_out (Supply current)	8	31	55	89	mA	ZL40802 Div16
Input frequency	2,3	1		6	GHz	RMS sinewave,
Input sensitivity	2,3		-20	-10	dBm	fin = 1GHz to 6GHz, Note 1
Input overload	2,3	4	10		dBm	fin = 1GHz to 6GHz, Note 1
Phase Noise	6,7		-150		dBC/Hz	@ 1KHz Offset Fin = 3GHz
Output voltage	6,7		1		Vp-p	Differential Into 50ohm pull up resistors
Output power	6,7	-7	-2	2	dBm	fin = 1GHz to 6GHz, Pin = -10dBm Note 2
Output t-rise	6,7		110		ps	fin = 1GHz to 6GHz, Pin = -10dBm
Output t-fall	6,7		110		ps	fin = 1GHz to 6GHz, Pin = -10dBm
T – prop delay	2,6		250		ps	50% IN to 50% OUT
Jitter	6,7		0.1		ps	
Output Duty Cycle	6,7	45	50	55	%	fin = 1GHz to 6GHz, In = -10dBm
Input Edge Speed	2,3	500			V/us	For < 1GHz input operation

† These characteristics are guaranteed by design and characterisation over the following range of operating conditions unless otherwise stated: Tamb = -40C to + 85C, Vcc = 3.3V to 3.6V.

Note 1: Pin = power measured into 50 ohm Load from 50 Ohm Source.

Note 2: Pout Single Ended AC coupled Single 50 Ohm Termination

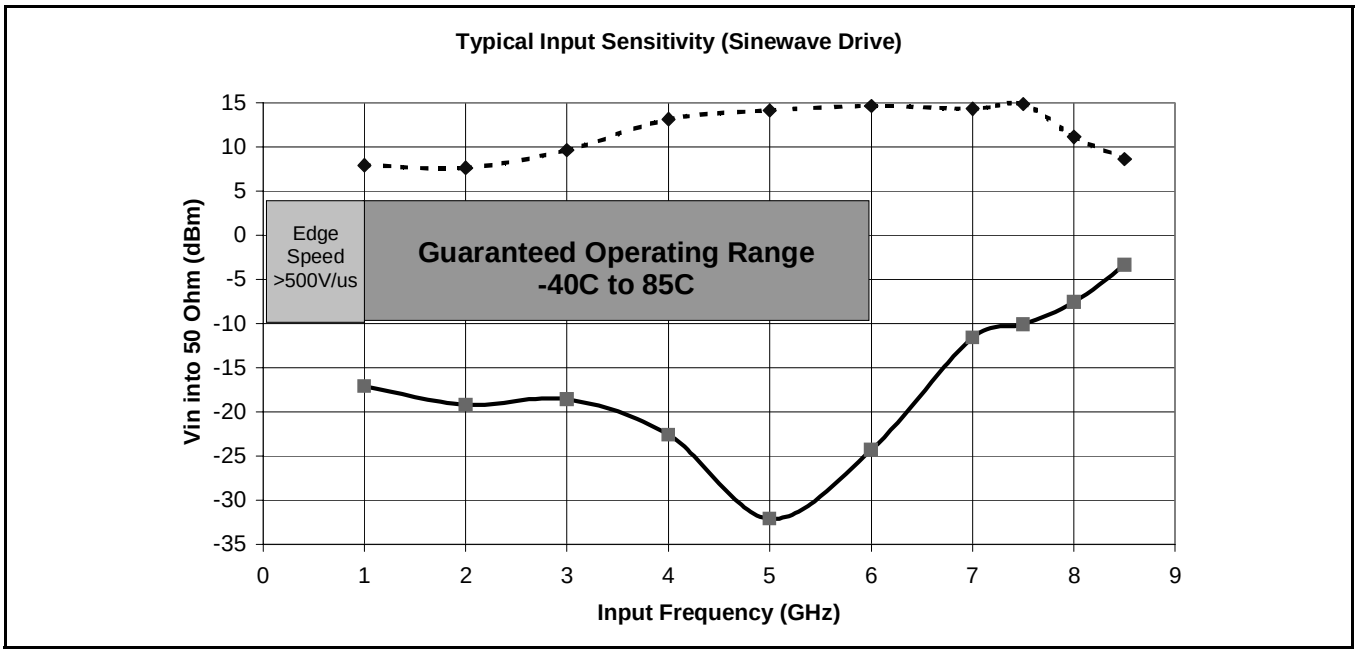


Figure 6 - Typical Input Sensitivity (sine wave drive)

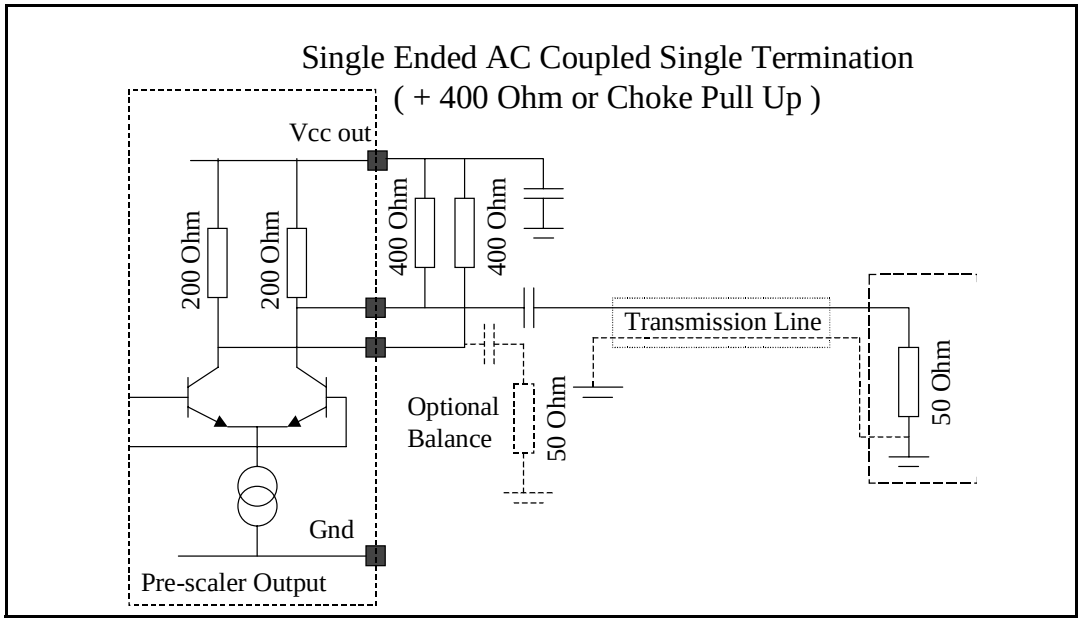


Figure 7 - Single Ended AC Coupled Single Termination

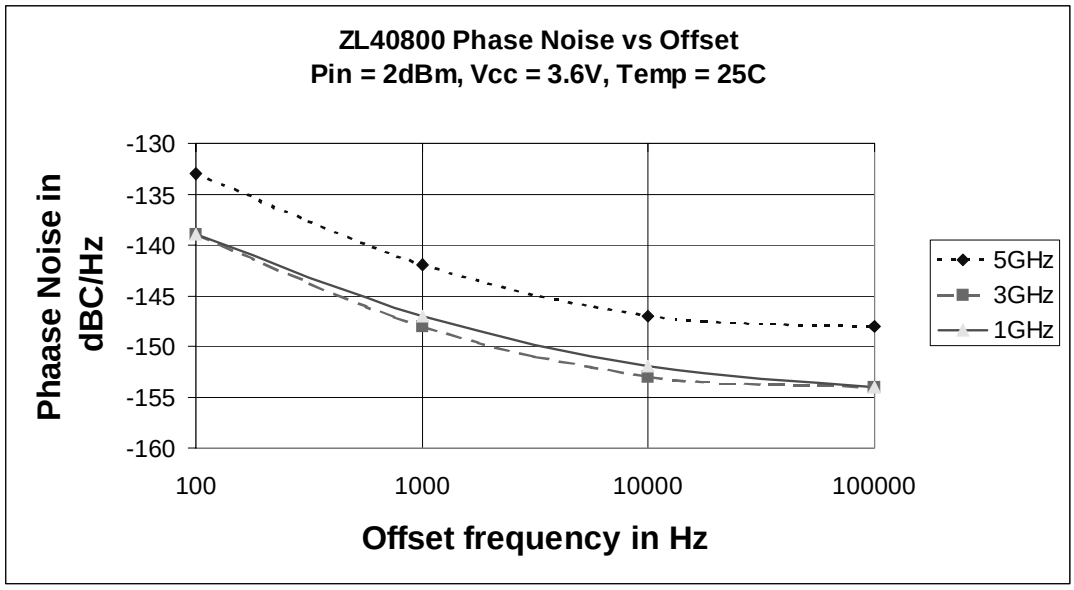


Figure 8 - ZL40800 Typical Phase Noise

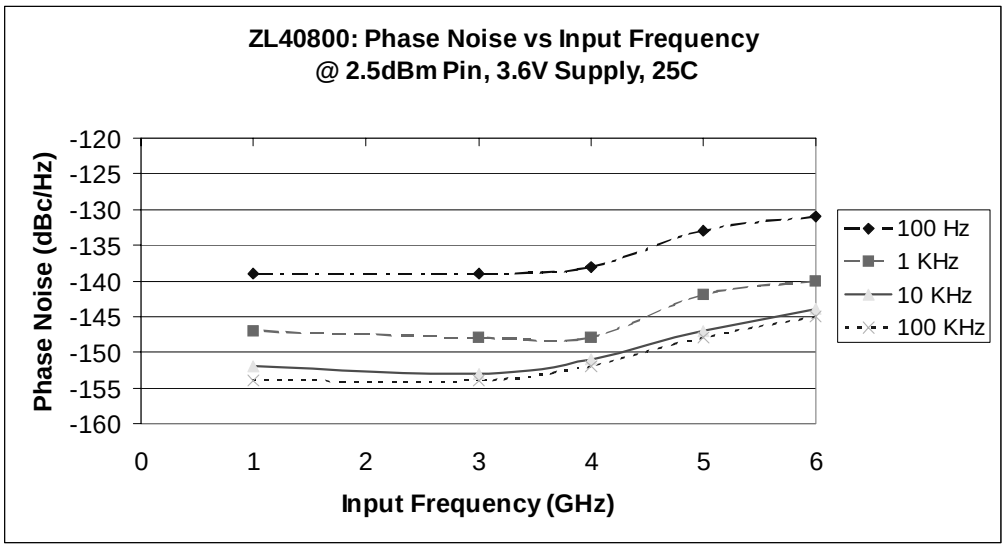


Figure 9 - ZL40800 Phase Noise vs Input Frequency

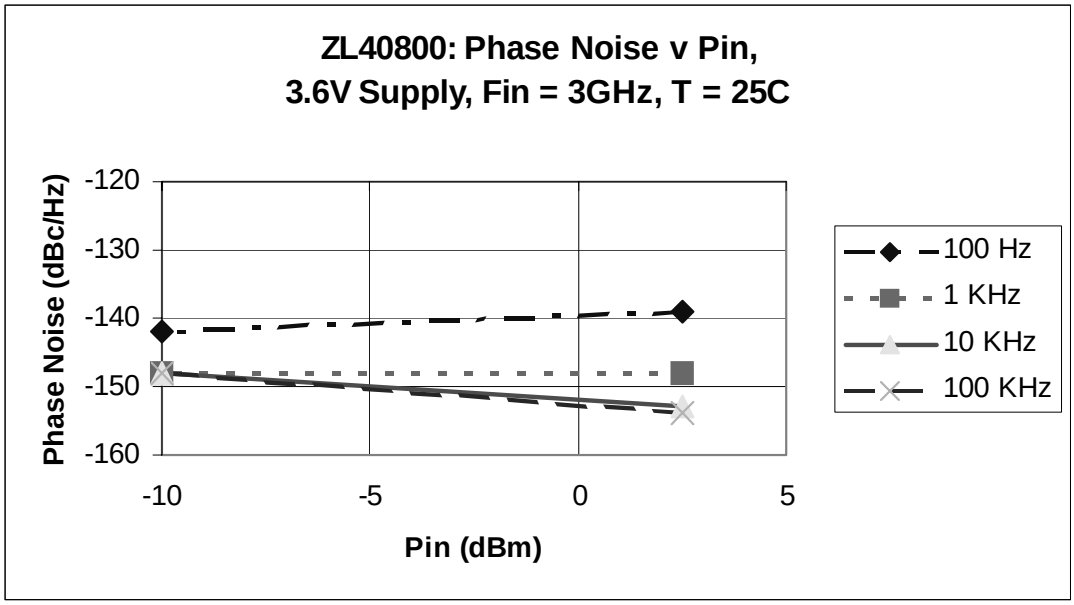


Figure 10 - ZL40800 Phase Noise vs Input Power

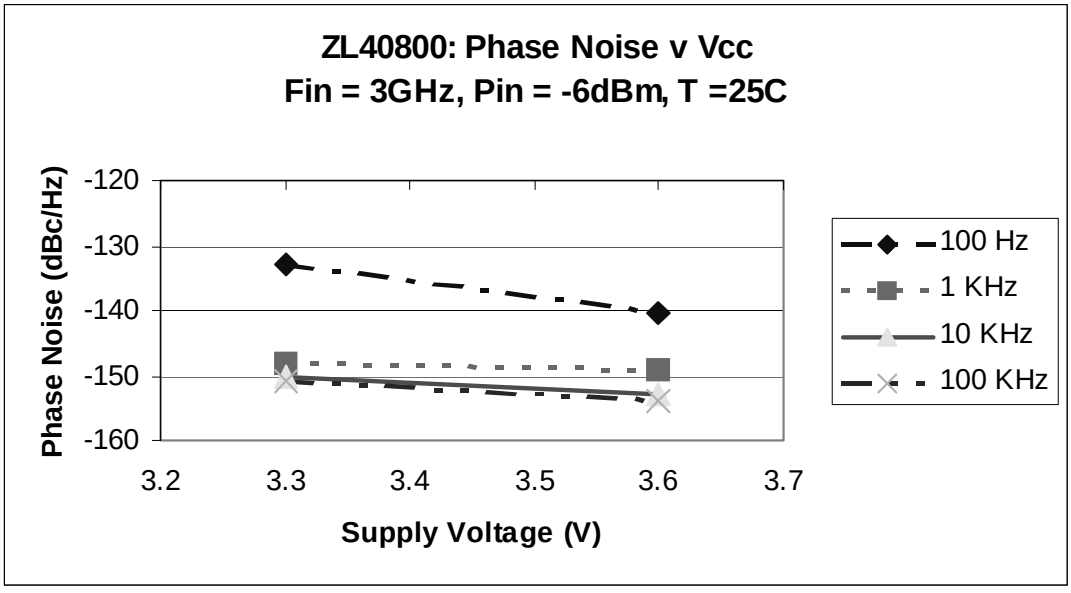


Figure 11 - ZL40800 Phase Noise vs Vcc

Single Ended or Differential Load

Figure 12 and Figure 13 illustrate the output waveform when measured differential and single ended with a 6GHz waveform at the input at a level of +2dBm. The single ended output contains some input frequency breakthrough which contributes to the distortion present. This is a common mode signal which is rejected if the output is taken differentially.

Differential operation also provides an additional 3dB. Differential Operation reduces the radiated EMI in the system and reduces the susceptibility to common mode system noise.

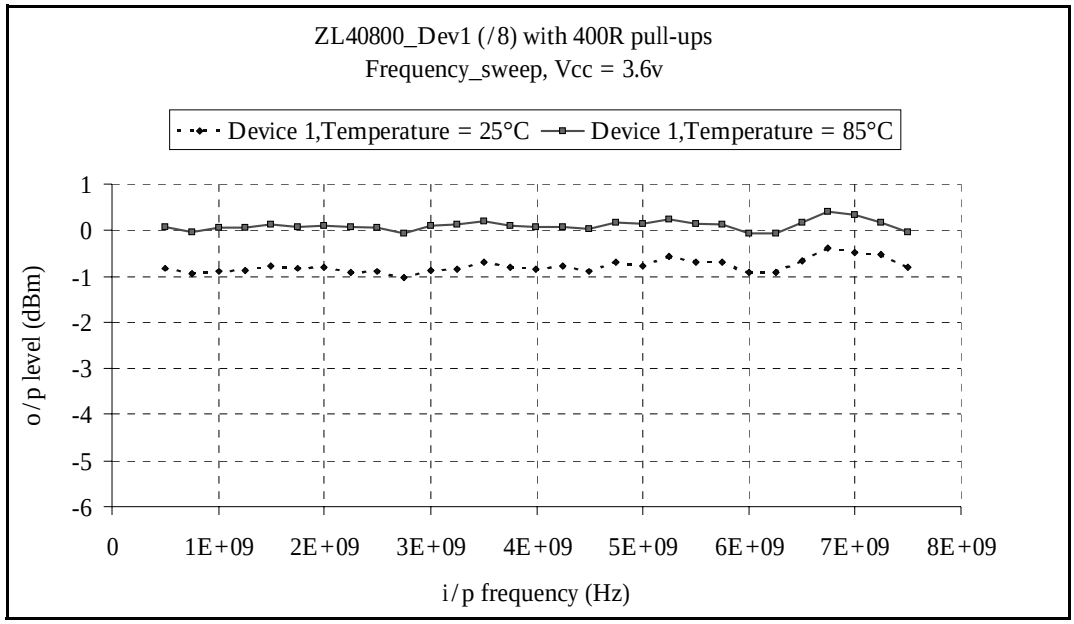


Figure 12 - ZL40800 Pout / Input Frequency

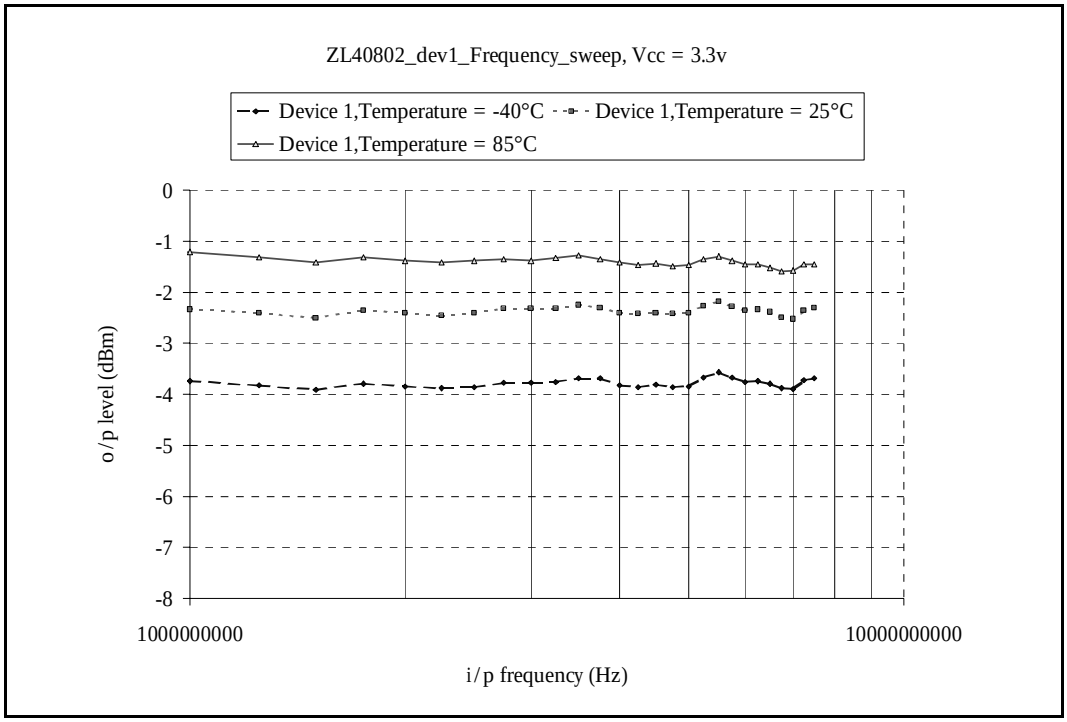


Figure 13 - ZL40800Pout v Input Frequency (Vcc=3.3V, T= -40C,25C, 85C)

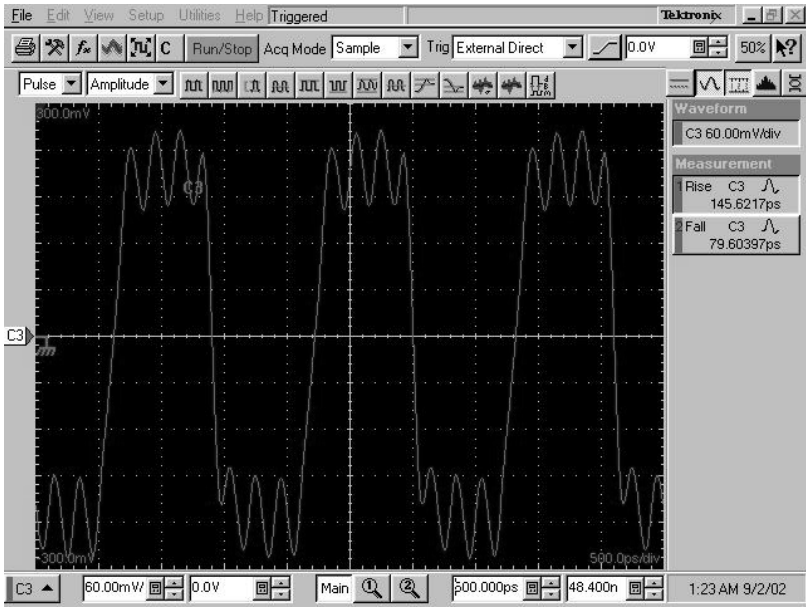


Figure 14 - ZL40800 Single Ended Out @ 5Ghz +2dBm

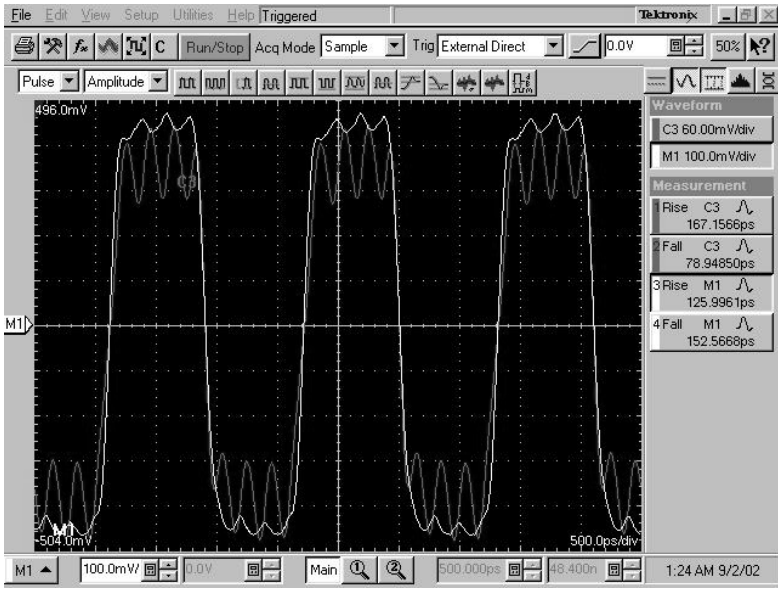
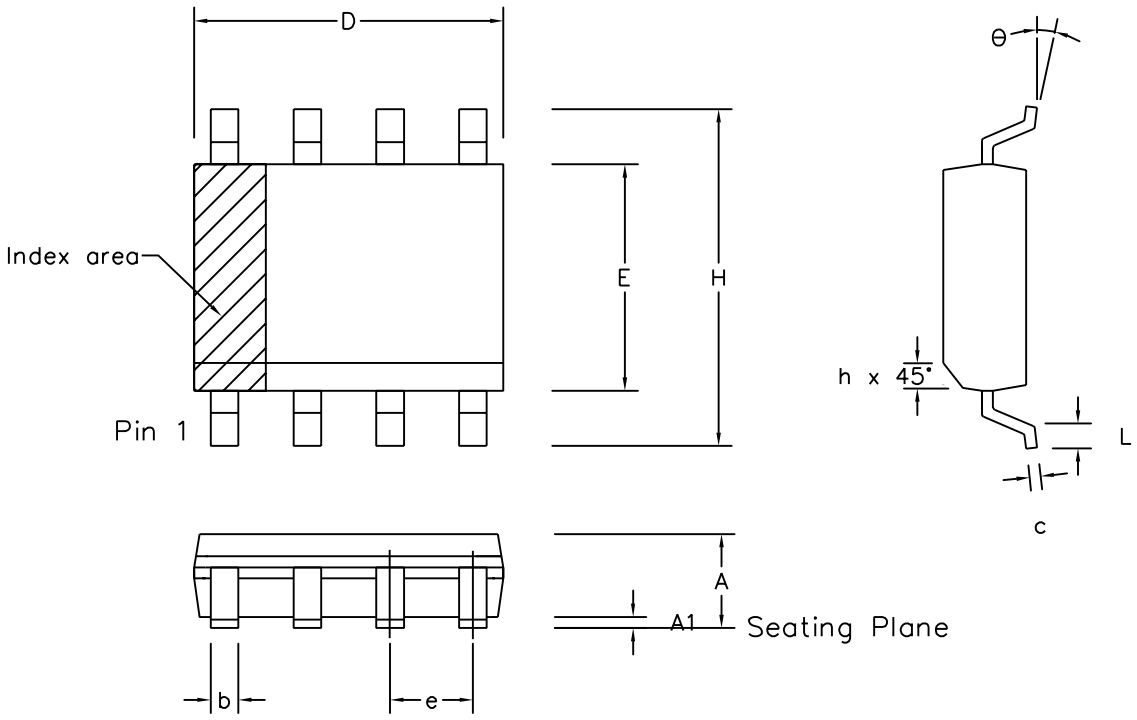


Figure 15 - ZL40800 Differential Out @ 5Ghz +2dBm



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	8		8	
Conforms to JEDEC MS-012AA Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	4	5
ACN	6745	201936	202595	203705	212424
DATE	5Apr95	27Feb97	12Jun97	9Dec97	22Mar02
APPRD.					

ZARLINK SEMICONDUCTOR

Previous package codes

MP / S

Package Code DC

Package Outline for 8 lead SOIC (0.150" Body width)

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