

## Revision History

### Revision 1 ( Dec. 2001 )

- 1.Fister release.

### Revision 2 ( Apr. 2002 )

1. Changed module current specification.
2. Add Performance range.
3. Changed AC Characteristics.
4. Changed typo size on module PCB in package dimensions.

## DDR SDRAM 184pin DIMM

### 16Mx64bits DDR SDRAM 184pin DIMM based on 16Mx8

#### General Description

The VDBDB1608 is 16Mx64 bits Double Data Rate SDRAM Modules, The modules are composed of eight 16Mx8 bits CMOS Double Data Rate SDRAMs in TSOP-II 400mil 66pin package and one 2Kbit EEPROM in 8pin TSSOP(TSOP) package on a 184pin glass-epoxy printed circuit board.

The V-Data is a Dual In-line Memory Module and is intended for mounting onto 184-pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

#### Performance range

Part No.	Max Freq.	Interface
VDBDB1608	166MHz	SSTL_2

#### Features

- DLL aligns DQ and DQS transition with CK transition
- Double-data-rate architecture.
- Bi-directional data strobe (DQS)
- Differential clock inputs(CK and /CK)
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Power supply: Vdd,Vddq:2.5V±0.2V
- Programmable Burst length (2,4,8)
- Serial Presence Detect with EEPROM
- Module bank : one physical bank
- PCB : BUDA84A,Height (29.21mm),single sided component, Six layers

#### Pin Assignment

FRONT SIDE								BACK SIDE							
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	VREF	24	DQ17	47	DQS8	70	VDD	93	VSS	116	VSS	139	VSS	162	DQ47
2	DQ0	25	DQS2	48	A0	71	*/CS2	94	DQ4	117	DQ21	140	DM8	163	*/CS3
3	VSS	26	VSS	49	CB2	72	DQ48	95	DQ5	118	A11	141	A10	164	VDDQ
4	DQ1	27	A9	50	VSS	73	DQ49	96	VDDQ	119	DM2	142	CB6	165	DQ52
5	DQS0	28	DQ18	51	CB3	74	VSS	97	DM0	120	VDD	143	VDDQ	166	DQ53
6	DQ2	29	A7	52	BA1	75	/CK2	98	DQ6	121	DQ22	144	CB7	167	NC
7	VDD	30	VDDQ	53	DQ32	76	CK2	99	DQ7	122	A8	145	VSS	168	VDD
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ	100	VSS	123	DQ23	146	DQ36	169	DM6
9	NC	32	A5	55	DQ33	78	DQS6	101	NC	124	VSS	147	DQ37	170	DQ54
10	NC	33	DQ24	56	DQS4	79	DQ50	102	NC	125	A6	148	VDD	171	DQ55
11	VSS	34	VSS	57	DQ34	80	DQ51	103	*A13	126	DQ28	149	DM4	172	VDDQ
12	DQ8	35	DQ25	58	VSS	81	VSS	104	VDDQ	127	DQ29	150	DQ38	173	NC
13	DQ9	36	DQS3	59	BA0	82	VDDID	105	DQ12	128	VDDQ	151	DQ39	174	DQ60
14	DQS1	37	A4	60	DQ35	83	DQ56	106	DQ13	129	DM3	152	VSS	175	DQ61
15	VDDQ	38	VDD	61	DQ40	84	DQ57	107	DM1	130	A3	153	DQ44	176	VSS
16	CK1	39	DQ26	62	VDDQ	85	VDD	108	VDD	131	DQ30	154	/RAS	177	DM7
17	/CK1	40	DQ27	63	/WE	86	DQS7	109	DQ14	132	VSS	155	DQ45	178	DQ62
18	VSS	41	A2	64	DQ41	87	DQ58	110	DQ15	133	DQ31	156	VDDQ	179	DQ63
19	DQ10	42	VSS	65	/CAS	88	DQ59	111	*CKE1	134	CB4	157	/CS0	180	VDDQ
20	DQ11	43	A1	66	VSS	89	VSS	112	VDDQ	135	CB5	158	*/CS1	181	SA0
21	CKE0	44	CB0	67	DQS5	90	NC	113	*BA2	136	VDDQ	159	DM5	182	SA1
22	VDDQ	45	CB1	68	DQ42	91	SDA	114	DQ20	137	CK0	160	VSS	183	SA2
23	DQ16	46	VDD	69	DQ43	92	SCL	115	*A12	138	/CK0	161	DQ46	184	VDDS

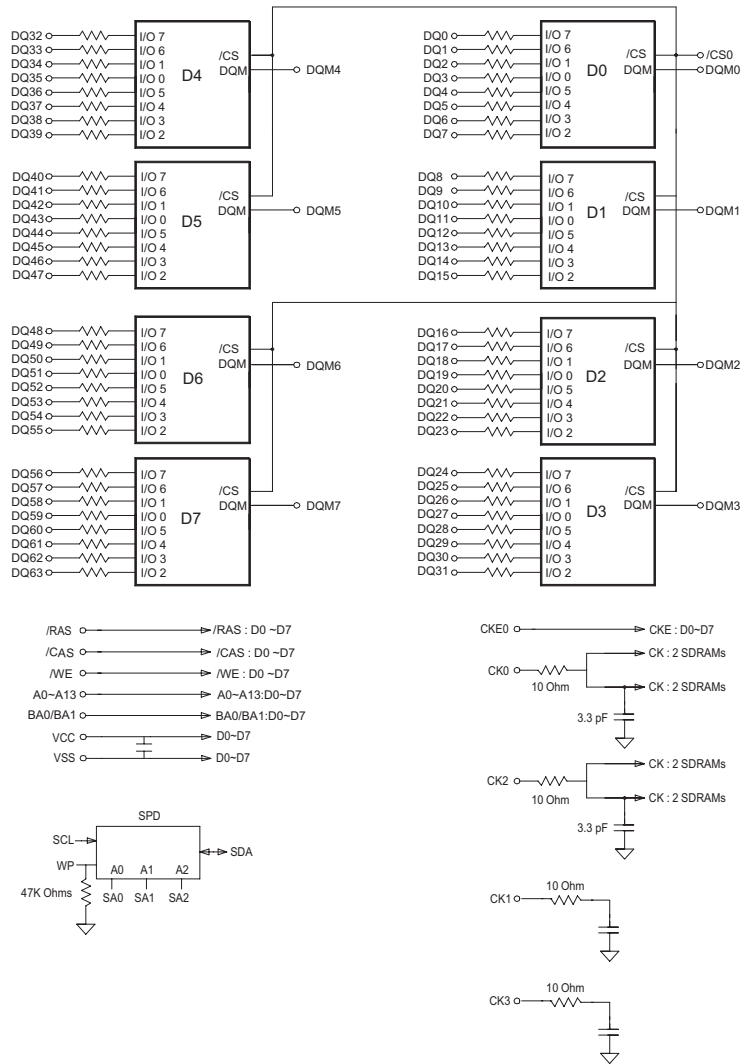
\* These pins are not used in this module.

## Pin Description

PIN	NAME	FUNCTION
CK0~CK2,/CK0~2	System Clock	Active on the positive edge to sample all inputs.
CKE0	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least on cycle prior new command. Disable input buffers for power down in standby
/CS0	Chip Select	Disables or Enables device operation by masking or enabling all input except CK, CKE and L(U)DQM
A0~A11	Address	Row / Column address are multiplexed on the same pins.
BA0~BA1	Banks Select	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
DQ0~DQ63	Data	Data inputs / outputs are multiplexed on the same pins.
DQS0~DQS7	Data Strobe	Bi-directional Data Strobe
DM0~8	Data Mask	Makes data output Hi-Z,
/RAS	Row Address Strobe	Latches row addresses on the positive edge of the CLK with /RAS low
/CAS	Column Address Strobe	Latches Column addresses on the positive edge of the CLK with /CAS low
/WE	Write Enable	Enables write operation and row recharge.
VDD/VSS	Power Supply/Ground	Power and Ground for the input buffers and the core logic.
VDDQ	Power Supply	Power Supply for DQS
VREF	Power Supply reference	Power Supply for reference
VDDS	SPD Power Supply	Serial EEPROM power Supply
SDA	Serial data I/O	EEPROM serial data I/O
SCL	Serial clock	EEPROM clock input
SA0~2	Address in EEPROM	EEPROM address input
VDDID	VDD identification	VDD identification flag
NC	No Connection	This pin is recommended to be left No Connection on the device.

## Block Diagram

1



## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>out</sub>	-0.5~3.6	V
Voltage on VDD supply relative to Vss	V <sub>DD</sub>	-1.0~3.6	V
Voltage on VDDQ supply relative to Vss	V <sub>DDQ</sub>	-0.5~3.6	V
Storage temperature	T <sub>STG</sub>	-55~+150	°C
Power dissipation	P <sub>D</sub>	12	W
Short circuit current	I <sub>OS</sub>	50	mA

**Note** : Permanent device damage may occur if ABSOLUTE MAXIMUM RATING are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## DC Operating Condition

Voltage referenced to Vss = 0V, T<sub>A</sub> = 0 to 70 °C

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V <sub>DD</sub> , V <sub>DDQ</sub>	2.3	2.7	V	
Reference voltage	V <sub>REF</sub>	V <sub>DDQ</sub> /2-50mV	V <sub>DDQ</sub> /2+50mV	V	1
Termination voltage	V <sub>TT</sub>	V <sub>REF</sub> -0.04	V <sub>REF</sub> +0.04		2
Input logic high voltage	V <sub>IH</sub>	V <sub>REF</sub> +0.15	V <sub>DDQ</sub> +0.3	V	3
Input logic low voltage	V <sub>IL</sub>	-0.3	V <sub>REF</sub> -0.15	V	3
Output logic high voltage	V <sub>OH</sub>	V <sub>TT</sub> +0.84	-	V	I <sub>OH</sub> =-16.8mA
Output logic low voltage	V <sub>OL</sub>	-	V <sub>TT</sub> -0.84	V	I <sub>OL</sub> =16.8mA
Input voltage Level	V <sub>IN</sub>	-0.3	V <sub>DDQ</sub> +0.3	V	
Input Differential Voltage	V <sub>ID</sub>	0.3	V <sub>DDQ</sub> +0.6	V	4
Input crossing point voltage	V <sub>IX</sub>	1.15	1.35	V	5
Input leakage current	I <sub>IL</sub>	-2	2	uA	
Output leakage current	I <sub>OL</sub>	-5	5	uA	

**Note** : 1. Includes±25mV margin for DC offset on V<sub>REF</sub>, and a combined total of ±50mV margin for all AC noise and DC offset on V<sub>REF</sub>, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V<sub>REF</sub> and internal DRAM noise coupled TO V<sub>REF</sub>, both of which may result in V<sub>REF</sub> noise. V<sub>REF</sub> should be de-coupled with an inductance of ≤ 3nH.

2.V<sub>TT</sub> is not applied directly to the device. V<sub>TT</sub> is a system supply for signal termination resistors, is expected to be set equal to V<sub>REF</sub>, and must track variations in the DC level of V<sub>REF</sub>

3.These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V<sub>REF</sub> envelop that has been bandwidth limited to 200MHz.

4.V<sub>ID</sub> is the magnitude of the difference between the input level on CK and the input level on /CK.

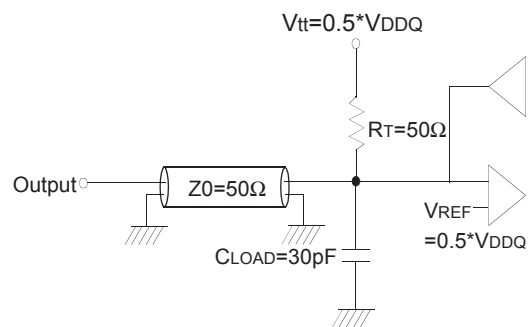
5.The value of V<sub>IX</sub> is expected to equal 0.5\*V<sub>DDQ</sub> of the transmitting device and must track variations in the DC level of the same.

## Capacitance

TA=25°C, VDDQ=2.5V, VDD=2.5V

Parameter	Pin	Symbol	Min	Max	Unit
Input capacitance	CK,A0~A11,BA0,BA1,RAS,/CAS,/WE	CI1	49	57	pF
Input capacitance	CKE,CS	CI2	42	50	pF
Input capacitance	CK0~CK2	CI3	22	25	PF
Data input / output capacitance	DQM	CI4	6	8	pF
Input capacitance	DM0~DM8	CI5	6	8	pF

## Output load circuit



Output Load Circuit (SSTL\_2)

## DC Characteristics II

TA=0 to 70°C

Symbol	Condition	Typical	Unit	Note
IDD0	One bank Active-Precharge	840	mA	
IDD1	One bank operation	1,040	mA	
IDD2P	Precharge power-down standby current	28	mA	
IDD2F	Precharge floating standby current	200	mA	
IDD2Q	Precharge quiet standby current	144	mA	
IDD3P	Active power-down standby current	280	mA	
IDD3N	Active standby current	480	mA	
IDD4R	Operating current-burst read	1,280	mA	
IDD4W	Operating current-burst write	1,216	mA	
IDD5	Auto refresh current	1,520	mA	
IDD6	Self refresh current	16	mA	
IDD7A	Operating current-Four bank operation	2,640	mA	

## AC Characteristics

Parameter		Symbol	VDBDB1608		Unit	Note
			Min	Max		
System clock	/CAS Latency = 2.5	tCK2.5	7.5	12	ns	
Cycle time	/CAS Latency = 2	tCK2	6	12		
Clock high pulse width		tCHW	0.45	0.55	tCK	
Clock low pulse width		tCLW	0.45	0.55	tCK	
Access time form clock		tAC	-0.75	0.75	ns	
/RAS cycle time		tRC	60		ns	
/RAS to /CAS delay		tRCD	18		ns	
/RAS active time		tRAS	42	120K	ns	
/RAS precharge time		tRP	18		ns	
/RAS to /RAS bank active delay		tRRD	12		ns	
Write recovery time		tWR	15		tCK	
Refresh row cycle time		tRFC	75		ns	
Col. Address to Col. Address delay		tCCD	1		tCK	
DQS out access time from CK /CK		tDQSCK	-0.6	+0.6	ns	
Data strobe edge to output data edge		tDQSQ		+0.45	ns	
CK to valid DQS-in		tDQSS	0.75	1.25	tCK	
DQS – input setup time		tWPRES	0		ns	
DQS – input hold time		tWPREH	0.25		tCK	
Address/Command setup time		tIS	0.75		ns	
Address/Command hold time		tIH	0.75		ns	
DQS falling edge to CK rising-setup time		tDDS	0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		tCK	
DQS in high level width		tDQSH	0.35		tCK	
DQS in low level width		tDQSL	0.35		tCK	
DQS in cycle time		tDSC	0.9	1.1	tCK	
MRS to new command		tMRD	12		ns	
Power down exit time		tPDEX	6		ns	

## Command Truth-Table

Command		CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	ADDR	A10/AP	BA
Mode Register Set		H	X	L	L	L	L	X	OP code		
No Operation		H	X	L	H	H	H	X	X		
Bank Active		H	X	L	L	H	H	X	RA		V
Read		H	X	L	H	L	H	X	CA	L	V
Read with Auto Precharge										H	
Write		H	X	L	H	L	L	X	CA	L	V
Write with Auto Precharge										H	
Precharge All Bank		H	X	L	L	H	L	X	X	H	X
Precharge select Bank										L	V
Burst Stop		H	X	L	H	H	L	X	X		
Auto Refresh		H	H	L	L	L	H	X	X		
Self Refresh	Entry	H	L	L	L	L	H	X	X		
	Exit	L	H	H	X	X	X	X			
				L	H	H	H				
Precharge Power down	Entry	H	L	H	X	X	X	X	X		
				L	H	H	H				
	Exit	L	H	H	X	X	X	X			
				L	H	H	H				
Clock Suspend	Entry	H	L	X	X	X	X	X	X		
	Exit	L	H	X	X	X	X	X			



## Package Information

