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Nonvolatile Memory, Dual 1024
Position Digital Potentiometers

AD5235

FEATURES

Dual, 1024 Position Resolution
 25K, 250K Ohm Terminal Resistance with 50ppm/°C Tempco
 Nonvolatile Memory Preset
 SPI Compatible Serial Data Input with Readback Function
 Increment/Decrement Commands, Push Button Command
 +3 to +5V Single Supply Operation
 ±2.5V Dual Supply Operation
 30 bytes of general purpose nonvolatile memory

APPLICATIONS

Mechanical Potentiometer Replacement
 Instrumentation: Gain, Offset Adjustment
 Programmable Voltage to Current Conversion
 Programmable Filters, Delays, Time Constants
 Line Impedance Matching
 Power Supply Adjustment
 DIP Switch Setting

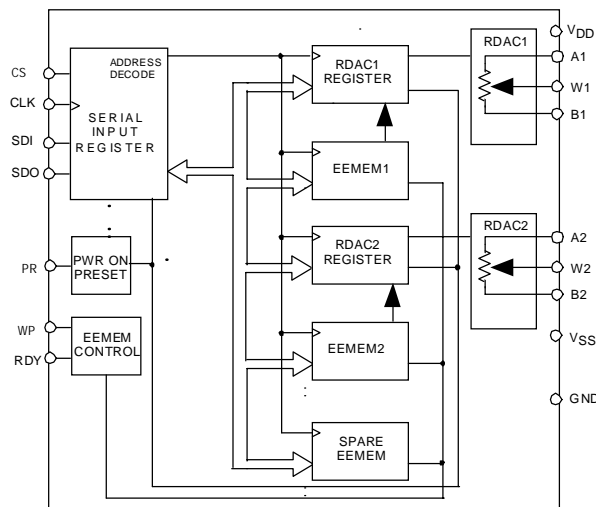
GENERAL DESCRIPTION

The AD5235 provides a dual channel, digitally controlled variable resistor (VR) with resolutions of 1024 positions. These devices perform the same electronic adjustment function as a potentiometer or variable resistor. The AD5235's versatile programming via a Micro Controller allows multiple modes of operation and adjustment.

In the direct program mode a predetermined setting of the RDAC register can be loaded directly from the micro controller. Another key mode of operation allows the RDAC register to be refreshed with the setting previously stored in the EEMEM register. When changes are made to the RDAC register to establish a new wiper position, the value of the setting can be saved into the EEMEM by executing an EEMEM save operation. Once the settings are saved in the EEMEM register, these values will be transferred automatically to the RDAC register to set the wiper position at system power ON. Such operation is enabled by the internal preset strobe and the preset can also be accessed externally.

An internal scratch pad RDAC register can be programmed by the micro controller to set the resistance between terminals W-and-B. Once the target value is achieved, the RDAC content register can be placed in the non-volatile memory for automatic recall during Power Up.

The AD5235 is available in the thin TSSOP-16 package. All parts are guaranteed to operate over the extended industrial temperature range of -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAMS

REV PrD 6 Nov 2000

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Nonvolatile Memory Digital Potentiometers

AD5235

ELECTRICAL CHARACTERISTICS 25K, 250K OHM VERSIONS(V_{DD} = +3V±10% or +5V±10% and V_{SS}=0V, V_A = +V_{DD}, V_B = 0V, -40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE Specifications apply to all VRs						
Resistor Differential NL ²	R-DNL	R _{WB} , V _A =NC	-1	±1/4	+1	LSB
Resistor Nonlinearity ²	R-INL	R _{WB} , V _A =NC	-2	±1/2	+2	LSB
Nominal resistor tolerance	ΔR	T _A = 25°C, V _{AB} = V _{DD} , Wiper (V _W) = No connect	-30		30	%
Resistance Temperature Coefficient	R _{AB} /ΔT	V _{AB} = V _{DD} , Wiper (V _W) = No Connect		50		ppm/°C
Wiper Resistance	R _W	I _W = 1 V/R, V _{DD} = +5V		50	100	Ω
Wiper Resistance	R _W	I _W = 1 V/R, V _{DD} = +3V		200		Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE Specifications apply to all VRs						
Resolution	N		10			Bits
Integral Nonlinearity ³	INL		-2	±1/2	+2	LSB
Differential Nonlinearity ³	DNL		-1	±1/4	+1	LSB
Voltage Divider Temperature Coefficient	ΔV _W /ΔT	Code = Half-scale		15		ppm/°C
Full-Scale Error	V _{WFSE}	Code = Full-scale	-3	-1	+0	LSB
Zero-Scale Error	V _{WZSE}	Code = Zero-scale	0	+1	+3	LSB
RESISTOR TERMINALS						
Voltage Range ⁴	V _{A,B,W}		V _{SS}		V _{DD}	V
Capacitance ⁵ Ax, Bx	C _{A,B}	f = 1 MHz, measured to GND, Code = Half-scale		45		pF
Capacitance ⁵ Wx	C _W	f = 1 MHz, measured to GND, Code = Half-scale		60		pF
Common-mode Leakage Current ⁷	I _{CM}	V _A = V _B = V _{DD} /2		0.01	1	μA
DIGITAL INPUTS & OUTPUTS						
Input Logic High	V _{IH}	with respect to GND			0.3•V _{DD}	V
Input Logic Low	V _{IL}	with respect to GND	0.7•V _{DD}			V
Output Logic High	V _{OH}	R _{PULL-UP} = 2.2KΩ to +5V	4.9			V
Output Logic High	V _{OH}	I _{OH} = 40μA, V _{LOGIC} = +5V	4			V
Output Logic Low	V _{OL}	I _{OL} = 1.6mA, V _{LOGIC} = +5V			0.4	V
Input Current	I _{IL}	V _{IN} = 0V or V _{DD}			±1	μA
Input Capacitance ⁵	C _{IL}			5		pF
POWER SUPPLIES						
Single-Supply Power Range	V _{DD}	V _{SS} = 0V	2.7		5.5	V
Dual-Supply Power Range	V _{DD} /V _{SS}	V _{SS} = 0V	±2.2		±2.7	V
Positive Supply Current	I _{DD}	V _{IH} = V _{DD} or V _{IL} = GND		2	20	μA
Programming Mode Current	I _{DD} (PG)	V _{IH} = V _{DD} or V _{IL} = GND		15		mA
Read Mode Current	I _{DD} (READ)	V _{IH} = V _{DD} or V _{IL} = GND		650		μA
Negative Supply Current	I _{SS}	V _{IH} = V _{DD} or V _{IL} = GND, V _{DD} = 2.5V, V _{SS} = -2.5V			10	μA
Power Dissipation ⁶	P _{DISS}	V _{IH} = V _{DD} or V _{IL} = GND			0.05	mW
Power Supply Sensitivity	PSS	ΔV _{DD} = +5V ±10%		0.002	0.01	%/%
DYNAMIC CHARACTERISTICS ^{5, 7}						
Bandwidth -3dB	BW_25K	R = 12KΩ		400		KHz
Total Harmonic Distortion	THD _W	V _A = 1Vrms, V _B = 0V, f = 1KHz		0.003		%
V _W Settling Time	t _S	V _A = V _{DD} , V _B = 0V, 50% of final value				μs
		25K/250K		0.6/3/6		
Resistor Noise Voltage	e _{N-WB}	R _{WB} = 10KΩ, f = 1KHz		9		nV/√Hz
Crosstalk	C _T	V _A = V _{DD} , V _B = 0V, Measure V _W with adjacent VR making full scale change		-65		dB

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ELECTRICAL CHARACTERISTICS 25K, 250K OHM VERSIONS ($V_{DD} = +3V \pm 10\%$ to $+5V \pm 10\%$ and $V_{SS} = 0V$, $V_A = +V_{DD}$, $V_B = 0V$, $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Units
INTERFACE TIMING CHARACTERISTICS applies to all parts (Notes 5, 8)						
Clock Cycle Time	t_1		20			ns
Input Clock Pulse Width	t_2, t_3	Clock level high or low	10			ns
\overline{CS} Setup Time	t_4		10			ns
Data Setup Time	t_5	From Positive CLK transition	5			ns
Data Hold Time	t_6	From Positive CLK transition	5			ns
CLK Shutdown Time	t_7		0			ns
\overline{CS} Rise to Clock Rise Setup	t_8		10			ns
\overline{CS} High Pulse Width	t_9		10			ns
CLK to SDO Propagation Delay ⁹	t_{10}	$R_L = 1K\Omega$, $C_L < 20pF$	1		25	ns
Store to Nonvolatile EEMEM Save Time ¹⁰	t_{11}	Applies to Command 2 _H , 3 _H			25	ms
\overline{CS} to SDO - SPI line acquire	t_{12}					ns
\overline{CS} to SDO - SPI line release	t_{13}					ns
RDY Rise to CLK Rise	t_{14}					ns
Startup Time	t_{15}					ms
CLK Setup Time	t_{16}	For 1 CLK period ($t_4 - t_3 = 1$ CLK period)				ns
Preset Pulse Width	t_{PR}		50			ns

NOTES:

- Typicals represent average readings at $+25^\circ\text{C}$ and $V_{DD} = +5V$.
- Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See figure 20 test circuit. $I_W = V_{DD}/R$ for both $V_{DD} = +3V$ or $V_{DD} = +5V$.
- INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and $V_B = 0V$. DNL specification limits of $\pm 1\text{LSB}$ maximum are Guaranteed Monotonic operating conditions. See Figure 19 test circuit.
- Resistor terminals A,B,W have no limitations on polarity with respect to each other.
- Guaranteed by design and not subject to production test.
- P_{DISS} is calculated from $(I_{DD} \times V_{DD} = +5V)$.
- All dynamic characteristics use $V_{DD} = +5V$.
- See timing diagram for location of measured values. All input control voltages are specified with $t_R = t_F = 2.5\text{ns}$ (10% to 90% of 3V) and timed from a voltage level of 1.5V. Switching characteristics are measured using both $V_{DD} = +3V$ or $+5V$.
- Propagation delay depends on value of V_{DD} , R_{PULL_UP} , and C_L see applications text.
- Low only for commands 8, 9, 10, 2, 3: CMD_8 ~ 1ms; CMD_9,10 ~ 0.1ms; CMD_2,3 ~ 20ms.

Timing Diagram

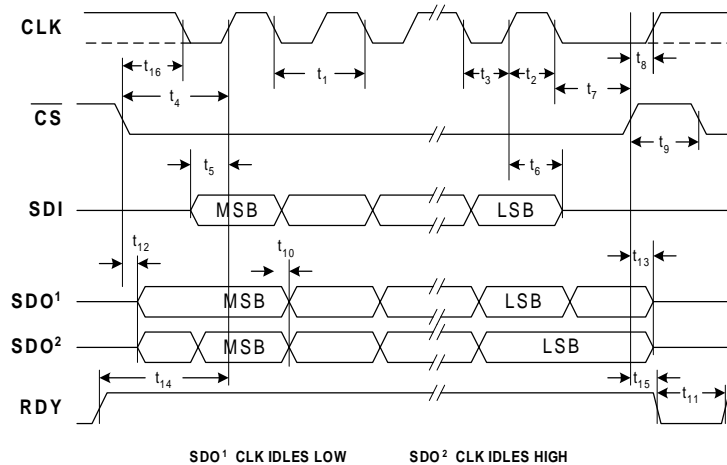


Figure 1. Timing Diagram

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Absolute Maximum Rating ($T_A = +25^\circ\text{C}$, unless otherwise noted)

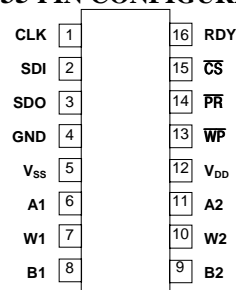
V_{DD} to GND.....	-0.3, +7V
V_{SS} to GND.....	0V, -7V
V_{DD} to V_{SS}	+7V
V_A, V_B, V_W to GND.....	V_{SS}, V_{DD}
$A_X - B_X, A_X - W_X, B_X - W_X$	$\pm 20\text{mA}$
O_X to GND.....	0V, V_{DD}
Digital Inputs & Output Voltage to GND.....	0V, +7V
Operating Temperature Range.....	-40°C to $+85^\circ\text{C}$
Maximum Junction Temperature ($T_J \text{ MAX}$).....	$+150^\circ\text{C}$
Storage Temperature.....	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec).....	$+300^\circ\text{C}$
Thermal Resistance θ_{JA} , TSSOP-16.....	180°C/W
Package Power Dissipation = $(T_J \text{ MAX} - T_A) / \theta_{JA}$	

Ordering Guide

Model	#CHs/ k Ohm	Temp Range	Package Description	Package Option
AD5235BRU25	X2/25	$-40/+85^\circ\text{C}$	TSSOP-16	RU-16
AD5235BRU250	X2/250	$-40/+85^\circ\text{C}$	TSSOP-16	RU-16

The AD5235 contains 16,000 transistors.
Die size: 100 x 105 mil = 10,500 sq. mil

AD5235 PIN CONFIGURATION



AD5235 PIN FUNCTION DESCRIPTION

#	Name	Description
1	CLK	Serial Input Register clock pin. Shifts in one bit at a time on positive clock edges.
2	SDI	Serial Data Input Pin. Shifts in one bit at a time on positive clock CLK edges.
3	SDO	Serial Data Output Pin. Open Drain Output requires external pull-up resistor. Commands 9 and 10 activate the SDO output. See Instruction operation Truth Table. Table 2.
4	GND	Ground pin, logic ground reference
5	V_{SS}	Negative Supply. Connect to zero volts for single supply applications.
6	A1	A terminal of RDAC1.
7	W1	Wiper terminal of RDAC1, ADDR(RDAC1) = 0_H .
8	B1	B terminal of RDAC1.
9	B2	B terminal of RDAC2.
10	W2	Wiper terminal of RDAC2, ADDR(RDAC3) = 1_H .
11	A2	A terminal of RDAC2.
12	V_{DD}	Positive Power Supply Pin. Should be \geq the input-logic HIGH voltage.
13	\overline{WP}	Write Protect Pin. Prevents any changes to the present EEMEM contents when active low.
14	\overline{PR}	Hardware over ride preset pin. Refreshes the scratch pad register with current contents of the EEMEM register. Factory default loads midscale 512_{10} .
15	\overline{CS}	Serial Register chip select active low. Serial register operation takes place when \overline{CS} returns to logic high.
16	RDY	Ready. Active-high open drain output. Identifies completion of commands 2, 3, 8, 9, 10.

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OPERATIONAL OVERVIEW

The AD5235 digital potentiometer is designed to operate as a true variable resistor replacement device for analog signals that remain within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$. The basic voltage range is limited to a $V_{DD} - V_{SS} < 5.5V$. Control of the digital potentiometer allows both scratch pad register (RDAC register) changes to be made, as well as 100,000 times of nonvolatile electrically erasable memory (EEMEM) register operations. The EEMEM update process takes approximately 20.2ms, during this time the shift register is locked preventing any changes from taking place. The RDY pin flags the completion of this EEMEM save. The EEMEM retention is designed to last 10 years without refresh. The scratch pad register can be changed incrementally by using the software controlled Increment/Decrement instruction or the Shift Left/Right instruction command. Once an Increment, Decrement or Shift command has been loaded into the shift register, subsequent CS strobes will repeat this command. This is useful for push button control applications. Alternately the scratch pad register can be programmed with any position value using the standard SPI serial interface mode by loading the representative data word. The scratch pad register can be loaded with the current contents of the nonvolatile EEMEM register under the program control. At system power ON, the default value of the scratch pad memory is the value previously saved in the EEMEM register. The factory EEMEM preset value is midscale 512₁₀.

A serial data output pin is available for daisy chaining and for readout of the internal register contents. The serial input data register uses a 24-bit instruction/address/data WORD. The write-protect (\overline{WP}) pin provides a hardware EEMEM protection feature disabling any changes of the present EEMEM contents.

SERIAL DATA INTERFACE

The AD5235 contains a four-wire SPI compatible digital interface (SDI, SDO, \overline{CS} , and CLK). Key features of this interface include:

- Independently Programmable Read & Write to all registers
- Direct parallel refresh of all RDAC wiper registers from corresponding EEMEM registers

- Permanent storage of the present scratch pad RDAC register values into the corresponding EEMEM register
- 30 bytes of user addressable electrical-erasable memory

The serial interface of AD5235 digital potentiometer uses a 24-bit serial word loaded with MSB first. The format of the SPI compatible word is shown in Table 1. The Command Bits (Cx) control the operation of the digital potentiometer according to the command instruction shown in Table 2. The Address Bits (Ax) determine which register is activated. The Data Bits (Dx) are the values that are loaded into the decoded register. The last instruction executed prior to a period of no programming activity should be the NOP instruction. This will place the internal logic circuitry in a minimum power dissipation state.

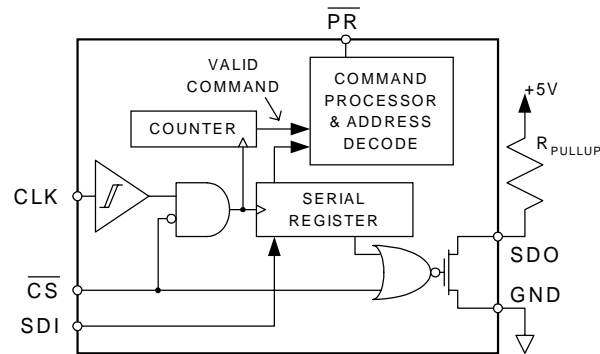


Figure 2. Equivalent Digital Input-Output Logic

The equivalent serial data input and output logic is shown in figure 2. The open drain output SDO is disabled whenever chip select \overline{CS} is logic high. The SPI interface can be used in two slave modes CPHA=1, CPOL=1 and CPHA=0, CPOL=0. CPHA and CPOL refer to the control bits, which dictate SPI timing in the following microprocessors/MicroConverters: ADuC812/824, M68HC11, and MC68HC16R1/916R1.

Table 1. AD5235 24-bit Serial Data Word

	M	S	B																					L	S	B
AD5235	C3	C2	C1	C0	A3	A2	A1	A0	X	X	X	X	X	X	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		

Command bits are identified as Cx, address bits are Ax, and data bits are Dx. Command instruction codes are defined in table 2.

Table 2. AD5235 Instruction/Operation Truth Table

Inst No.	Instruction Byte 1 B15 B8 C3 C2 C1 C0 A3 A2 A1 A0	Data Byte 1 B15 B8 X ... D9 D8	Data Byte 0 B7 ... B0 D7 ... D0	Operation
0	0 0 0 0 X X X X	X ... X X	X ... X	NOP: Do nothing
1	0 0 0 1 << ADDR >>	X ... X X	X ... X	Write contents of EEMEM(ADDR) to RDAC(ADDR) Register
2	0 0 1 0 << ADDR >>	X ... X X	X ... X	SAVE WIPER SETTING: Write contents of RDAC(ADDR) to EEMEM(ADDR)
3	0 0 1 1 << ADDR >>	X ... D9 D8	D7 ... D0	Write contents of Serial Register Data Byte 0 & 1 to EEMEM(ADDR)
4	0 1 0 0 << ADDR >>	X ... X X	X ... X	DEC 6dB: Right Shift contents of RDAC(ADDR) , LSB rolls over to MSB position
5	0 1 0 1 X X X X	X ... X X	X ... X	DEC All 6dB: Right Shift contents of all RDAC Registers, LSB rolls over to MSB position
6	0 1 1 0 << ADDR >>	X ... X X	X ... X	Decrement contents of RDAC(ADDR) by One, does not rollover at zero-scale
7	0 1 1 1 X X X X	X ... X X	X ... X	Decrement contents of all RDAC Registers by One, does not rollover at zero-scale
8	1 0 0 0 0 0 0 0	X ... X X	X ... X	RESET: Load all RDACs with their corresponding EEMEM previously-saved values
9	1 0 0 1 << ADDR >>	X ... X X	X ... X	Write contents of EEMEM(ADDR) to Serial Register Data Byte 0 & 1
10	1 0 1 0 << ADDR >>	X ... X X	X ... X	Write contents of RDAC(ADDR) to Serial Register Data Byte 0 & 1
11	1 0 1 1 << ADDR >>	X ... D9 D8	D7 ... D0	Write contents of Serial Register Data Byte 0 & 1 to RDAC(ADDR)
12	1 1 0 0 << ADDR >>	X ... X X	X ... X	INC 6dB: Left Shift contents of RDAC(ADDR), stops at all 'Ones'.
13	1 1 0 1 X X X X	X ... X X	X ... X	INC All 6dB: Right Shift contents of all RDAC Registers, stops at all 'Ones'.
14	1 1 1 0 << ADDR >>	X ... X X	X ... X	Increment contents of RDAC(ADDR) by One, does not rollover at full-scale stops at all 'Ones'.
15	1 1 1 1 X X X X	X ... X X	X ... X	Increment contents of all RDAC Registers by One, does not rollover at full-scale stops at all 'Ones'.

NOTES:

1. The SDO output shifts-out the last 24-bits of data clocked into the serial register for daisy chain operation. Exception, following Instruction #9 or #10 the selected internal register data will be present in data byte 0 & 1. Instructions following #9 & #10 must be a full 24-bit data word to completely clock out the contents of the serial register.
2. The RDAC register is a volatile scratch pad register that is refreshed at power ON from the corresponding non-volatile EEMEM register.
3. The increment, decrement and shift commands ignore the contents of the shift register Data Byte 0.
4. Execution of the Operation column noted in the table takes place when the \overline{CS} strobe returns to logic high.

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Detail Potentiometer Operation

The actual structure of the RDAC is designed to emulate the performance of a mechanical potentiometer. The RDAC contains a string of connected resistor segments, with an array of analog switches that act as the wiper connection to several points along the resistor array. The number of points is the resolution of the device. The AD5235 has 1024 connection points allowing it to provide better than 0.5% set-ability resolution. Figure 3 provides an equivalent diagram of the connections between the three terminals that make up one channel of the RDAC. The SW_A and SW_B will always be ON while one of the switches $SW(0)$ to $SW(2^N-1)$ will be ON one at a time depends upon the resistance step decoded from the Data Bits. Note that there are two 50Ω wiper resistances, R_W . The resistance contributed by R_W must be accounted for when calculating the output resistance. R_W is the sum of the resistances of $SW_A + SW_X$ and $SW_B + SW_X$ for A-to-Wiper and B-to-Wiper respectively.

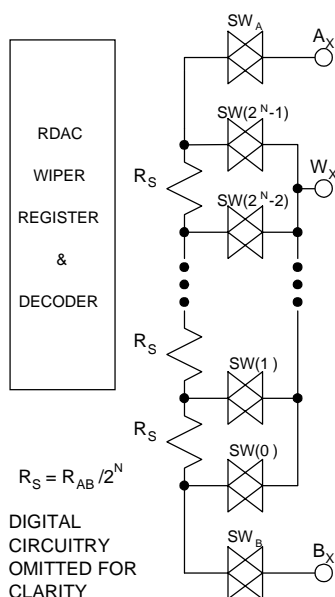


Figure 3. Equivalent RDAC structure

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between terminals A and B are available with values of $25K\Omega$, and $250K\Omega$. The final digits of the part number determine the nominal resistance value, e.g., $25K\Omega = 25$; $250K\Omega = 250$. The nominal resistance (R_{AB}) of the AD5235 VR has 1024 contact points accessed by the wiper terminal, plus the B terminal contact. The 10-bit data word in the RDAC latch is decoded to select one of the 1024 possible settings. The wiper's first connection starts at the B terminal for data 00_H . This B-terminal connection has a wiper contact resistance, R_W of 50Ω , regardless of what the nominal resistance R_{AB} is. The second connection ($25K\Omega$ part) is the first tap point where $R_{WB} = 74\Omega$ [$R_{WB} = R_{AB}/1024 + R_W = 24\Omega + 50\Omega$] for data 01_H . The third connection is the next tap point representing $R_{WB} = 49 + 50 = 99\Omega$ for data 02_H . Each LSB data value increase moves the wiper up the resistor

ladder until the last tap point is reached at $R_{WB} = 25025\Omega$. See figure 3 for a simplified diagram of the equivalent RDAC circuit.

The general equation, which determines the digitally programmed output resistance between W_X and B_X , is:

$$R_{WB}(D_x) = (D_x/2^N) * R_{AB} + R_W \quad \text{eqn. 1}$$

Where N is the resolution of the VR, D_x is the data contained in the $RDAC_x$ latch, and R_{AB} is the nominal end-to-end resistance. Since $N=10$ and $R_W=50\Omega$ for AD5235, eqn. 1 becomes:

$$R_{WB}(D_x) = (D_x/1024) * R_{AB} + 50\Omega \quad \text{eqn. 2}$$

For example, when $V_B = 0V$ and A-terminal is open circuit the following output resistance values will be set for the following RDAC latch codes (applies to $R_{AB}=25K\Omega$ potentiometers):

D_x (DEC)	R_{WB} (Ω)	Output State
1023	25025Ω	Full-Scale
512	12500Ω	Mid-Scale
1	74Ω	1 LSB
0	50Ω	Zero-Scale (Wiper contact resistance)

Note that in the zero-scale condition a finite wiper resistance of 50Ω is present. Care should be taken to limit the current flow between W and B in this state to no more than 20mA to avoid degradation or possible destruction of the internal switch contact.

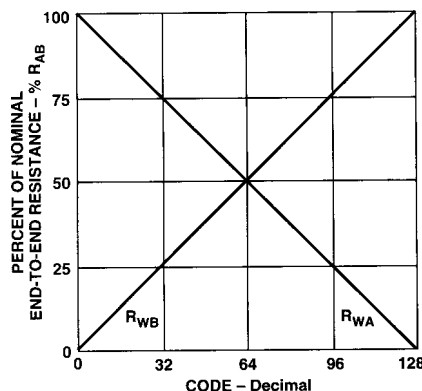


Figure 4. Symmetrical RDAC Operation

Like the mechanical potentiometer the RDAC replaces, the AD5235 part is totally symmetrical. The resistance between the wiper W and terminal A also produces a digitally controlled resistance R_{WA} . Figure 4 shows the symmetrical programmability of the various terminal connections. When these terminals are used, the B-terminal should be tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value. The general equation for this operation is:

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$$R_{WA}(Dx) = \left[(2^N - Dx) / 2^N \right] * R_{AB} + R_W \quad \text{eqn. 3}$$

ESD PROTECTION CIRCUITS

Similarly, eqn. 3 becomes:

$$R_{WA}(Dx) = \left[(1024 - Dx) / 1024 \right] * R_{AB} + 50\Omega \quad \text{eqn. 4}$$

For example, when $V_A = 0V$ and B-terminal is tied to the wiper W the following output resistance values will be set for the following RDAC latch codes (applies to $R_{AB}=10K\Omega$ potentiometers):

Dx (DEC)	R_{WA} (Ω)	Output State
1023	74	Full-Scale
512	12500	Mid-Scale
1	25000	1 LSB
0	25050	Zero-Scale

A $\pm 1\%$ typical distribution of R_{AB} from channel-to-channel occurs within the same package. On the other hand, device to device matching is process lot dependent such that a maximum of $\pm 30\%$ variation is possible. The change in R_{AB} with temperature has a 50 ppm/ $^{\circ}C$ temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates an output voltage proportional to the input voltage applied to a given terminal. For example connecting A-terminal to +5V and B-terminal to ground produces an output voltage at the wiper which can be any value starting at zero volts and up to 1 LSB less than +5V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 2^N resolution of the potentiometer divider. The general equation defining the output voltage with respect to ground for any given input voltage applied to terminals AB is:

$$V_W(Dx) = Dx / 2^N * V_{AB} + V_B \quad \text{eqn. 5}$$

Since $N=10$,

$$V_W(Dx) = (Dx / 1024) * V_{AB} + V_B \quad \text{eqn. 6}$$

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Here the output voltage is dependent on the ratio of the internal resistors and not the absolute value. Therefore, the drift reduces to 15ppm/ $^{\circ}C$.

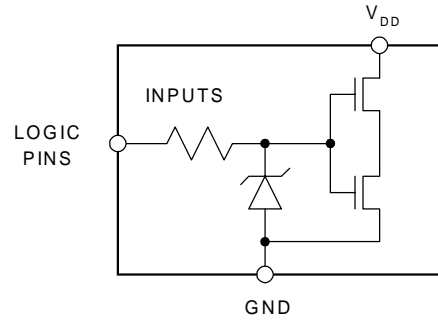


Figure 5A. Equivalent Digital Input ESD Protection

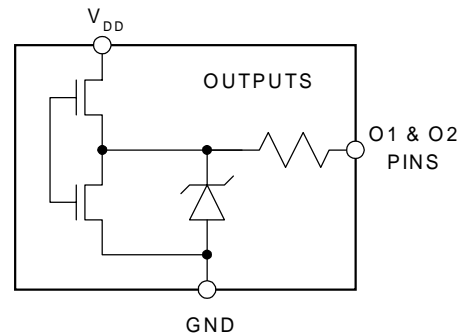


Figure 5B. Equivalent Digital Output ESD Protection

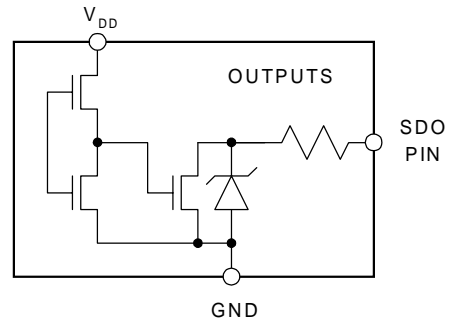


Figure 5C. Equivalent SDO Output ESD Protection Circuit

Figure 5 shows the equivalent ESD protection circuit for digital pins. Figure 6 shows the equivalent analog-terminal protection circuit for the variable resistors.

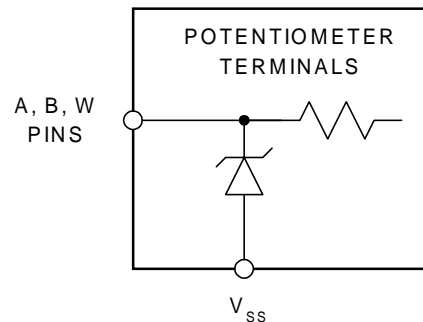


Figure 6. Equivalent VR-Terminal ESD Protection

Nonvolatile Memory Digital Potentiometers

AD5235

TEST CIRCUITS

Figures 7 to 15 define the test conditions used in the product specification's table.

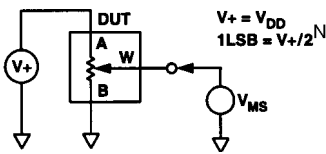


Figure 7. Potentiometer Divider Nonlinearity error test circuit (INL, DNL)

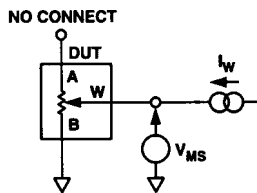


Figure 8. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

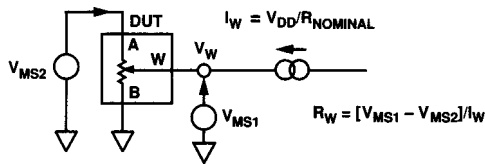


Figure 9. Wiper Resistance test Circuit

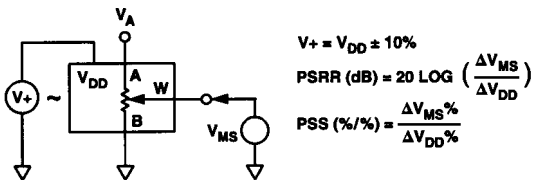


Figure 10. Power supply sensitivity test circuit (PSS, PSSR)

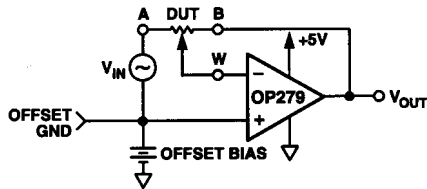


Figure 11. Inverting Gain test Circuit

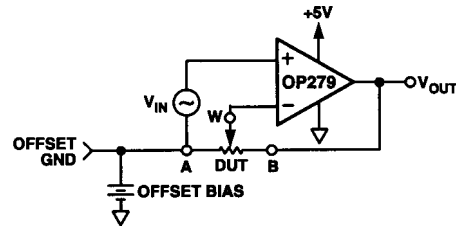


Figure 12. Non-Inverting Gain test circuit

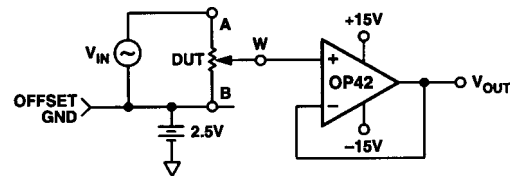


Figure 13. Gain Vs Frequency test circuit

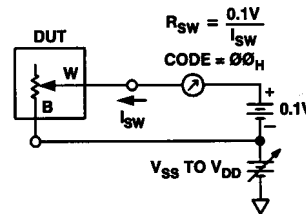


Figure 14. Incremental ON Resistance Test Circuit

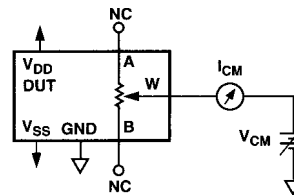


Figure 15. Common Mode Leakage current test circuit

TYPICAL PERFORMANCE GRAPHS

TBD

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

16-Lead TSSOP (RU-16)

