Twos Complement, Dual 12-Bit DAC with Internal REF and Fast Settling Time

AD5399

FEATURES

2-channel 12-bit DAC
Twos complement facilitates bipolar applications
Bipolar zero with 2 V dc offset
Built-in 2.000 V precision reference with 10 ppm/°C typ TC
Buffered voltage output: 0 V to 4 V
Single-supply operation: 4.5 V to 5.5 V
Fast 0.8 µs settling time typ
Ultracompact MSOP-10 package
Monotonic DNL < ±1 LSB
Optimized accuracy at zero scale
Power-on reset to V_{REF}
3-wire serial data input
Extended temperature range: –40°C to +105°C

APPLICATIONS

Single-supply bipolar converter operations
General-purpose DSP applications
Digital gain and offset controls
Instrumentation level settings
Disk drive control
Precision motor control

GENERAL DESCRIPTION

The AD5399 is the industry-first dual 12-bit digital-to-analog converter that accepts twos complement digital coding with 2 V dc offset for single-supply operation. Augmented with a built-in precision reference and a solid buffer amplifier, the AD5399 is the smallest self-contained 12-bit precision DAC that fits many general-purpose as well as DSP specific applications. The twos complement programming facilitates the natural coding implementation commonly found in DSP applications, and allows operation in single supply. The AD5399 provides a 2 V reference output, V_{REF}, for bipolar zero monitoring. It can also be used for other on-board components that require a precision reference. The device is specified for operation from 5 V ± 10% single supply with bipolar output swing from 0 V to 4 V centered at 2 V.

The AD5399 is available in the compact 1.1 mm low profile MSOP-10 package. All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +105°C.

FUNCTIONAL BLOCK DIAGRAM

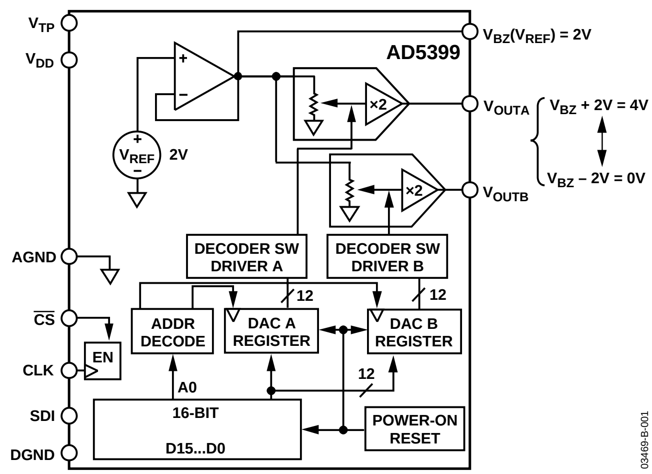

Figure 1.

$V_{OUT} = ((D – 2048)/4096 \times 4\text{ V}) + 2\text{ V}$ for $0 \le D \le 4095$, where D is the decimal code.

Table 1. Examples of Twos Complement Codes

Twos Complement	D	Scale	V_{OUT} (V)
2047	4095	+FS	4.000
2046	4094	+FS – 1 LSB	3.999
1	2049	BZS + 1 LSB	2.001
0	2048	BZS	2.000
4095	2047	BZS – 1 LSB	1.999
2049	1	–FS + 1 LSB	0.001
2048	0	–FS	0.000

FS = Full Scale, BZS = Bipolar Zero Scale.

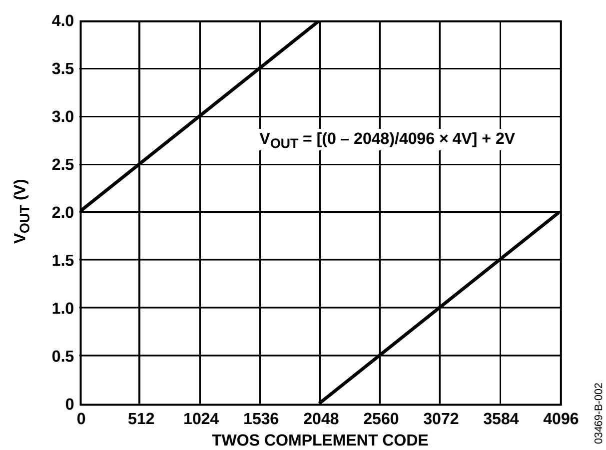

Figure 2. Output vs. Twos Complement Code

Rev. D

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

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Added Power-Up/Power-Down section 10

3/03—Data sheet changed from Rev. 0 to Rev. A

Change to Table 1 1

2/03—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} = 5 V ± 10%, −40°C < T_A < +105°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS						
Resolution	N		12			Bits
Differential Nonlinearity Error	DNL		−1	±0.5	+1	LSB
		Codes 2048 to 2052, due to int. op amp offset	−1.2	±0.5	+1.2	LSB
Integral Nonlinearity Error	INL		−0.4	±0.02	+0.4	%FS
Positive Full-Scale Error	V_{+FSE}	Code = 0xF	−0.75	−0.15	+0.75	%FS
Bipolar Zero-Scale Error	V_{BZSE}	Code = 0x000	−0.75	−0.15	+0.75	%FS
Negative Full-Scale Error	V_{-FSE}	Code = 0x800	−0.75	−0.15	+0.75	%FS
ANALOG OUTPUTS						
Nominal Positive Full-Scale	$V_{OUTA/B}$	Code = 0x7FF		4		V
Positive Full-Scale Tempco[2]	$TCV_{OUTA/B}$	Code = 0x7FF, T_A = 0°C to 70°C	−40	±10	+40	ppm/°C
		Code = 0xFF, T_A = −40°C to +105°C	−60	±10	+60	ppm/°C
Nominal V_{BZ} Output Voltage	V_{BZ}		1.995	2.000	2.004	V
Bipolar Zero Output Resistance[2]	R_{BZ}			1		Ω
V_{BZ} Output Voltage Tempco	TCV_{BZ}	T_A = 0°C to 70°C	−40	±10	+40	ppm/°C
		T_A = −40°C to +105°C	−60	±10	+60	ppm/°C
Nominal Peak-to-Peak Output Swing	$\|V_{+FS}\| + \|V_{-FS}\|$	Code 0x7FF to Code 0x800		4		V
DIGITAL INPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V, V_{DD} = 5 V			±1	µA
Input Capacitance[2]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		4.5		5.5	V
Supply Current	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = 0 V		1.8	2.6	mA
Supply Current in Shutdown	I_{DD_SHDN}	$V_{IH} = V_{DD}$ or V_{IL} = 0 V, B14 = 0, T_A = 0°C to 105°C		10	100	µA
		$V_{IH} = V_{DD}$ or V_{IL} = 0 V, B14 = 0, T_A = −40°C to 0°C		100	500	µA
Power Dissipation[3]	P_{DISS}	$V_{IH} = V_{DD}$ or V_{IL} = 0 V, V_{DD} = 5.5 V		9	13	mW
Power Supply Sensitivity	P_{SS}	ΔV_{DD} = 5 V ± 10%	−0.006	+0.003	+0.006	%/%
DYNAMIC CHARACTERISTICS[2]						
Settling Time	t_S	0.1% error band		0.8		µs
Digital Feedthrough	Q			10		nV-s
Bipolar Zero-Scale Glitch	G			10		nV-s
Capacitive Load Driving Capability	CL	No oscillation			1000	pF
INTERFACE TIMING CHARACTERISTICS[2, 4]						
SCLK Cycle Frequency	t_{CYC}				33	MHz
SCLK Clock Cycle Time	t_1		30			ns
Input Clock Pulse Width	t_2, t_3	Clock level low or high	15			ns
Data Setup Time	t_4		5			ns
Data Hold Time	t_5		0			ns
$\overline{CS}$ to SCLK Active Edge Setup Time	t_6		5			ns
SCLK to $\overline{CS}$ Hold Time	t_7		0			ns
Repeat Programming, $\overline{CS}$ High Time	t_8		30			ns

[1] Typical values represent average readings at 25°C and V_{DD} = 5 V.
[2] Guaranteed by design and not subject to production test.
[3] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[4] See timing diagram (Figure 5) for location of measured values. All input control voltages are specified with $t_R = t_F$ = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using V_{DD} = 5 V. Input logic should have a 1 V/µs minimum slew rate.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	–0.3 V, +7.5 V
V_{OUTA}, V_{OUTB}, V_{BZ} to GND	0 V, V_{DD}
Digital Input Voltages to GND	0 V, V_{DD} + 0.3 V
Operating Temperature Range	–40°C to +105°C
Maximum Junction Temperature ($T_{J\ MAX}$)	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Package Power Dissipation	$(T_{J\ MAX} – T_A)/\theta_{JA}$
Thermal Resistance, θ_{JA}, MSOP-10	206°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

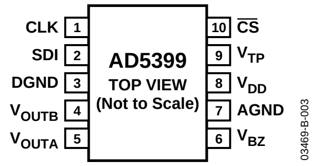

Figure 3. MSOP-10 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Serial Clock Input. Positive edge triggered.
2	SDI	Serial Data Input. MSB first format.
3	DGND	Digital Ground.
4	V_{OUTB}	DAC B Voltage Output (A0 = Logic 1).
5	V_{OUTA}	DAC A Voltage Output (A0 = Logic 0).
6	V_{BZ}	2 V, Virtual Bipolar Zero (Active Output).
7	AGND	Analog Ground.
8	V_{DD}	Positive Power Supply. Specified for operation at 5 V.
9	V_{TP}	Connect to V_{DD}. Reserved for factory testing.
10	$\overline{CS}$	Chip Select (Frame Sync Input). Allows clock and data to shift into the shift register when $\overline{CS}$ goes from high to low. After the 16^{th} clock pulse, it is not necessary to bring $\overline{CS}$ high to shift the data to the output. However, $\overline{CS}$ should be brought high any time after the 16th clock positive edge in order to allow the next programming cycle.

Table 5. Serial Data-Word Format

ADDR				DATA						
B15	B14	B13	B12	B11	B10	…	B3	B2	B1	B0
A0	X	SD	0	D11	D10	…	D3	D2	D1	D0
MSB										LSB

A0	Address Bit. Logic low selects DAC A and logic high selects DAC B. Both channels are shut down when the SD bit is high. However, the A0 bit must be at the same state for shutdown activation and deactivation. See the Shutdown Function section.
X	Don't Care.
SD	Shutdown Bit. Logic high puts both DAC outputs and V_{BZ} into high impedance. A0 bit must be at the same state for shutdown activation and deactivation.
0	B12 must be 0.
D0–D11	Data Bits.

TIMING CHARACTERISTICS

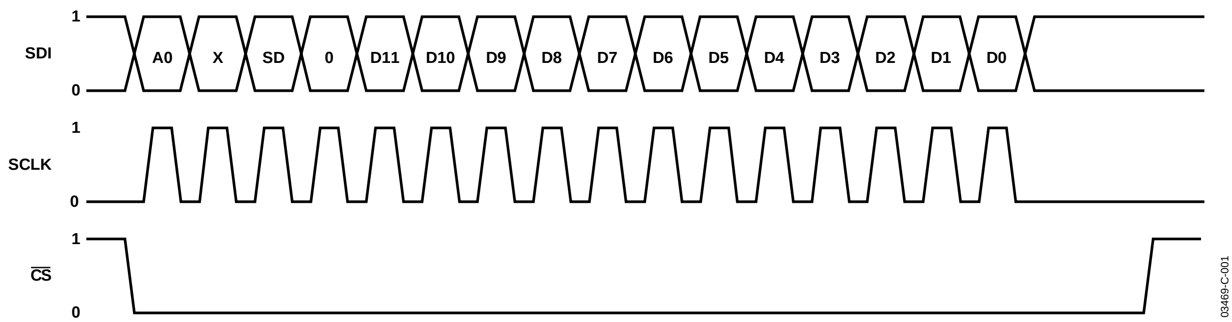

Figure 4. Timing Diagram

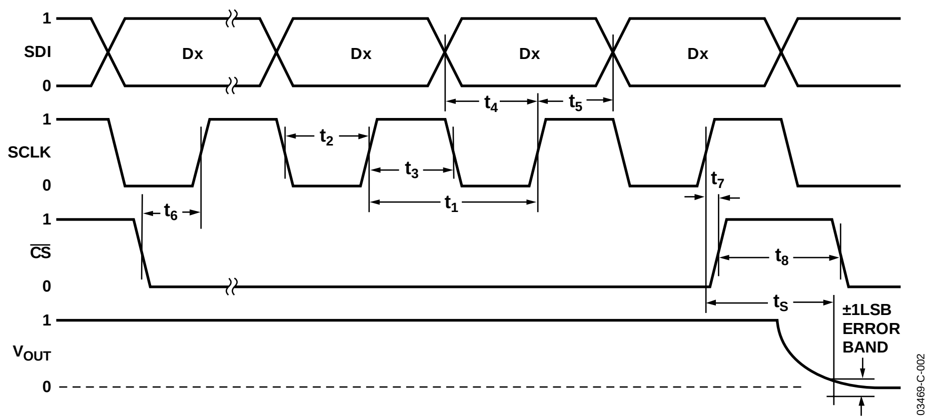

Figure 5. Detailed Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

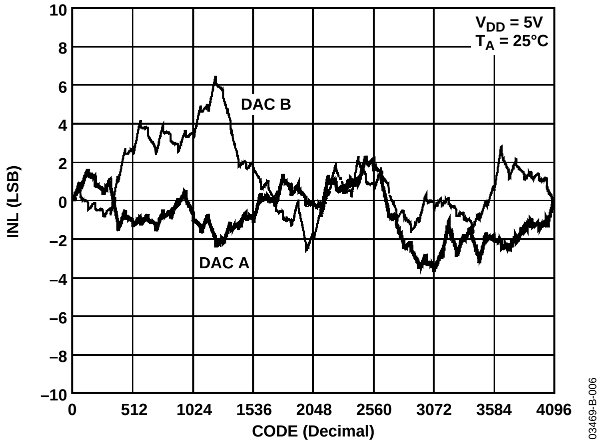

Figure 6. Integral Nonlinearity Errors

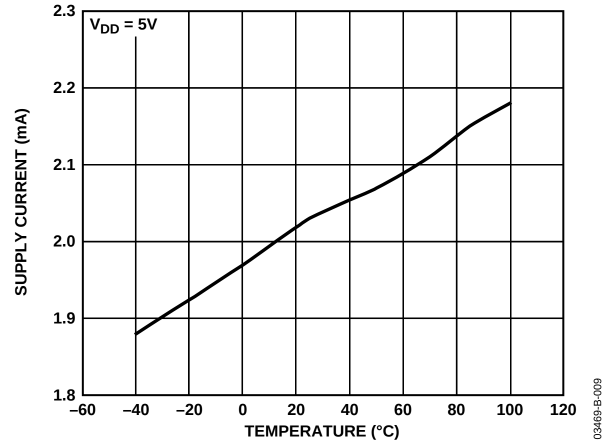

Figure 9. Supply Current vs. Temperature

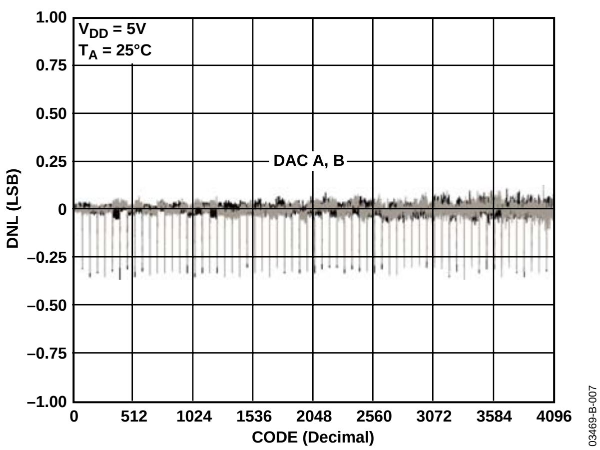

Figure 7. Differential Nonlinearity Errors

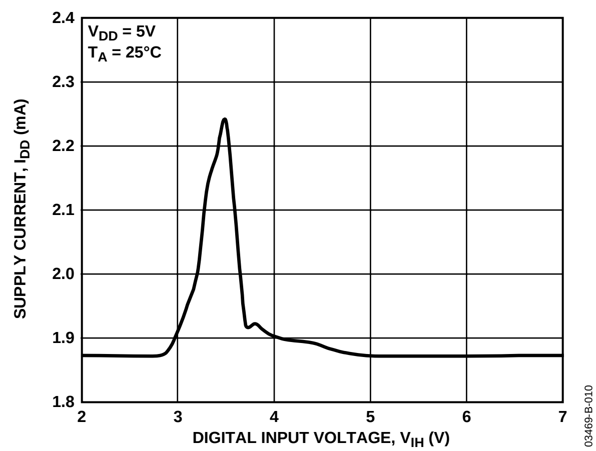

Figure 10. Supply Current vs. Digital Input Voltage

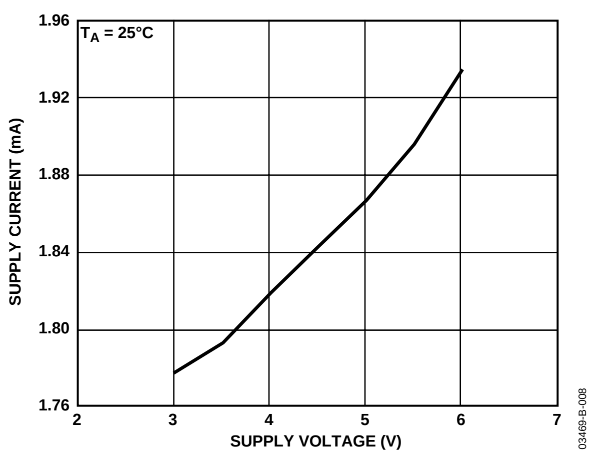

Figure 8. Supply Current vs. Supply Voltage

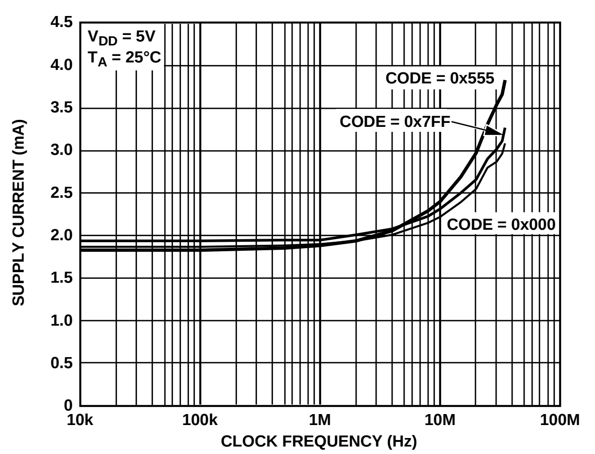

Figure 11. Supply Current vs. Clock Frequency

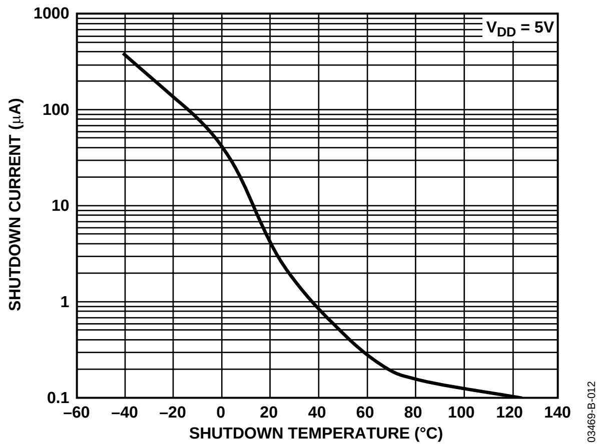

Figure 12. Shutdown Current vs. Temperature

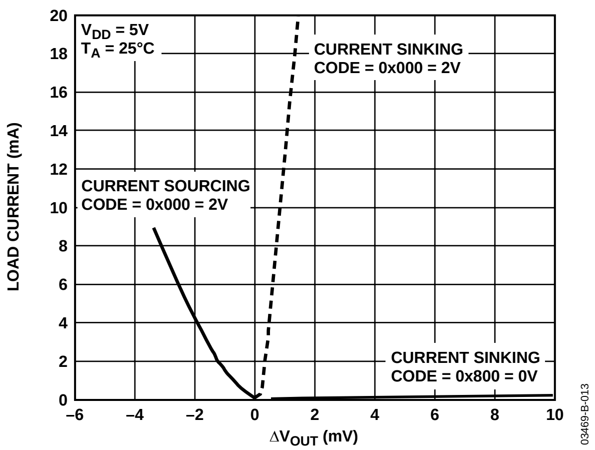

Figure 13. Load Current vs. Voltage Drop

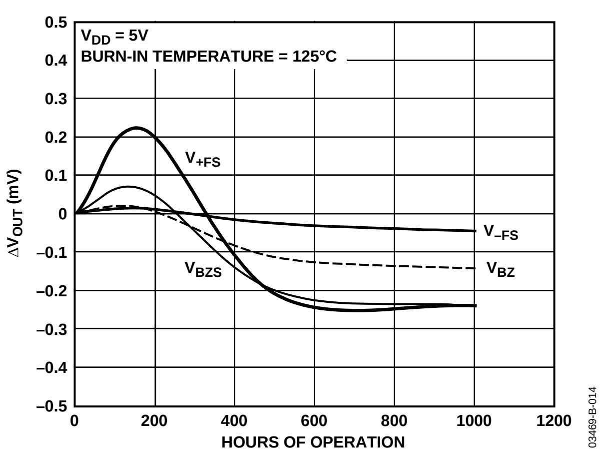

Figure 14. Long-Term Drift

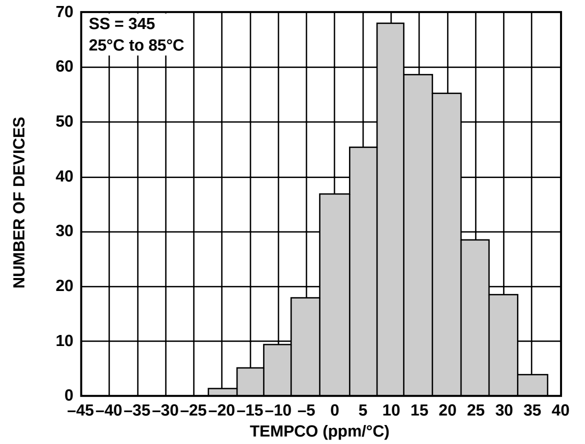

Figure 15. V_{BZ} Temperature Coefficient (T_A = 25°C to 85°C)

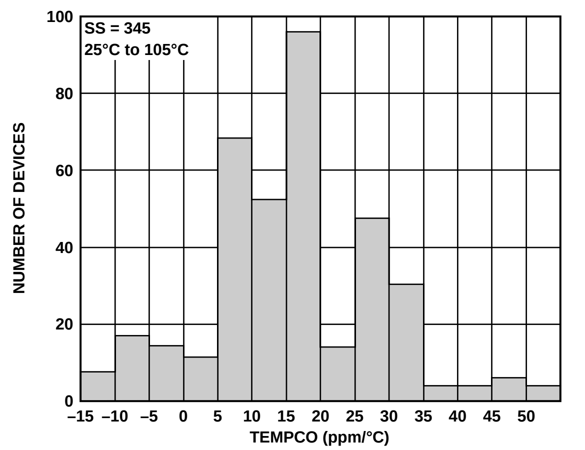

Figure 16. V_{BZ} Temperature Coefficient (T_A = 25°C to 105°C)

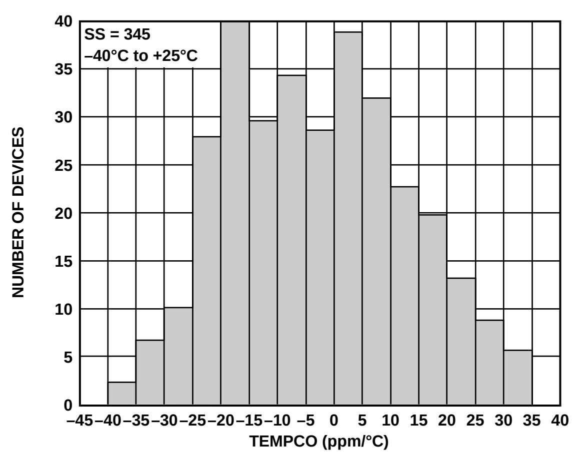

Figure 17. V_{BZ} Temperature Coefficient (T_A = –40°C to +25°C)

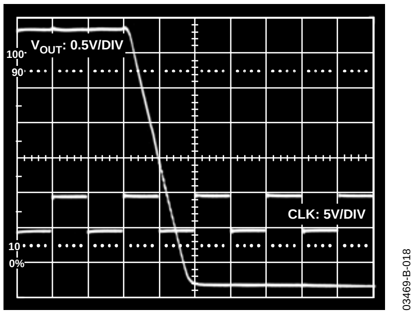

Figure 18. Large Signal Settling (0.5 µs/DIV)

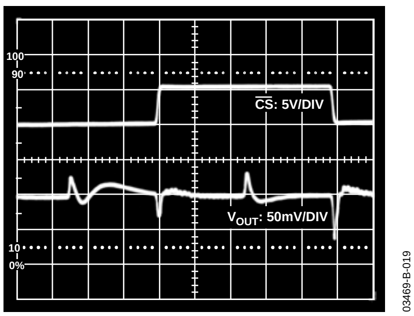

Figure 19. Midscale Glitch and Digital Feedthrough (2 µs/DIV)

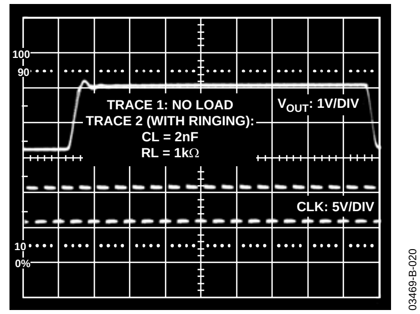

Figure 20. Capacitive Load Output Performance (2 µs/DIV)

OPERATION

The AD5399 provides a 12-bit, twos complement, dual voltage output, digital-to-analog converter (DAC). It has an internal reference with 2 V bipolar zero dc offset, where $0 \leq V_{OUT} \leq 4$ V.

The output transfer equation is

$$V_{OUT} = ((D - 2048)/4096 \times 4\ \text{V}) + 2\ \text{V}$$

where:
D is the 12-bit decimal code and not the twos complement code.
V_{OUT} is with respect to ground.

In data programming, the data is loaded MSB first on the positive clock edge (SCLK) after chip select ($\overline{CS}$) goes from high to low. The digital word is 16 bits wide, with the MSB, B15, as an address bit (DAC A: A0 = 0; DAC B: A0 = 1). B14 is don't care, B13 is a shutdown bit, B12 must be logic low, and the last 12 bits are data bits. An internal counter allows data transferred from the shift register to the output after the 16th positive clock edge while $\overline{CS}$ stays low (see Figure 5). After the 16th clock pulse, it is not necessary to bring $\overline{CS}$ high to shift the data to the output. However, $\overline{CS}$ should be brought high anytime after the 16th clock positive edge in order to allow the next programming cycle.

Table 6. Input Logic Control Truth Table

CLK	$\overline{CS}$	Register Activity
L	H	No Shift Register Effect
H	H	No Shift Register Effect
P	L	Shift One SDI Bit into the SR
16th P	L	Transfer SR Data into DAC Register and Update the Output

P = Positive Edge, X = Don't Care, SR = Shift Register.

The data setup and data hold times in the Specifications table determine the timing requirements. The internal power-on reset circuit clears the serial input registers to all 0s, and sets the two DAC registers to a V_{BZ} (zero code) of 2 V.

Software shutdown B13 turns off the internal REF and amplifiers. The output is close to zero potential, and the digital circuitry remains active such that new data can be written. Therefore, the DAC register is refreshed with the new data once the shutdown bit is deactivated.

All digital inputs are ESD protected with a series input resistor and parallel Zener, as shown in Figure 21, that apply to digital input pins CLK, SDA, and $\overline{CS}$. The basic connection is shown in Figure 22.

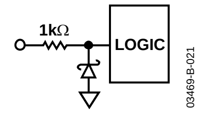

Figure 21. Equivalent ESD Protection Circuit

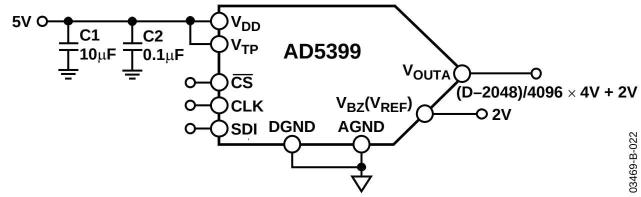

Figure 22. Basic Connection

POWER-UP/POWER-DOWN SEQUENCE

Like most CMOS devices, it is recommended to power V_{DD} and ground prior to any digital signals. The ideal power-up sequence is GND, V_{DD}, and digital signals. The reverse sequence applies to the power-down condition.

Layout and Power Supply Bypassing

It is a good practice to employ compact, minimum lead-length layout design. The input leads should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 µF to 0.1 µF disc or chip ceramic capacitors. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at V_{DD} to minimize any transient disturbance and to filter any low frequency ripple (see Figure 23). Users should not apply switching regulators for V_{DD} due to the power supply rejection ratio degradation over frequency.

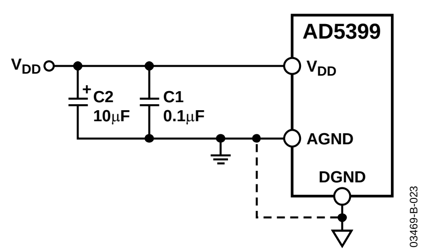

Figure 23. Power Supply Bypassing and Grounding Connection

Grounding

The DGND and AGND pins of the AD5399 refer to the digital and analog ground references. To minimize the digital ground bounce, the DGND terminal should be joined remotely at a single point to the analog ground plane, as shown in Figure 23.

Shutdown Function

The AD5399 shutdown function allows both DACs to be shutdown simultaneously. However, the A0 and SD bits work in tandem, and the A0 logic state must be the same for shutdown activation and deactivation (see Table 7).

Table 7. Shutdown Activation and Deactivation Sequence.

Sequence of Events	Data-Word in Binary	Shutdown Status
1	0X10 XXXX XXXX XXXX	Activate shutdown on both DACs.
2	1X00 XXXX XXXX XXXX	Both DACs remain at shutdown.
3	0X00 XXXX XXXX XXXX	Deactivate shutdown. Both DACs resume normal operation.

The A0 bit (MSB) must be in the same state when activating and deactivating shutdown.

For users whose logic signals may be in three-state (random levels) during power-up initialization, it is recommended to put a pull-up resistor at the $\overline{CS}$ pin to disable chip select (Figure 24). This avoids inadvertent shutdown as well as the inability to deactivate shutdown due to an unknown A0 state. The resistor value depends on the digital controller's output impedance.

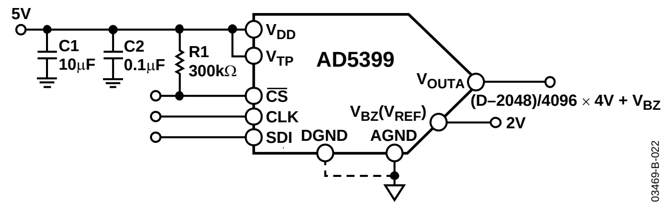

Figure 24. Disable $\overline{CS}$ for Random Logic Mode

OUTLINE DIMENSIONS

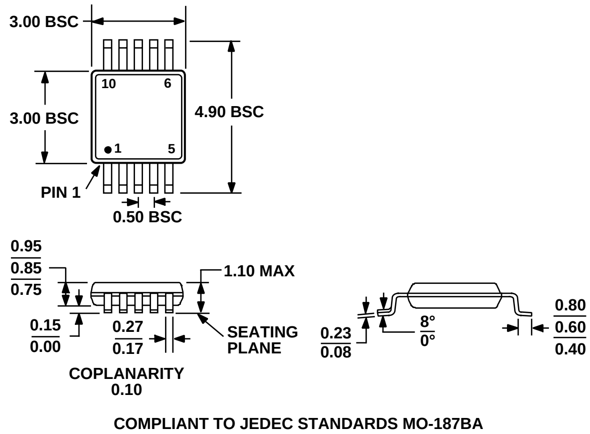

Figure 25. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Models	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
AD5399YRM	–40°C to +105°C	MSOP	RM-10	DSB	50
AD5399YRM-REEL7	–40°C to +105°C	MSOP	RM-10	DSB	1,000

C03469–0–6/04(D)