



DNC5X3125 Gigabit Ethernet Transceiver Macrocell

Overview

The DNC5X3125 is a low-cost, low-power transceiver macrocell. It is used for data transmission over fiber or coaxial media in conformance with *IEEE** 802.3z Gigabit Ethernet specification and Fibre Channel *ANSI*† X3T11 at 1.0 Gbits/s and 1.25 Gbits/s.

The transmitter section accepts parallel 10-bit 8b/10b encoded data that is latched on the rising edge of TBC. It also accepts the low-speed, TTL compatible system clock, REFCLK, and uses this clock to synthesize the internal high-speed serial bit clock. The serialized data is then available at the differential PECL outputs, terminated in 50 Ω or 75 Ω to drive either an optical transmitter or coaxial media.

The receive section receives high-speed serial data at its differential PECL input port. This data is fed to the digital clock recovery section, which generates a recovered clock and retimes the data. The retimed data is deserialized and presented as 10-bit parallel data on the output port. A divided-down version of the recovered clock, synchronous with parallel data bytes, is also available as a TTL compatible output. The receive section recognizes the comma character and aligns the comma-containing byte on the word boundary, when ENCDT = 1.

Features

- Designed to operate in Ethernet, fibre channel, *FireWire*‡ or backplane applications.
- Operationally compliant to *IEEE* 802.3z Gigabit Ethernet specification.
- Operationally compliant to Fibre Channel *ANSI* X3T11. Provides FC-0 services at 1.0 Gbits/s—1.25 Gbits/s (10-bit encoded data rate).
- 100 MHz—125 MHz differential or single-ended reference clock.
- 10-bit parallel interface.
- 8b/10b encoded data.
- High-speed comma character recognition (K28.1, K28.5, K28.7) for latency-sensitive applications and alignment to word boundary.
- Two 50.0 MHz—62.5 MHz receive-byte clocks.
- Single analog PLL design requires no external components for the frequency synthesizer.
- Novel digital data lock in receiver avoids the need for multiple analog PLLs.
- Expandable beyond single-channel SERDES.
- PECL high-speed interface I/O for use with optical transceiver or coaxial copper media.
- Requires one external resistor for PECL output reference level definition.
- Low-power digital 0.25 μ m CMOS technology.
- 3.3 V \pm 5% power supply.
- 0 °C—70 °C ambient temperature.

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† *ANSI* is a registered trademark of American National Standards Institute.

‡ *FireWire* is a registered trademark of Apple Computer, Inc.

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Functional Description

The DNC5X3125 transceiver provides for data transmission over fiber or coaxial media at 1.0 Gbits/s to 1.25 Gbits/s. The block diagram of the macrocell used as a quad-channel transceiver is shown in Figure 1 and the single-channel macrocell design is shown in Figure 2. The input/output designations are given in Table 3.

Transmitter Section

The typical transmit and receive, high-speed I/O interfacing for single-channel applications is shown in Figures 8 and 9.

The transmitter brings in 8b/10b encoded bits in 10-bit parallel form for up to 1.25 Gbits/s transmission and converts the data to serial format. The serial nonreturn to zero (NRZ) bits are then shifted out of the device at a maximum rate of 1.25 Gbits/s. Internally, the device uses two parallel shift registers that operate at half rate (i.e., a maximum of 625 MHz) for reduced power consumption. The two shift registers drive the PECL output buffer in an interleaved manner to construct the 1.25 Gbit/s output data stream.

The transmit shift register and other circuits are driven with clocks generated from a 625 MHz internal clock. This internal clock is sourced from a voltage controlled oscillator (VCO) that is locked to the external reference of 100 MHz—125 MHz. The internal transmit phase-lock loop multiplies the frequency of the input reference clock by a factor of 5, and controls the transmit jitter bandwidth with appropriate design of the jitter transfer function. The transmit phase-lock loop generates multiple clock phases that are all used by each of the four receiver circuits. The clock phases are derived from the transmit VCO.

Receiver Section

The receiver circuit extracts clock from and retimes the serial input data. The data are input to the receiver on differential PECL buffers. External termination resistors are supplied by the user in accordance with *ANSI* standard, X3T11. The serial differential inputs, HDINP and HDINN, are ac-coupled to the device and internally biased to the PECL input common-mode range center.

The receiver data-retiming circuit uses a digital timing recovery loop that compares the phase of the input data to multiple phases of the on-device VCO in the transmit section. One of the phases is chosen to retime the receive data. A digital low-pass filter is used in the timing recovery loop to reject jitter from the data input. A novel phase interpolation circuit permits the retiming clock's phase to be stepped with fine resolution for precise alignment of the sampling clock within the data eye. Use of this digital data-locking scheme for each receiver advantageously avoids the use of multiple analog phase-lock loops on-device that can potentially injection lock to one another. Additionally, the digital data-locking loop maintains precise loop dynamics, hence the jitter transfer function is process and temperature independent.

Lock to Reference

The receive circuit has two modes of operation, lock to reference, and lock to data with retiming. When no data or invalid data is present on the HDINP and HDINN input nodes, the user can program the device to ignore the input data by setting LCKREFN equal to logic 0. In this mode, neither the PECL input buffer nor the RX parallel data bus toggles. In normal operations, LCKREFN is a logic 1 and the receiver attempts to lock to the incoming data. If the input data is invalid or outside the nominal \pm frequency range, the receive digital PLL will simply ramp the phase of the output clock until it locks to data.

Table 1. Receiver Circuit Operating Modes*

Mode	Lock to Reference	Lock to Receive Data
LCKREFN = 1 (normal operation)	Not applicable	Continually attempts to lock to data.
LCKREFN = 0	Lock to clock, output data does not toggle. Disable PECL input buffer.	Not applicable.

* REFCLK requirements are given in Table 4.

Functional Description (continued)

Byte Alignment

When ENCDDET = 1, the DNC5X3125 recognizes the comma character and aligns this 10-bit character to the word boundary, bits RX[0:9].

COMDET = 1 when the parallel output word contains a byte-aligned comma character. The COMDET flag will continue to pulse a logic 1 whenever a byte aligned comma character is at the parallel output port, independent of ENCDDET. When ENCDDET = 0, there are two possible scenarios depending upon when the comma character is received:

1. If byte-alignment had been previously achieved when ENCDDET had been a logic 1, the COMDET flag will continue to pulse a logic 1 whenever a byte-aligned comma character is at the parallel output port. If a comma character occurs that is not on the word boundary, no attempt will be made to align this comma character, and the COMDET flag will remain at a logic 0.
2. If byte-alignment had **not** been previously achieved when ENCDDET had been a logic 1, then the first (and only the first) comma character received will be aligned to the word boundary. COMDET will pulse when the comma character is aligned to the word boundary.

Parallel Output Port

Timing for the parallel output data and the 50 MHz to 62.5 MHz receive-byte clock is given in Table 14.

Two low data-rate, receive-byte clocks are available as outputs during use of the parallel output port in 10-bit mode. RXCLK1 is the receive-byte clock used by the protocol device to register bytes 0 and 2. RXCLK0 is the receive-byte clock used by the protocol device to register bytes 1 and 3, and it is 180 degrees out of phase with RXCLK1. Both RXCLK1 and RXCLK0 can be stretched during byte alignment but not truncated or slivered. The maximum allowable frequency of these two clocks under all circumstances, excluding start-up, will not exceed 80 MHz. The start-up time is specified as 1 ms.

Loopback Mode Operation

A control signal input, EWRAP, selects between two possible sets of inputs: normal data (HDINP, HDINN) or internal loopback data. When EWRAP = 1, the serial output ports, HDOUTP and HDOUTN, remain active. The serial transmit data prior to the PECL output driver is directed to the data recovery circuit, where the clock is recovered and data is resynchronized to the recovered clock. Retimed data and clock then go to the serial-to-parallel converter.

Table 2. Definition of Bit Transmission/Reception Order

Serial Transmit/Receive Rate	TX[9:0]	RX[9:0]
1.0 Gbits/s to 1.25 Gbits/s	TX[0] bit serially transmitted first at HDOUTP, HDOUTN	RX[0] bit received first at serial inputs, HDINP, HDINN

Functional Description (continued)

Powerup Sequence

An appropriate powerup reset (PUR) standard cell must be placed in the ASIC to hold the transceiver in reset until full power is supplied to the macrocell. REFCLK must be active at the time the PUR output goes low and must stay active while powered up, unless in Reset.

When PUR and signals RESET, BYPPLL, and LPWR are all low, the following start-up sequence occurs:

1. 0 μ s—32 μ s, the analog PLL is held at minimum frequency to allow dc bias to settle.
2. 32 μ s—262 μ s, the analog PLL has locked in and receiver analog circuits start to lock in.
3. 262 μ s—326 μ s, the receiver analog circuits are locked; receiver starts to lock onto incoming data.
4. After 358 μ s, receiver is locked onto incoming data and can be viewed at the parallel output ports. The comma detect circuit is enabled at this point allowing byte alignment if ENCDDET = 1.

If LCKREFN goes low after the 358 μ s, the receiver will sit idle. When LCKREFN goes high, the receiver will be locked onto data after 2 μ s.

Macrocell Reset

The RESET input to the macrocell is an active-high. When activated with a pulse duration of 1 μ s, the RESET signal globally resets the macrocell and the following is performed:

1. The single analog PLL is forced to operate at the minimum frequency possible for its VCO. The PLL will not be locked in this condition.
2. The high-speed serial output HDOUTP is forced to a PECL logic 0, HDOUTN to logic 1.
3. The deserializer clocks are reset, input data at HDINP, HDINN is ignored and the RX[9:0] signals remain in their previous state.
4. The phase interpolation/selection circuits are deactivated and the selected phase is reset.
5. The receiver digital low-pass filter in the DPLL is reset. Normally, a reset is not necessary for correct operation, although a reset can aid rapid lock-in of the internal PLL circuitry.

Sleep Mode

The DNC5X3125 has a sleep mode that is activated by enabling LPWR. In this mode, a divided-down version of the REFCLK is used to refresh the dynamic circuits within the transceiver. The PLL is powered down in this mode also. LCKREFN can also be activated to reduce the power even further. Note that complete power down for IDDQ testing is not supported due to the dynamic logic used in the high-speed sections of the transceiver. The lock-in sequence timing is needed when coming out of sleep mode.

Functional Description (continued)

Block Diagrams

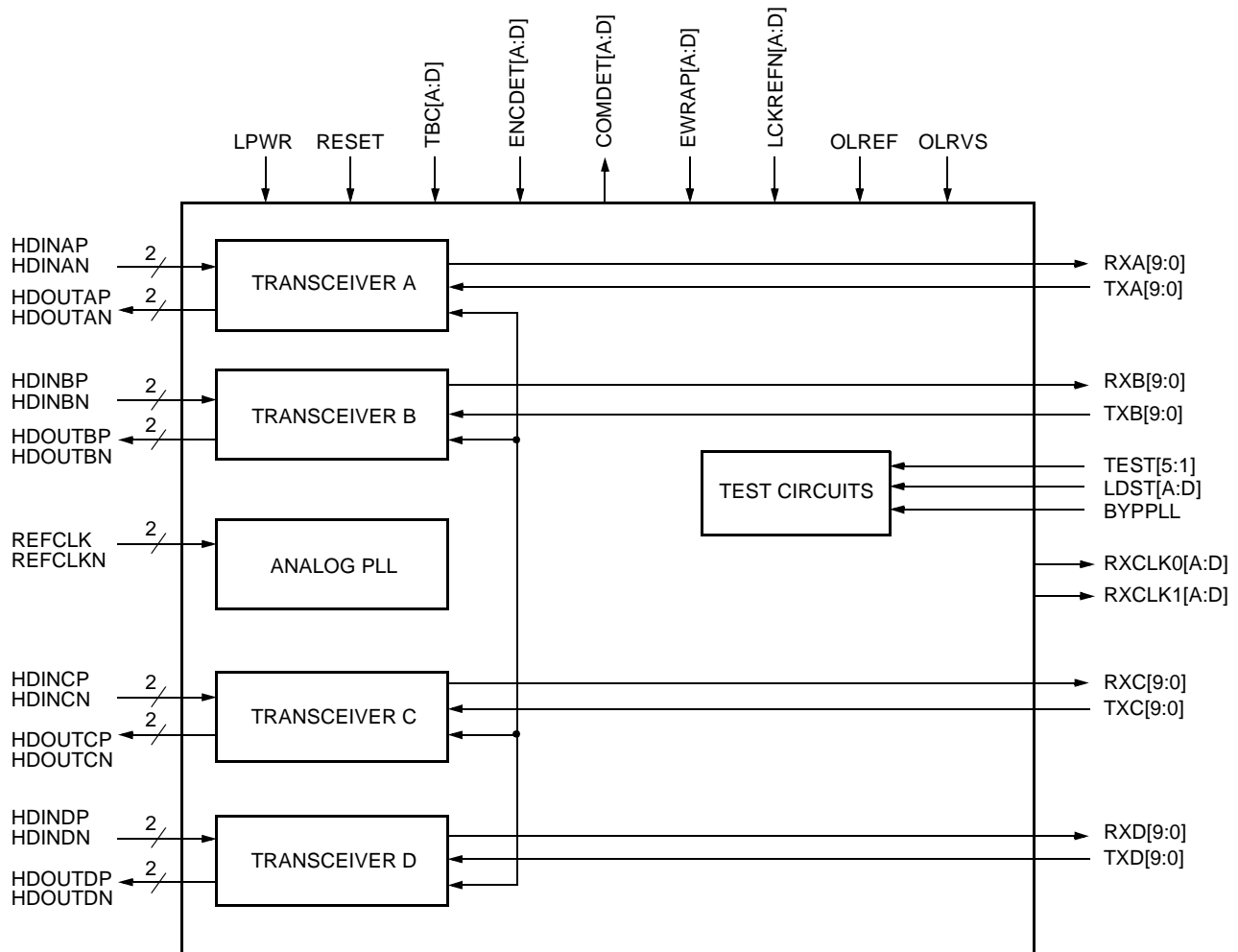
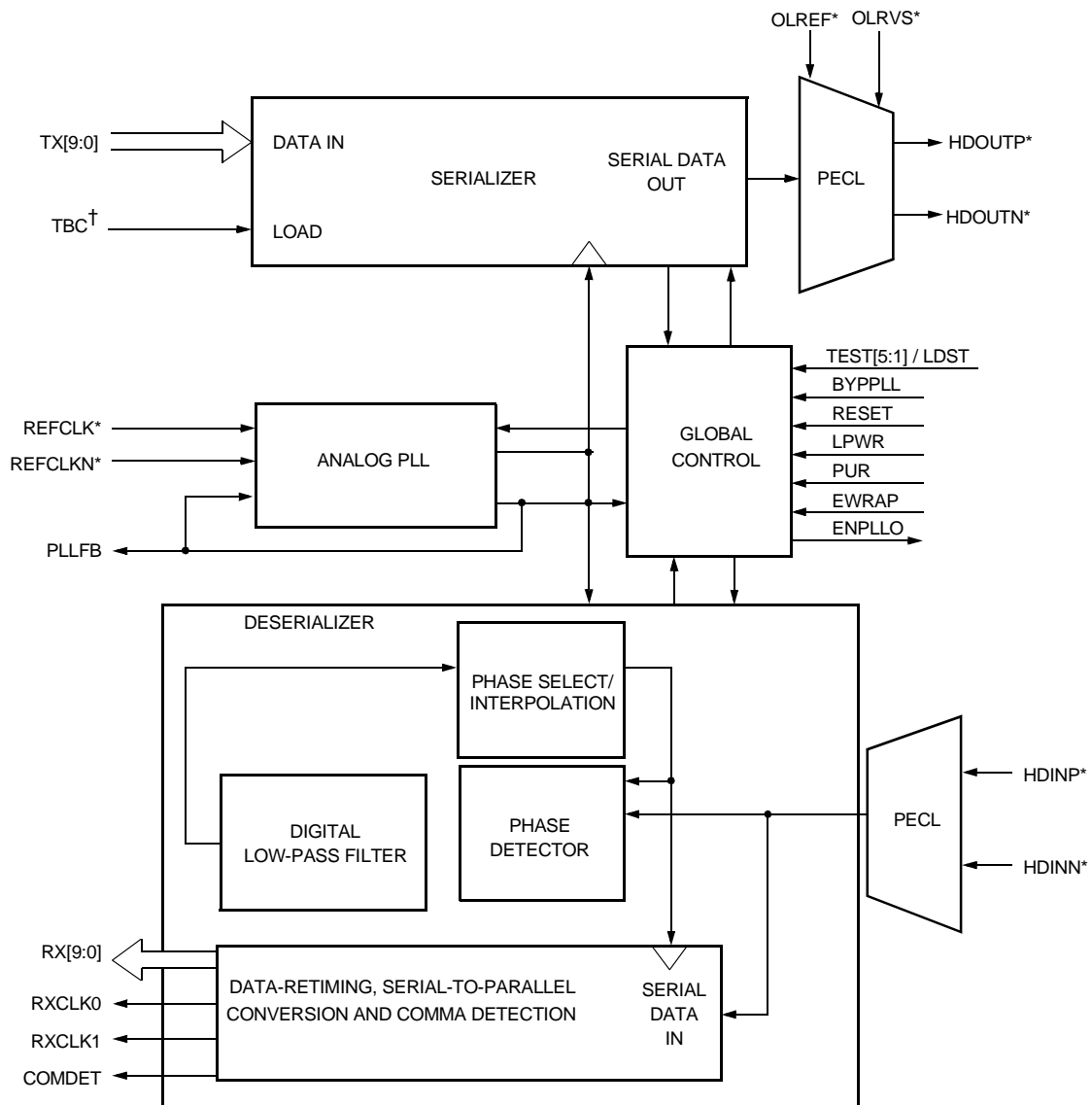


Figure 1. Quad Gigabit Ethernet Transceiver Block Diagram

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Functional Description (continued)

Block Diagrams (continued)



5-8809(F)

* These signals brought to I/O pads for SERDES integration.

† Synchronous with REFCLKN.

Figure 2. DNC5X3125 Single-Channel Transceiver Functional Block Diagram

Input/Output Information

Table 3a. I/O Channel Interface

Name	I/O	Level	Description
TX[9:0]	Input	CMOS	Transmit Data [9:0]. Parallel input bits [9:0], one 10-bit, 8b/10b encoded data byte, clocked-in on the rising edge of TBC. TX0 is the least significant bit.
RX[9:0]	Output	CMOS	Receive Data [9:0]. Parallel output bits [9:0], one 10-bit data type, clocked-out on the alternate rising edges of RXCLK0, RXCLK1. RX0 is the least significant bit.
TBC	Input	TTL/CMOS	Transmit Byte Clock (100 MHz—125 MHz). Synchronous with REFCLKN.
RXCLK0	Output	CMOS	Receive Byte Clock 0.
RXCLK1	Output	CMOS	Receive Byte Clock 1.
ENCDET	Input	CMOS	Enable Comma Detection.
COMDET	Output	CMOS	Byte-Aligned Comma Detect.
EWRAP	Input	CMOS	Loopback at Serial I/O.
LCKREFN	Input	CMOS	Lock Receiver to Clock.
HDINP, HDINN	Input	PECL	Differential Serial Inputs.
HDOUTP, HDOUTN	Output	PECL	Differential Serial Outputs.
LDST	Input	CMOS	Load TEST[5:1] Inputs.

Table 3b. I/O Control/PLL Interface Connections

Name	I/O	Level	Description
OLREF	Input/Output	Analog	PECL Level Set Resistor Terminal 1.
OLRVS	Input/Output	Analog	PECL Level Set Resistor Terminal 2.
LPWR	Input	CMOS	Macrocell Low-Power Mode.
RESET	Input	CMOS	Macrocell Reset (Active-High).
TEST5	Input	CMOS	Global Test Control Input.
TEST4	Input	CMOS	Local Test Control Input.
TEST3	Input	CMOS	Local Test Control Input.
TEST2	Input	CMOS	Local Test Control Input.
TEST1	Input	CMOS	Local Test Control Input.
BYPPLL	Input	CMOS	Test Control—PLL Bypass Mode.
REFCLK, REFCLKN	Input	PECL or TTL/CMOS	Reference Clock Input (100 MHz—125 MHz).
PUR	Input	CMOS	Powerup Reset.
PLLFB	Output	CMOS	PLL Feedback Clock.
ENPLLO	Output	CMOS	Enable PLL Feedback.

Input/Output Information (continued)**Table 3c. Power Connections**

Name	Description
VDDG	Global Digital Power.
VDDR	High-Speed Receive Power.
VDDT	High-Speed Transmit Power.
VDDP	PLL Power.
VDD	Power.
VSSG	Global Digital Ground.
VSSR	High-Speed Receive Ground.
V SST	High-Speed Transmit Ground
VSSP	PLL Ground.
VSS	Ground.

Electrical Specifications**Transmitter****Table 4. Reference Clock Specifications (REFCLK and REFCLKN)**

Parameter	Minimum	Maximum	Unit
Frequency Range	100	125	MHz
Frequency Tolerance	−100	100	ppm
Duty Cycle*	40	60	%
Rise Time (PECL)	—	0.8	ns
Fall Time (PECL)	—	0.8	ns
Rise Time (TTL/CMOS)	—	1.5	ns
Fall Time (TTL/CMOS)	—	1.5	ns
In-band Jitter 1 Gbits/s—1.25 Gbits/s	—	30	ps p-p
Out-of-Band Jitter	—	50	ps p-p

* Measured at 50% amplitude point.

Table 5. PLL Specifications

Parameter	Minimum	Typical	Maximum	Unit
Bandwidth	—	1.5	—	MHz
Jitter Peaking	—	0.5	—	dB
Lock Time	—	—	230	μs

Table 6. Output Jitter at 1.0 Gbits/s—1.25 Gbits/s

Parameter	Minimum	Maximum	Unit
Deterministic	—	0.08	UI p-p
Random	—	0.12	UI p-p
Total	—	0.2	UI p-p

Electrical Specifications (continued)

Receiver

Table 7. Receiver Input Data Rate

Parameter	Minimum	Maximum	Unit
Data Rate	1.0	1.25	Gbits/s
Frequency Tolerance with REFCLK	−100	100	ppm

Table 8. Data Lock Characteristics

Parameter	Minimum	Typical	Maximum	Unit
Bandwidth	0.3 *	—	1†	MHz
Jitter Peaking†	—	0.5	—	dB
Lock time*	—	—	2	μs

* Data pattern: 111110000 . . .

† Data pattern: 101010 . . .

Table 9. Power Dissipation*

Parameter	Minimum	Maximum	Unit
Power	—	750	mW
Sleep Mode	—	TBD	mW

* Depending on application (PCB layout, etc.)

Table 10. dc Electrical Specifications

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Supply Voltage	V _{DD} , V _{DDA}	—	3.135	3.3	3.465	V
Diff. PECL Output	—	Load, as in Figure 8	800	—	—	mV
Diff. PECL Input	—	Source configuration, as in Figure 8	400	—	1600	mV

Table 11. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage	3.135	3.465	V
TTL High Input Voltage	3.0	3.6	V
PECL Output Current	—	16	mA
Junction Operating Temperature	0	125	°C
Storage Temperature	−65	150	°C

Timing Characteristics

Serial Timing

Table 12. Serial Output Timing Levels

Description	Minimum	Typical	Maximum	Unit
Rise Time 20%—80%	0.17	0.2	0.22	ns
Fall Time 80%—20%	0.17	0.2	0.22	ns
Common Mode	$V_{DD}/2 - 0.1$	$V_{DD}/2$	$V_{DD}/2 + 0.1$	V
Differential Swing	0.8	—	1.6	V p-p
Load (See Table 16.)	50	—	75	Ω

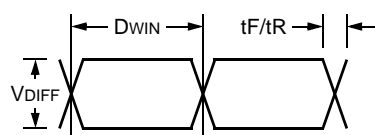


Figure 3. Serial Interface Timing

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Table 13. Serial Input Interface Timing

Description	Minimum	Maximum	Unit
Rise Time (t_R)	150	225	ps
Fall Time (t_F)	150	225	ps
Differential Swing (V_{DIFF})	0.4	1.6	V p-p
Source Impedance	50	75	Ω
Data Eye Opening (D_{WIN})	320	—	ps

Timing Characteristics (continued)

Receiver Section Timing

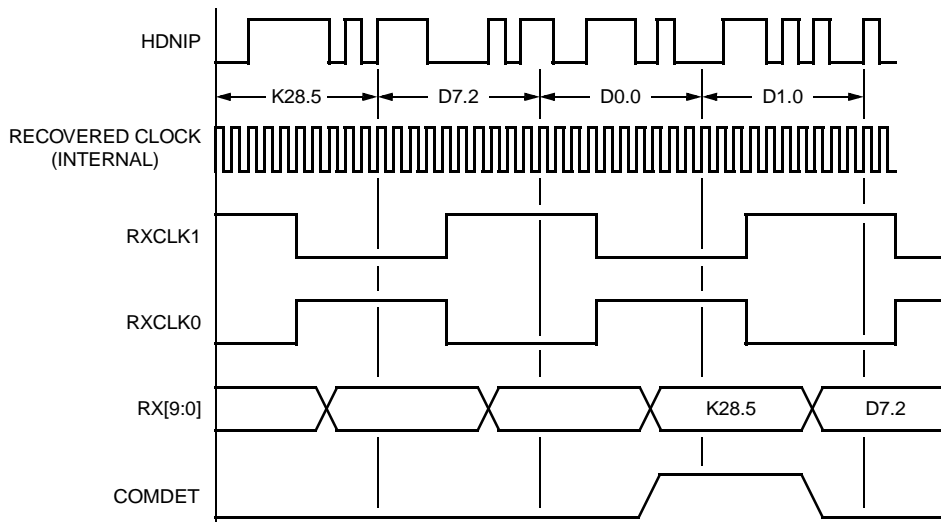


Figure 4. Receiver Section Timing

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Receiver Port Timing

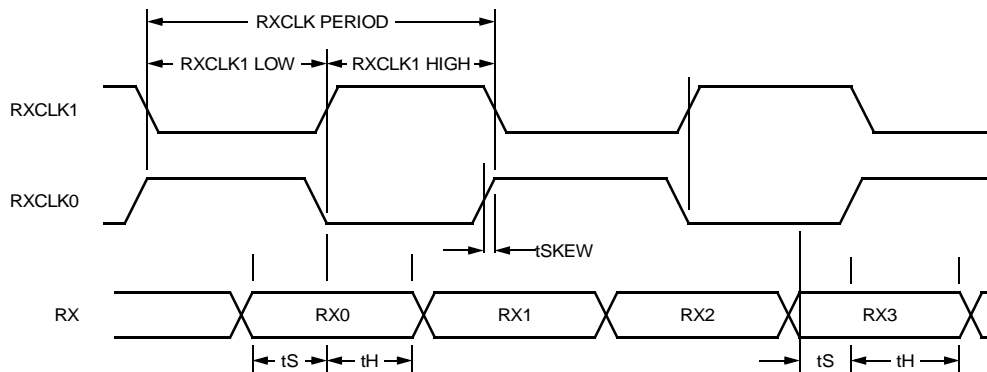


Figure 5. Receiver Port Timing

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Table 14. Receiver Parallel Port Timing

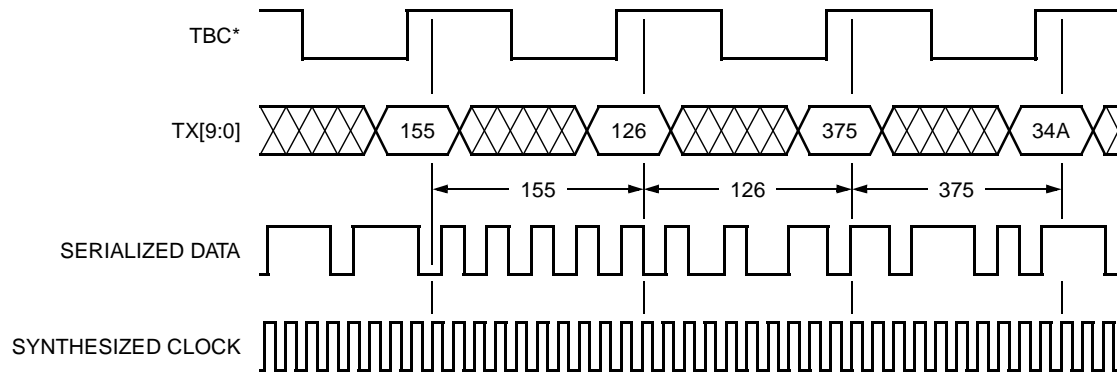
Symbol	Parameter	Min	Max	Unit
—	RXCLK[1:0] Frequency*	—	62.5	MHz
—	RXCLK[1:0] Low	7.0	9.0	ns
—	RXCLK[1:0] High	7.0	9.0	ns
t _{R/F}	RXCLK[1:0] (0.4 V to 2.6 V) [†]	0.2	0.5	ns
t _{R/F}	Data Output (0.4 V to 2.6 V) [†]	0.2	0.5	ns
t _S	Setup Time	3.0	—	ns
t _H	Hold Time	2.0	—	ns
t _{SKEW}	Skew	—	1.0	ns

* 1.25 Gbits/s.

[†] 0.5 pF load.

Timing Characteristics (continued)

Transmitter Section Timing



* Synchronous with REFCLKN.

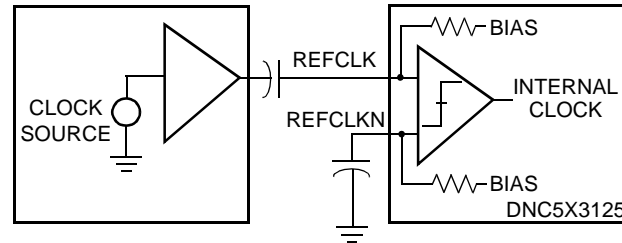
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Figure 6. Parallel Interface Transmit Timing

Table 15. Transmitter Timing at Parallel Interface

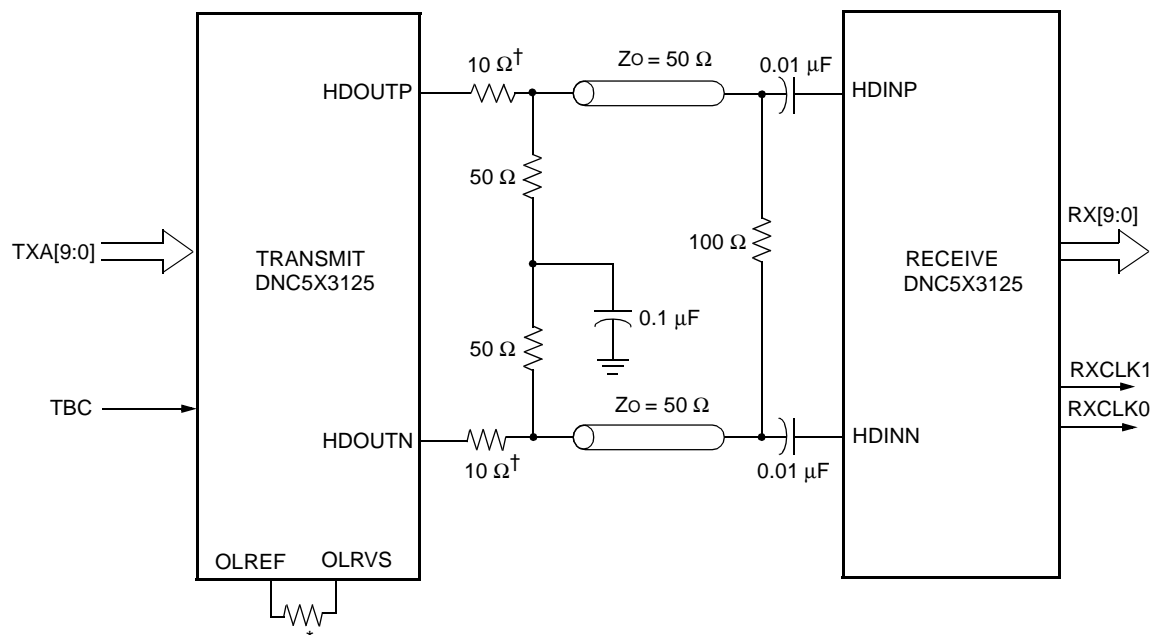
Description	Minimum	Maximum	Unit	Conditions
Data Setup	2	—	ns	With Positive Edge TBC
Data Hold	2	—	ns	With Positive Edge TBC
Rise Time	—	1	ns	—
Fall Time	—	1	ns	—

Application Information



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Figure 7. Reference Clock Connections with Single-Ended Source



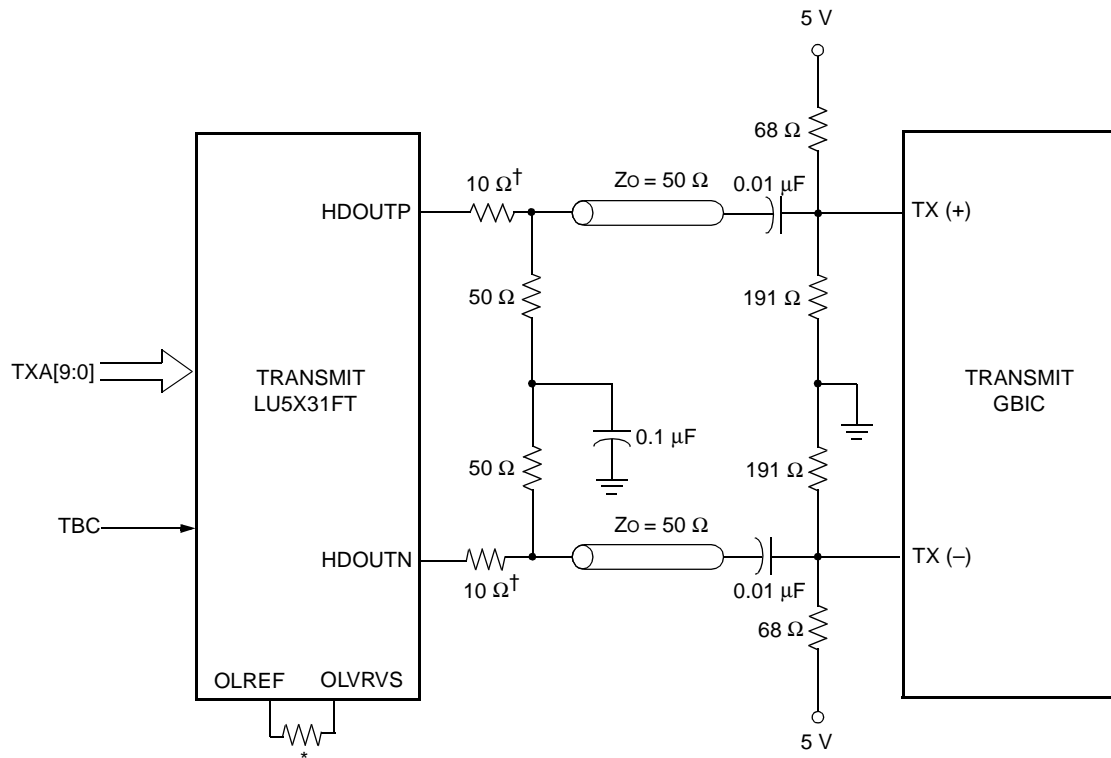
* External resistor connected between OLREF and OLRVS. See Table 16 for external resistor value required for differential output swing.

† Damping resistor, maximum = 10 Ω.

Figure 8. Typical Termination for a Single-Channel, High-Speed Serial Transmit-and-Receive Port in a 50 Ω Backplane Application

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Application Information (continued)



5-8811(F)b

* External resistor connected between OLREF and OLVRVS. See Table 16 for resistor value vs. termination impedance and output swing.
† Damping resistor, maximum = 10 Ω

Figure 9. Typical Termination for a Single-Channel, High-Speed Serial Transmit Port Interfacing a 5 V GBIC Transceiver

Table 16. External Resistor Value vs. Differential Output Level Viewing

Resistor Value (Ω)	Termination Impedance (Ω)	Differential Output Voltage (V)
7.5 K/11.25 K	50/75	0.8
5 K/7.5 K		1.2
4 K/6 K		1.6

Test Modes

Note: Test modes are intended for manufacture test only and are not guaranteed to be operational. They may be modified or eliminated without prior notice.

The device has per-channel test modes as well as global test modes. The bypass PLL, BYPPLL, is a global test input because it modifies the operation of the analog PLL. Test bits TEST[4:1] generally operate in the localized mode. The LDST[A:D] inputs are enable signals that permit the TEST[4:1] signals to be injected into a particular channel.

For example, if LDST = 1, the TEST[4:1] signals directly control the test modes in the A channel. Once LDST = 0, the previous values of TEST[4:1] are held for the A channel. The TEST[4:1] signals control the four channels (A, B, C, D) via level sense latches that are gated with the LDST[A:D] inputs. TEST[5] is a global test node used for both injection of signals as well as for monitoring points within the device.

Table 17. Test Modes

Global	Local Test Configuration				Global	Operation
BYPPLL	Test1	Test2	Test3	Test4	Test5	
0	1	1	1	1	X	Normal operation.
0	1	1	1	0	Output	Analog PLL feedback signal viewed at TEST5.
0	1	1	0	1	X	Transceiver operates normally except RX[9:0] output is from digital filter, not the serial data.
0	1	1	0	0	Output	Transceiver operates normally except RX[9:0] output is from digital filter and the analog PLL feedback signal is viewed at TEST5.
0	1	0	1	P	P	Digital filter forced to count. Pulses applied at TEST4 increments accumulator, pulses at TEST5 decrements accumulator.
0	1	0	0	P	P	RX[9:0] output is from digital filter, not the serial data. Digital filter forced to count. Pulses applied at TEST4 increments accumulator, pulses at TEST5 decrements accumulator.
0	0	1	1	1	X	Parallel loopback. TX[9:0] = RX[9:0]. RX[9:0] remains active.
0	0	1	1	0	Output	Parallel loopback. TX[9:0] = RX[9:0] and analog PLL feedback signal viewed at TEST5. RX[9:0] remains active.
0	0	1	0	1	X	RX[9:0] output is from digital filter, not the serial data. Receive channel is held in reset. BYPPLL overrides this reset.
0	0	1	0	0	Output	RX[9:0] output is from digital filter, not the serial data. Receive channel is held in reset. BYPPLL overrides this reset. Analog PLL feedback signal viewed at TEST5.
0	0	0	1	1	X	Transmitter is held in reset. BYPPLL overrides this reset.

Test Modes (continued)

Table 17. Test Modes (continued)

Global	Local Test Configuration				Global	Operation
BYPPLL	Test1	Test2	Test3	Test4	Test5	
0	0	0	1	0	Output	Transmitter is held in reset. BYPPLL overrides this reset. Analog PLL feedback signal viewed at TEST5.
0	0	0	0	1	X	Transmitter and receiver are held in reset. RX[9:0] output is from digital filter, not the serial data.
0	0	0	0	0	Output	Transmitter and receiver are held in reset. RX[9:0] output is from digital filter, not the serial data. Analog PLL feedback signal viewed at TEST5.
1	X	X	1	C-0	C-90	Analog PLL is bypassed for low speed functional test. A low speed clock is input to TEST4, and a quadrature clock is applied to TEST5. Frequency of clocks is 5 x REFCLK, but here REFCLK is lowered to about 1 MHz.
1	X	X	0	C-0	C-90	Analog PLL is bypassed for low speed functional test. A low speed clock is input to TEST4, and a quadrature clock is applied to TEST5. Frequency of clocks is 5 x REFCLK, but here REFCLK is lowered to about 1 MHz. RX[9:0] output is from digital filter, not the serial data.

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