

## L8567 SLIC for People's Republic of China Applications

---

### Features

- Low active power (typical 149 mW during on-hook transmission)
- Sleep state for low idle power (47 mW typical)
- Quiet tip/ring polarity reversal
- Distortion-free on-hook transmission
- -35 V to -65 V battery operation
- Convenient operating states:
  - Forward active
  - Polarity reversal active
  - Sleep
  - Forward disconnect
- Supervision functions:
  - Fixed threshold off-hook detector with longitudinal rejection and hysteresis
  - Ring trip detector
  - Thermal shutdown indication
- Adjustable loop current limit
- Three driver outputs for relay driver
- LED driver output to indicate off-hook
- Latched parallel data interface
- Battery and +5 V required:
  - Optional auxiliary lower voltage battery to reduce short loop power
- -40 °C to +85 °C operational temperature range
- User-selectable power management techniques
- Thermal protection
- 32-pin PLCC or 44-pin PLCC packaging

### Description

#### General

This electronic subscriber loop interface circuit (SLIC) is optimized for low cost and low power consumption while providing a full-feature set.

Included in the feature set is quiet reverse battery. Quiet polarity reversal is possible because the ac path is uninterrupted during transmission. The dc loop current limit is user-adjustable via a single external resistor. The maximum battery voltage is specified as -65 V for long loop applications. The L8567 supports on-hook transmission.

The total short loop off-hook power may be reduced by use of a lower-voltage auxiliary battery supply. If, when using the 32-pin PLCC, the user does not wish to supply an auxiliary battery, the component of the total short loop off-hook power that is dissipated on the L8567 SLIC is controlled by use of an external power resistor. With the 44-pin PLCC, a power resistor is not necessary.

Included are both the loop closure and ring trip supervision functions. The loop closure threshold is fixed internally, which eliminates the need for an external precision resistor to set the threshold. To minimize noise at the supervision output, hysteresis is included on the loop closure function. The loop closure and ring trip outputs are multiplexed into a single NSTAT output. Also included is a thermal shutdown mechanism. If device temperature exceeds 165 °C, as may be the case under an extended power cross fault, the SLIC will shut down (i.e., enter a high-impedance state) to provide protection against the fault. A logic output will indicate the SLIC is in thermal shutdown.

## Table of Contents

<b>Contents</b>	<b>Page</b>		
Features .....	1	Outline Diagrams .....	39
Description.....	1	32-Pin PLCC .....	39
General.....	1	44-Pin PLCC .....	40
Application for People's Republic of China .....	4	Ordering Information.....	41
Pin Information .....	6		
Coding Information .....	9	<b>Figures</b>	<b>Page</b>
Absolute Maximum Ratings.....	11	Figure 1. Functional Diagram .....	5
Recommended Operating Conditions .....	11	Figure 2. 32-Pin Diagram (PLCC Chip) .....	6
Electrical Characteristics .....	12	Figure 3. 44-Pin Diagram (PLCC Chip) .....	6
Logic Interface .....	14	Figure 4. Ring Trip Circuits .....	16
Ring Trip Requirements .....	16	Figure 5. Timing Requirements .....	16
Test Configurations .....	17	Figure 6. Basic Test Circuit .....	17
RFI Rejection.....	19	Figure 7. Metallic PSRR .....	18
Functional Description.....	21	Figure 8. Longitudinal PSRR .....	18
General.....	21	Figure 9. Longitudinal Balance .....	18
Use with T7507 Codec for Use in People's Republic of China .....	21	Figure 10. Longitudinal Impedance .....	18
Chip Set Performance Specifications .....	22	Figure 11. ac Gains .....	18
Gain.....	22	Figure 12. RFI Rejection Test Circuit .....	19
Gain Flatness—In Band .....	22	Figure 13. RFI Testing, Forward Battery, 600 $\Omega$ Loop, No Capacitor, 1 Vrms .....	20
Gain Flatness—Out of Band—High Frequencies .....	22	Figure 14. RFI Testing, Forward Battery, 600 $\Omega$ Loop, No Capacitor, 2 Vrms .....	20
Gain Flatness—Out of Band—Low Frequencies .....	22	Figure 15. Termination Impedance .....	22
Loss vs. Level Relative to Loss at -10 dBm Input at 1020 Hz .....	23	Figure 16. Transmit and Receive Direction Frequency-Dependent Loss Relative to Gain at 3400 Hz .....	22
Return Loss .....	23	Figure 17. Loss vs. Level .....	23
Hybrid Balance .....	23	Figure 18. Return Loss .....	23
Applications .....	24	Figure 19. Hybrid Balance .....	23
Design Considerations .....	26	Figure 20. Basic Loop Start Application Using T7507 Codec and L7583 Switch for 200 $\Omega$ + (680 $\Omega$    100 nF) Complex Termination and Hybrid Balance .....	24
Characteristic Curves .....	27	Figure 21. L8567 Typical V <sub>CC</sub> Power Supply Rejection .....	27
Power Control.....	28	Figure 22. L8567 Typical V <sub>BAT</sub> Power Supply Rejection .....	27
Power Control—Auxiliary Battery .....	29	Figure 23. L8567 Loop Current vs. Loop Voltage .....	27
Power Control—32-Pin PLCC with Power Control Resistor .....	29	Figure 24. L8567 Loop/Battery Current (with Battery Switch) vs. Loop Resistance .....	27
Power Considerations .....	30	Figure 25. Power Derating .....	28
Power Control—44-Pin PLCC Package .....	32	Figure 26. Tip/Ring Voltage Decrease .....	33
dc Characteristics .....	33	Figure 27. SLIC 2-Wire Output Stage .....	34
Loop Range.....	34	Figure 28. Ring Trip Equivalent Circuit and Equivalent Application .....	36
dc Applications .....	34	Figure 29. Simplified Control Scheme .....	37
On-Hook Transmission.....	34	Figure 30. Logic Output Latches .....	38
Supervision.....	35		
Loop Closure .....	35		
Ring Trip Detection.....	36		
Other Supervision Functions .....	36		
Latched Parallel Data Interface .....	37		
ac Design .....	38		
First-Generation Codecs .....	38		
Second-Generation Codecs .....	38		
Third-Generation Codecs .....	38		
T7507 Codec.....	38		

## Table of Contents (continued)

Tables	Page
Table 1. Pin Descriptions .....	7
Table 2. Input State Coding .....	9
Table 3. Supervision Coding .....	10
Table 4. Power Supply .....	12
Table 5. 2-Wire Port .....	13
Table 6. Analog Pin Characteristics .....	13
Table 7. ac Feed Characteristics .....	14
Table 8. Logic Inputs (B0, B1, EN, RD1I, RD2I, and RD3I) and Outputs (NSTAT and NTSD) .....	14
Table 9. Drivers (RD1O, RD2O, and RD3O) .....	15
Table 10. LED Driver (NLED) .....	15
Table 11. Timing Requirements (DI, EN, DO, and RD), CCLK = 2.048 MHz .....	16
Table 12. Gain .....	22
Table 13. Gain Flatness—In Band .....	22
Table 14. Gain Flatness—Out of Band—Low Frequencies .....	22
Table 15. Parts List for Loop Start Application .....	25
Table 16. $200\ \Omega + 680\ \Omega \parallel 0.1\ \mu\text{F}$ Design Parameters .....	26
Table 17. Power Connections .....	28
Table 18. $R_{PWR} = 2600\ \Omega$ .....	31
Table 19. $R_{PWR} = 2200\ \Omega$ .....	31
Table 20. $R_{PWR} = 1800\ \Omega$ .....	31
Table 21. $R_{PWR} = 4400\ \Omega$ .....	32
Table 22. $R_{PWR} = 2310\ \Omega$ ( $R_{PWR} = 2200\ \Omega + 5\%$ ).....	32
Table 23. $R_{PWR} = 2090\ \Omega$ ( $R_{PWR} = 2200\ \Omega - 5\%$ ).....	32
Table 24. Valid Data at NSTAT and NTSD .....	38

## **Description** (continued)

### **General** (continued)

This device uses a latched parallel data input interface and a gated parallel output data interface. Level-sensitive data latches are used for state control inputs, and level-sensitive control gates are used for supervision outputs. Latch and gate control are through an ENABLE pin. When the ENABLE pin is high, input data is latched and the SLIC will not respond to changes at its logic input. When ENABLE is low, input control data will flow through the latch. Valid supervision data will appear at the NSTAT and NTSD outputs only when ENABLE is low. In this manner, the data input and data output of multiple SLICs can be serviced by a single control input or output. The L8567 is designed to be controlled/supervised using control/supervision outputs and inputs from the T7507 codec.

Three relay drivers are also included. These drivers are meant to drive electromechanical relays (EMRs). State control of the relay drivers is via latched parallel data inputs. Like the B0/B1 and supervision data, control leads from the T7507 codec drive these inputs. The T7507 relay driver control outputs are meant to control the associated control input on all four of the L8567 SLICs associated with the T7507 codec.

If an L7583 solid-state switch is used (instead of EMRs), the data control outputs from the T7507 codec will drive the latched state control inputs of the L7583 directly. Again, one data control output from the T7507 will drive the corresponding data input on four channels of the L7583. In the case of using the L7583, tie RD1I, RD2I, and RD3I relay driver control inputs of the L8567 to ground.

Included are two supervision outputs. Both supervision outputs are the wire-OR of the loop closure and ring trip detectors. One (NSTAT) is used as a data control

output and is gated via the EN input. The other (NLED) can be used to drive an LED to indicate loop states. The NLED driver is an open collector output, so multiple outputs may be used to drive a single LED. NLED is not gated, so valid supervision data appears at NLED regardless of the state of EN. NLED can be used as an alternative, nongated, data control output.

The L8567 is available in a 32-pin PLCC or 44-pin PLCC package.

## **Application for People's Republic of China**

This SLIC may be used with any commercially available codec; however, when used with the Agere Systems Inc. T7507, the two devices form a complete line circuit optimized for requirements in the People's Republic of China. The ac interface between the two components is extremely simple, requiring only a single capacitor in the transmit direction and a short-circuit connection, using no external components, in the receive direction.

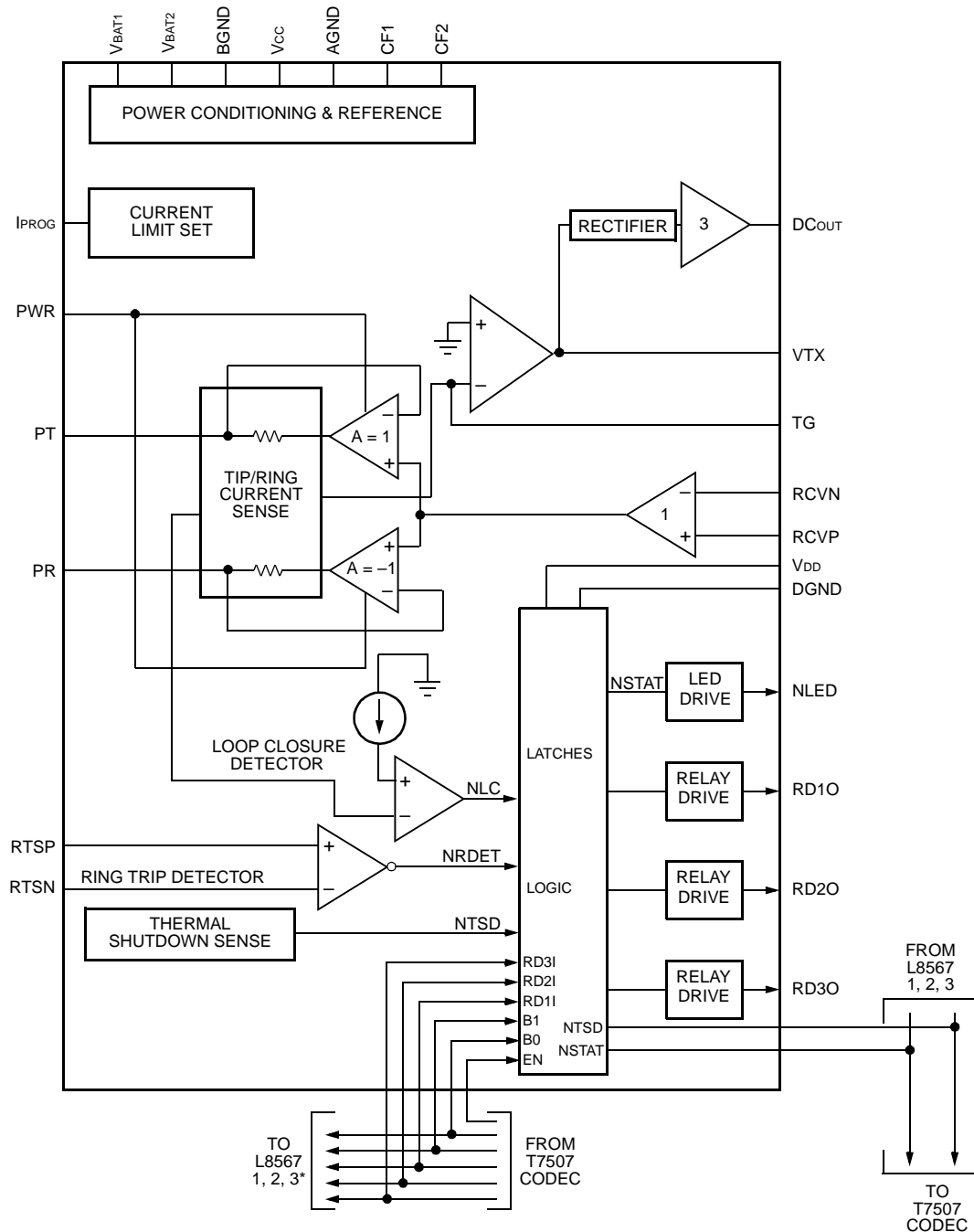
The complex  $200\ \Omega + 680\ \Omega \parallel 100\ \text{nF}$  termination and hybrid balance is digitally synthesized by the T7507 codec. Additionally, the tip/ring to PCM (transmit) gain is fixed and set digitally by the T7507 codec at 0 dB. The PCM to tip/ring (receive) gain is also digitally set by the T7507 codec and is programmable via a bit in the codec serial data control stream to either  $-3.5\ \text{dB}$  or  $-7.0\ \text{dB}$ .

The control interfaces of the L8567 and T7507 are designed for compatibility with each other.

Both the T7507 codec and L8567 SLIC require only battery and +5 V to operate. When both devices are used, no  $-5\ \text{V}$  supply is required.

## Description (continued)

## Application for People's Republic of China (continued)



12-2551.f (F)

\* Relay driver controls routed to L8567 RD1I, RD2I, and RD3I pins when using EMR. If L7583 solid-state switch is used, driver control buses are routed directly to L7583 control inputs, and SLIC pins RD1I, RD2I, and RD3I are grounded.

**Figure 1. Functional Diagram**



## Pin Information (continued)

Table 1. Pin Descriptions

44-Pin	32-Pin	Symbol	Type	Description
2	1	RD3I	I	<b>Relay Driver 3 Input.</b> This latched logic input sets the state of the relay driver number 3. When using EMRs, the relay driver is controlled by this input via a data bus or independent data line. When using an L758X solid-state switch, the solid-state switch is controlled directly via the data bus or independent data line and the relay driver is unused; in this case, tie this logic input to ground.
3	2	RD2I	I	<b>Relay Driver 2 Input.</b> This latched logic input sets the state of the relay driver number 2. When using EMRs, the relay driver is controlled by this input via a data bus or independent data line. When using an L758X solid-state switch, the solid-state switch is controlled directly via the data bus or independent data line and the relay driver is unused; in this case, tie this logic input to ground.
4	3	RD1I	I	<b>Relay Driver 1 Input.</b> This latched logic input sets the state of the relay driver number 1. When using EMRs, the relay driver is controlled by this input via a data bus or independent data line. When using an L758X solid-state switch, the solid-state switch is controlled directly via the data bus or independent data line and the relay driver is unused; in this case, tie this logic input to ground.
6	4	RD3O	O	<b>Relay Driver 3 Output.</b> Output to drive an EMR, controlled by RD3I.
5, 12, 14, 15, 20, 26, 28, 32, 35, 39, 42, 43	—	NC	—	<b>No Connect.</b>
7	5	RD2O	O	<b>Relay Driver 2 Output.</b> Output to drive an EMR, controlled by RD2I.
8	6	RD1O	O	<b>Relay Driver 1 Output.</b> Output to drive an EMR, controlled by RD1I.
9	7	NLED	O	<b>NSTAT LED Driver.</b> This output is equivalent to NSTAT, except this output has sufficient drive capability to drive an LED. This LED driver output is an open-collector output, so multiple outputs may be used to drive a single LED. This output may be used as an alternative logic output to the latched NSTAT output to indicate ring trip or loop supervision status. This output is valid regardless of the state of EN.
10	8	DGND	PWR	<b>Digital Ground.</b>
11	9	VDD	PWR	<b>+5 V Digital Power Supply.</b>
13	10	VCC	PWR	<b>+5 V Analog Power Supply.</b>
16	11	I <sub>PROG</sub>	I	<b>Current-Limit Program Resistor.</b> A resistor to DC <sub>OUT</sub> sets the dc current limit.
17	12	DC <sub>OUT</sub>	O	<b>dc Output Voltage.</b> This output is a voltage that is directly proportional to the absolute value of the differential tip/ring current.
18	13	RTSP	I	<b>Ring Trip Sense Positive.</b> Connect this pin to the ring relay and to the ringer series through a high-value resistor.
19	14	RTSN	I	<b>Ring Trip Sense Negative.</b> Connect this pin to the ringing generator through a high-value resistor.

## Pin Information (continued)

Table 1. Pin Descriptions (continued)

44-Pin	32-Pin	Symbol	Type	Description
21	15	PR	I/O	<b>Protected Ring.</b> The output of the ring driver amplifier and input to loop sensing circuitry. Connect to loop through overcurrent series resistance.
22	16	PT	I/O	<b>Protected Tip.</b> The output of the tip driver amplifier and input to loop sensing circuitry. Connect to loop through overcurrent series resistance.
23	17	VBAT1	PWR	<b>Battery Supply.</b> Most negative primary high-voltage power supply.
24	18	BGND	PWR	<b>Battery Ground.</b> Ground return for battery supply.
25	19	VBAT2	PWR	<b>Auxiliary Battery Supply.</b> Connect to the lower-voltage (magnitude) auxiliary battery supply. If a lower-voltage auxiliary battery is not used, connect directly to the primary high-voltage battery side.
27	20	PWR	PWR	<b>Power Control.</b> With a 32-pin PLCC, connect a lower-voltage auxiliary battery supply directly to PWR or connect a resistor from this node to high-voltage battery to control short-loop power dissipation. With a 44-pin PLCC, connect the higher-voltage battery directly to PWR. Please see the Power Control section of this data sheet for more information.
29	21	CF1	—	<b>Filter Capacitor 1.</b> Connect a 0.47 $\mu$ F capacitor from this pin to CF2.
30	22	CF2	—	<b>Filter Capacitor 2.</b> Connect a 0.1 $\mu$ F capacitor from this pin to AGND.
31	23	TG	I	<b>Transmit Gain.</b> Noninverting input to internal AX transmit amplifier. Connect a 7.87 k $\Omega$ resistor from this node to VTX to set internal SLIC transconductance to 39.75 V/A. Transconductance of 39.75 V/A is assumed for use with T7507 codec.
33	24	VTX	O	<b>Transmit ac Output Voltage.</b> Output of SLIC transmit amplifier. This output is a voltage that is directly proportional to the differential tip/ring current. Connect a 7.87 k $\Omega$ resistor from this node to TG to set internal SLIC transconductance to 39.75 $\Omega$ .
34	25	AGND	PWR	<b>Analog Signal Ground.</b>
36	26	RCVN	I	<b>Receive ac Signal (Inverting).</b> This high-impedance input controls the ac differential voltage on tip and ring.
37	27	RCVP	I	<b>Receive ac Signal (Noninverting).</b> This high-impedance input controls the ac differential voltage on tip and ring.
38	28	EN	I	<b>Data Enable.</b> Level-sensitive data latch control; when high, data at the B0, B1, and relay driver control inputs is latched. When low, the data latch is transparent and control signals will flow through the data latch to the SLIC control logic. NSTAT and NTSD supervision outputs are valid only when EN is low.
40	29	NTSD	O	<b>Not Thermal Shutdown.</b> This gated logic output indicates if the L8567 die temperature has exceeded the thermal shutdown temperature and the device has entered the thermal shutdown mode. Input EN needs to be low for valid data to appear at NTSD. The actual thermal shutdown is not affected by EN.
41	30	NSTAT	O	<b>Loop Detector Output/Ring Trip Output.</b> This gated logic output is a wired-OR of the Not Loop Closure/Not Ring Trip detect outputs. When low, this logic output indicates that an off-hook condition exists or that ringing has been tripped. Input EN needs to be low for valid data to appear at NSTAT.
44	31	B1	I	<b>State Control Input.</b> This latched logic input, with B0, controls the state of the SLIC.
1	32	B0	I	<b>State Control Input.</b> This latched logic input, with B1, controls the state of the SLIC.



## Coding Information

Table 2 shows the input state coding.

**Table 2. Input State Coding**

B0*	B1*	RD3I*	RD2I*	RD1I*	State/Definition
1	1	X	X	X	<b>Powerup, Forward Battery.</b> Normal talk and battery feed state. Pin PT is positive with respect to PR. On-hook transmission is enabled. The ring trip and loop closure detectors are active.
1	0	X	X	X	<b>Powerup, Reverse Battery.</b> Normal talk and battery feed state. Pin PR is positive with respect to PT. On-hook transmission is enabled. The ring trip and loop closure detectors are active.
0	1	X	X	X	<b>Low-Power Scan.</b> Except for off-hook supervision, all circuits are shut down to conserve power. Pin PT is positive with respect to PR. Thermal shutdown is active. Note that the ring trip detector is not active during the low-power scan. To ensure that the ring trip detector is active during ringing, the L8567 SLIC must be put into the forward or reverse powerup state before applying power ringing to the loop.
0	0	X	X	X	<b>Disconnect.</b> The tip and ring amplifiers are turned off and the SLIC goes into a high-impedance (>100 kΩ) state. The L8567 will reset into this state on powerup.
X	X	1	X	X	<b>Driver RD1 Output Is Active.</b> Input pin RD1I is high. This will activate or place the RD1 driver output into the on state. In the on state, the driver will supply up to 40 mA of current (at 0.6 V) to the coil of an EMR, thus activating the EMR.
X	X	0	X	X	<b>Driver RD1 Output Is Not Active<sup>†</sup>.</b> Input pin RD1I is low. This will place the RD1 driver output into the off state. In the off state, the driver will not supply current to the coil of an EMR, thus deactivating the EMR.
X	X	X	1	X	<b>Driver RD2 Output Is Active.</b> Input pin RD2I is high. This will activate or place the RD2 driver output into the on state. In the on state, the driver will supply up to 40 mA of current (at 0.6 V) to the coil of an EMR, thus activating the EMR.
X	X	X	0	X	<b>Driver RD2 Output Is Not Active<sup>†</sup>.</b> Input pin RD2I is low. This will place the RD2 driver output into the off state. In the off state, the driver will not supply current to the coil of an EMR, thus deactivating the EMR.
X	X	X	X	1	<b>Driver RD3 Output Is Active.</b> Input pin RD3I is high. This will activate or place the RD3 driver output into the on state. In the on state, the driver will supply up to 40 mA of current (at 0.6 V) to the coil of an EMR, thus activating the EMR.
X	X	X	X	0	<b>Driver RD3 Output Is Not Active<sup>†</sup>.</b> Input pin RD3I is low. This will place the RD3 driver output into the off state. In the off state, the driver will not supply current to the coil of an EMR, thus deactivating the EMR.

\* All logic inputs are latched. The data latch is controlled by pin EN. The EN latch control is level sensitive.

When EN is high, the input data latches are active; that is, data at the B0, B1, RD1I, RD2I, and RD3I inputs are latched. The latched data will control the state of the SLIC and drivers so that the SLIC and drivers will not respond to changes at the logic inputs while the level at EN is high. When EN is low, the input latch is not active; therefore, data at the logic inputs will flow through the latch and immediately determine the state of the SLIC and drivers.

† If using an L758X solid-state switch, the switch is controlled directly from the T7507 codec; thus the relay drivers in the L8567 SLIC cannot be used. If the relay drivers are not used, force them into the lowest power (not active) state by connecting RD1I, RD2I, and RD3I to ground.

## Coding Information (continued)

Table 3 gives the output coding.

**Table 3. Supervision Coding**

Output	State
<b>NSTAT*</b>	
0	<b>Off-Hook or Ring Trip.</b> dc current greater than the typical 11 mA loop current threshold is flowing in the subscriber loop, or the ring trip comparator has detected a dc voltage greater than the ring trip threshold. This indicates that dc current is flowing in the loop with the ring relay set in the power ring state. The presence of dc current in the power ring state implies that the handset is off-hook, or that a ring trip condition exists. This is a latched output. EN must be low for data on this output to be valid.
1	<b>On-Hook or Not Ring Trip.</b> dc current less than the difference of the off-hook current threshold and loop current hysteresis is flowing, or the loop is in the power ringing state and the handset is on-hook—no dc current has been detected. This is a latched output. EN must be low for data on this output to be valid.
<b>NTSD*</b>	
0	The SLIC die temperature has exceeded the thermal shutdown temperature threshold, and the SLIC is forced into the equivalent of the disconnect state, regardless of the state of the B0 and B1 logic inputs. There is a hysteresis in the shutdown circuit, and the device will remain in thermal shutdown until the die temperature drops below the hysteresis threshold. This is a latched output. EN must be low for data on this output to be valid.
1	The SLIC die temperature has not exceeded the thermal shutdown temperature threshold, and the SLIC state is set per B0 and B1 logic. This is a latched output. EN must be low for data on this output to be valid.
<b>NLED†</b>	
0	Identical to the off-hook or ring trip state of output NSTAT. In this state, NLED can supply 10 mA at 1.0 V, which is sufficient to drive an LED. This output is an open collector output, so multiple NLED outputs from different devices can be used to drive a common LED. This output is not latched, so it has valid data regardless of the state of EN. NLED can be used as an alternative to the latched NSTAT output.
1	Identical to the on-hook or not ring trip state of the pin NSTAT.

\* Data outputs NSTAT and NTSD are gated. In order to drive the NSTAT or NTSD outputs low, both the internal detector (i.e., an off-hook or thermal shutdown condition, respectively, exists) and pin EN must be low.

† This output is not latched; data is valid regardless of the state of EN. It can be used to drive an LED or as an alternative unlatched ring trip/off-hook detector.

## Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
+5 V Power Supply	$V_{CC}$	—	—	7.0	V
+5 V Digital Supply	$V_{DD}$	—	—	7.0	V
Battery (talking) Supplies*	$V_{BAT1}, V_{BAT2}$	—	—	-70	V
Logic Input Voltage	—	-0.5	—	7.0	V
Analog Input Voltage	—	-7.0	—	7.0	V
Maximum Junction Temperature	$T_J$	—	—	165	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-40	—	125	$^\circ\text{C}$
Relative Humidity Range	$R_H$	5	—	95	%
Ground Potential Difference (BGND to AGND)	—	—	—	$\pm 3$	V

\* Use of an auxiliary battery,  $V_{BAT2}$ , whose magnitude is equal to the primary battery  $V_{BAT1}$  but does not exceed the absolute maximum rating, will not damage the chip. However, in a 32-pin PLCC, it will drive the L8567 into thermal shutdown under short-loop conditions. Use a power resistor to node PWR.

Note: The IC can be damaged unless all ground connections are applied before, and removed after, all other connections. Furthermore, when powering the device, the user must guarantee that no external potential creates a voltage on any pin of the device that exceeds the device ratings. Some of the known examples of conditions that cause such potentials during powerup are 1) an inductor connected to tip and ring can force an overvoltage on  $V_{BAT}$  through the protection devices if the  $V_{BAT}$  connection chatters, and 2) inductance in the  $V_{BAT}$  lead could resonate with the  $V_{BAT}$  filter capacitor to cause a destructive overvoltage.

## Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Ambient Temperature	-40	—	85	$^\circ\text{C}$
$V_{CC}$ Supply Voltage	4.75	5.0	5.25	V
$V_{DD}$ Supply Voltage	4.75	5.0	5.25	V
$V_{BAT1}$ Supply Voltage	-65	-48	-35	V
$V_{BAT2}$ Auxiliary Battery Supply Voltage	-35	-24	-15	V
dc Loop Current-limit Programming Range	15	40	45	mA
On- and Off-hook 2-wire Signal Level	—	3.17	—	dBm

## Electrical Characteristics

Minimum and maximum values are testing requirements in the temperature range of 25 °C to 85 °C and battery range of –35 V to –65 V. These minimum and maximum values are guaranteed to –40 °C based on component simulations and design verification of samples, but devices are not tested to –40 °C in production. The test circuit shown in Figure 6 is used unless otherwise noted. Positive currents flow into the device.

Typical values are characteristics of the device design at 25 °C based on engineering evaluations and are not part of the test requirements. Supply values used for typical characterization are  $V_{CC} = V_{DD} = 5.0$  V,  $V_{BAT1} = -48$  V,  $V_{BAT2} = -25.5$  V.

**Table 4. Power Supply**

Parameter	Min	Typ	Max	Unit
Power Supply Rejection 500 Hz to 3 kHz (See Figures 6 and 7.) <sup>1</sup> :				
$V_{CC}$ (1 kHz)	35	—	—	dB
$V_{BAT}$ (500 Hz—3 kHz)	45	—	—	dB
Thermal Protection Shutdown ( $T_{TSD}$ ) <sup>1</sup>	—	165	—	°C
Thermal Resistance, Junction to Ambient ( $\theta_{JA}$ ) (still air) <sup>1</sup> :				
32-pin PLCC	—	60	—	°C/W
44-pin PLCC	—	47	—	°C/W
Power Supply—Powerup, No Loop Current with On-hook Transmission, Relay Drivers Off, dc Supplies at Typical Values, Use $V_{BAT1}$ and $V_{BAT2}$ :				
$I_{CC} + I_{DD}$	—	6.0	6.6	mA
$I_{BAT1}$ ( $V_{BAT1} = -48$ V)	—	2.25	2.7	mA
$I_{BAT2}$ ( $V_{BAT2} = -24$ V)	—	0.45	0.54	mA
Quiescent Active Power Dissipation	—	149	180	mW
Power Supply—Low-power Scan, Forward Battery, No Loop Current, Relay Drivers Off, Use $V_{BAT1}$ and $V_{BAT2}$ :				
$I_{CC} + I_{DD}$	—	4.0	4.5	mA
$I_{BAT1}$ ( $V_{BAT1} = -48$ V)	—	0.61	0.78	mA
$I_{BAT2}$ ( $V_{BAT2} = -24$ V)	—	0.0	0.0	mA
Quiescent Active Power Dissipation	—	47	60	mW
Power Supply—Powerup, No Loop Current with On-hook Transmission, Relay Drivers Off, dc Supplies at Typical Values, Use $V_{BAT1}$ Only:				
$I_{CC} + I_{DD}$	—	6.0	6.6	mA
$I_{BAT}$ ( $V_{BAT1} = -48$ V)	—	2.7	3.46	mA
Quiescent Active Power Dissipation <sup>2</sup>	—	160	199	mW
Power Supply—Low-power Scan, Forward Battery, No Loop Current, Relay Drivers Off:				
$I_{CC} + I_{DD}$	—	4.0	4.5	mA
$I_{BAT}$ ( $V_{BAT1} = -48$ V)	—	0.61	0.78	mA
Power Dissipation <sup>2</sup>	—	47	60	mW

1. This parameter is not tested in production. It is guaranteed by design and device characterization.

2. This is the total power drawn from the power supplies. If a power resistor is not used, the total power is dissipated by the SLIC through the package. If a power resistor is used, the power is shared by the resistor and the SLIC.

## Electrical Characteristics (continued)

Table 5. 2-Wire Port

Parameter	Min	Typ	Max	Unit
Tip or Ring Drive Current = dc + Longitudinal + Signal Currents	65	—	—	mA
Signal Current <sup>1</sup>	10	—	—	mArms
Longitudinal Current Capability per Wire <sup>1, 2</sup>	8.5	15	—	mArms
dc Loop Current Limit <sup>3</sup> : R <sub>LOOP</sub> = 100 Ω Programmability Range Accuracy (18 mA < I <sub>LIM</sub> < 45 mA)	— 15 —	I <sub>LIM</sub> — —	— 45 ±15	mA mA %
Powerup Open-loop Voltage Levels: Common-mode Voltage Differential Voltage	—  V <sub>BAT</sub> + 7.8	V <sub>BAT</sub> /2  V <sub>BAT</sub> + 7.1	—  V <sub>BAT</sub> + 6.4	V V
Disconnect State: PT Resistance (V <sub>BAT</sub> < V <sub>PT</sub> < 0 V) PR Resistance (V <sub>BAT</sub> < V <sub>PR</sub> < 0 V)	— —	1 1	— —	MΩ MΩ
dc Feed Resistance (for I <sub>LOOP</sub> below current limit)	—	110	—	Ω
Loop Resistance Range (3.17 dBm overload into 200 + 680    0.1 μF): I <sub>LOOP</sub> = 18 mA at V <sub>BAT</sub> = -48 V	1800	—	—	Ω
Longitudinal to Metallic Balance— <i>IEEE</i> <sup>4</sup> Std. 455 (See Figure 9.) <sup>5</sup> : 50 Hz to 300 Hz 300 Hz to 600 Hz 600 Hz to 3400 Hz	38 48 52	— — —	— — —	dB dB dB
Metallic to Longitudinal Balance: 1 kHz to 3 kHz	38	—	—	dB

1. This parameter is not tested in production. It is guaranteed by design and device characterization.
2. The longitudinal current is independent of dc loop current.
3. Current-limit I<sub>LIM</sub> is programmed by a resistor, R<sub>PROG</sub>, from pin I<sub>PROG</sub> to AGND. R<sub>PROG</sub> (kΩ) = 1.59 I<sub>LIM</sub> (mA).
4. *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.
5. Longitudinal balance of circuit card will depend on loop series resistance matching.

Table 6. Analog Pin Characteristics

Parameter	Min	Typ	Max	Unit
Differential PT/PR Current Sense (DC <sub>OUT</sub> ) Gain (PT/PR to DC <sub>OUT</sub> ): Forward Battery Reverse Battery	— —	-119 119	— —	V/A V/A
Loop Closure Detector Threshold (on-hook to off-hook at V <sub>BAT1</sub> = -48 V)	9	11	13	mA
Loop Closure Detector Hysteresis: Variation	— —	2 ±0.5	— —	mA mA
Ring Trip Comparator: Input Offset Voltage	—	±10	—	mV
RCVN, RCPV: Input Impedance Gain RCPV to PT/PR Gain RCVN to PT/PR	— — —	100 2 -2	— — —	kΩ — —

## Electrical Characteristics (continued)

Transmit direction is tip/ring to 4-wire. Receive direction is 4-wire to tip/ring.

**Table 7. ac Feed Characteristics**

Parameter	Min	Typ	Max	Unit
Total Harmonic Distortion—200 Hz to 4 kHz <sup>1</sup> :				
Off-hook	—	—	0.3	%
On-hook	—	—	1.0	%
Transmit Gain, f = 1020 Hz (See Figure 11.); PT/PR to VTX Transmit Gain	38.56	39.75	40.94	V/A
Receive Gain, f = 1020 Hz (See Figure 11.); RCVP/RCVN to PT/PR Receive Gain	1.94	2	2.06	—
2-wire Idle-channel Noise (200 $\Omega$ + 680 $\Omega$    0.1 $\mu$ F termination):				
Psophometric <sup>1</sup>	—	—	–77	dBmp
C-message	—	—	12	dBrnC
3 kHz Flat <sup>1</sup>	—	—	20	dBrn
Transmit Idle-channel Noise:				
Psophometric <sup>1</sup>	—	—	–77	dBmp
C-message	—	—	12	dBrnC
3 kHz Flat <sup>1</sup>	—	—	20	dBrn

1. This parameter is not tested in production. It is guaranteed by design and device characterization.

## Logic Interface

**Table 8. Logic Inputs (B0, B1, EN, RD1I, RD2I, and RD3I) and Outputs (NSTAT and NTSD)**

Parameter <sup>1</sup>	Symbol	Min	Max	Unit
High-level Input Voltage	V <sub>IH</sub>	2.4	V <sub>DDD</sub>	V
Low-level Input Voltage	V <sub>IL</sub>	0	0.8	V
Input Bias Current (high and low)	I <sub>IN</sub>	—	±50	$\mu$ A
High-level Output Voltage (I <sub>OUT</sub> = –100 $\mu$ A)	V <sub>OH</sub>	V <sub>DD</sub> – 1.5	V <sub>DD</sub>	V
Low-level Output Voltage (I <sub>OUT</sub> = 180 $\mu$ A)	V <sub>OL</sub>	0	0.4	V
Output Short-circuit Current (V <sub>OUT</sub> = V <sub>DD</sub> )	I <sub>OSS</sub>	1	35	mA
Output Load Capacitance <sup>2</sup>	C <sub>OL</sub>	0	50	pF

1. Unless otherwise specified, all logic voltages are referenced to DGND.

2. This parameter is not tested in production. It is guaranteed by design and device characterization.

## Electrical Characteristics (continued)

### Logic Interface (continued)

**Table 9. Drivers (RD1O, RD2O, and RD3O)<sup>1</sup>**

Parameter <sup>2</sup>	Symbol	Min	Max	Unit
Off-state Output Current ( $V_{OUT} = V_{DD}$ )	$I_{OFF}$	—	$\pm 200$	$\mu A$
On-state Output Voltage ( $I_{OUT} = 40\text{ mA}$ )	$V_{ON}$	0	0.60	V
On-state Output Voltage ( $I_{OUT} = 20\text{ mA}$ )	$V_{ON}$	0	0.40	V
Clamp Diode Reverse Current ( $V_{OUT} = 0$ )	$I_R$	—	$\pm 10$	$\mu A$
Clamp Diode On Voltage ( $I_{OUT} = 80\text{ mA}$ )	$V_{OC}$	$V_{CC} + 0.5$	$V_{CC} + 3.0$	V
Turn-on Time <sup>3</sup>	$t_{ON}$	—	10	$\mu s$
Turn-off Time <sup>3</sup>	$t_{OFF}$	—	10	$\mu s$

1. The relay drivers operate using the  $V_{DD}$  supply. When  $V_{DD}$  is first applied to the device, the relay drivers will power up and remain in the off state until the SLIC is configured via the data interface.

2. Unless otherwise specified, all logic voltages are referenced to DGND.

3. This parameter is not tested in production. It is guaranteed by design and device characterization.

**Table 10. LED Driver (NLED)<sup>1</sup>**

Parameter <sup>2</sup>	Symbol	Min	Max	Unit
Off-state Output Current ( $V_{OUT} = V_{DD}$ )	$I_{OFF}$	—	$\pm 10$	$\mu A$
On-state Output Voltage ( $I_{OUT} = 10\text{ mA}$ )	$V_{ON}$	0	1.0	V
Turn-on Time <sup>3</sup>	$t_{ON}$	—	10	$\mu s$
Turn-off Time <sup>3</sup>	$t_{OFF}$	—	10	$\mu s$

1. NLED is an open collector output, so multiple NLED outputs may be used to drive a common LED.

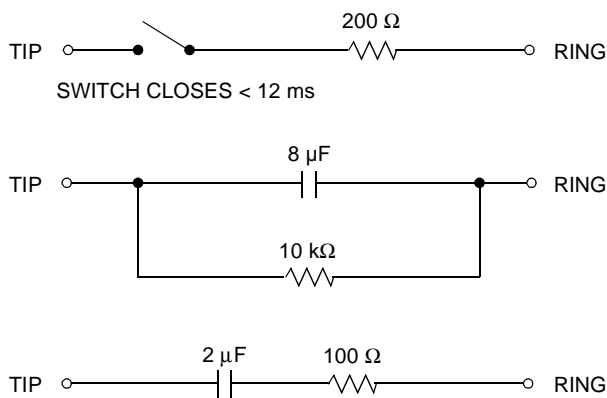
2. Unless otherwise specified, all logic voltages are referenced to DGND.

3. This parameter is not tested in production. It is guaranteed by design and device characterization.

## Electrical Characteristics (continued)

### Ring Trip Requirements

- Ringing signal:
  - Voltage, minimum 35 Vrms, maximum 100 Vrms.
  - Frequency, 17 Hz to 28 Hz.
  - Crest factor, 1.4 to 2.
- Ringing trip:
  - $\leq 100$  ms (typical),  $\leq 250$  ms ( $V_{BAT} = -33$  V, loop length = 530  $\Omega$ ).
- Pretrip:
  - The circuits in Figure 4 will not cause ringing trip.



5-5841 (F)

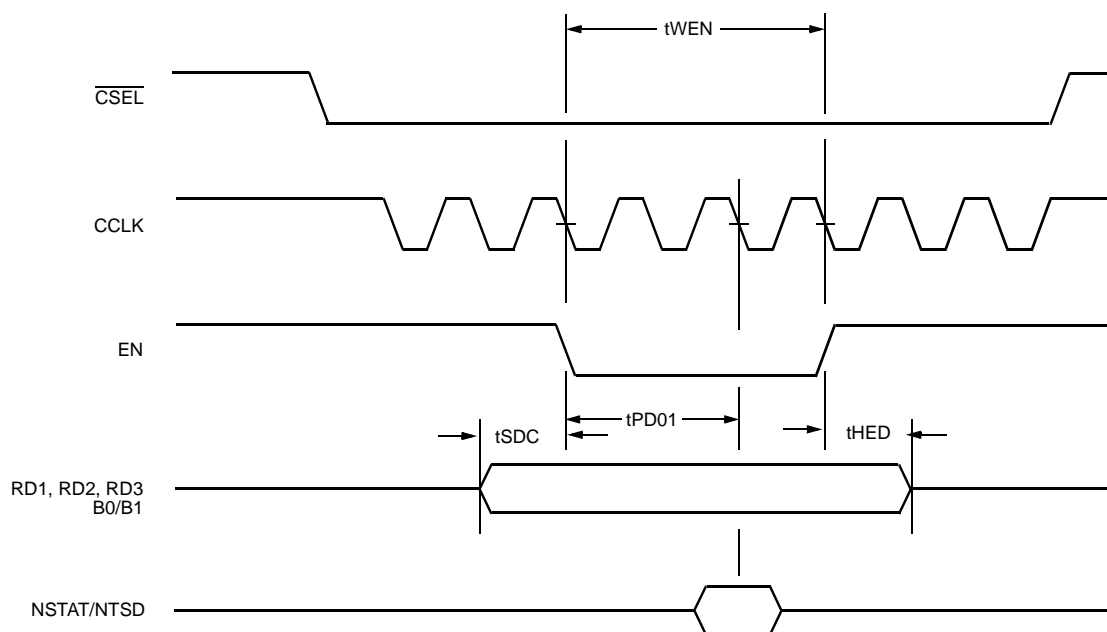
Figure 4. Ring Trip Circuits

Table 11. Timing Requirements (DI, EN, DO, and RD), CCLK = 2.048 MHz

Symbol	Parameter <sup>1</sup>	Min	Max	Unit
$t_R, t_F$	Input Rise and Fall Time EN (10% to 90%) <sup>2</sup>	0	75	ns
$C_{IN}$	Maximum Input Capacitance <sup>2</sup>	—	5	pF
$t_{PD01}$	Propagation Delay EN to DO <sup>2</sup>	0	977	ns
$t_{PDR}$	Propagation Delay EN to RD Outputs <sup>2</sup>	0	10	$\mu$ s
$t_{SDC}$	Minimum Setup Time from DI to EN <sup>2</sup>	488	—	ns
$t_{HED}$	Minimum Hold Time from EN to DI <sup>2</sup>	488	—	ns
$t_{WEN}$	Minimum Pulse Width of EN <sup>2</sup>	1465	—	$\mu$ s

1. Unless otherwise specified, all times are measured from the 50% point of logic transitions.

2. This parameter is not tested in production. It is guaranteed by design and device characterization.

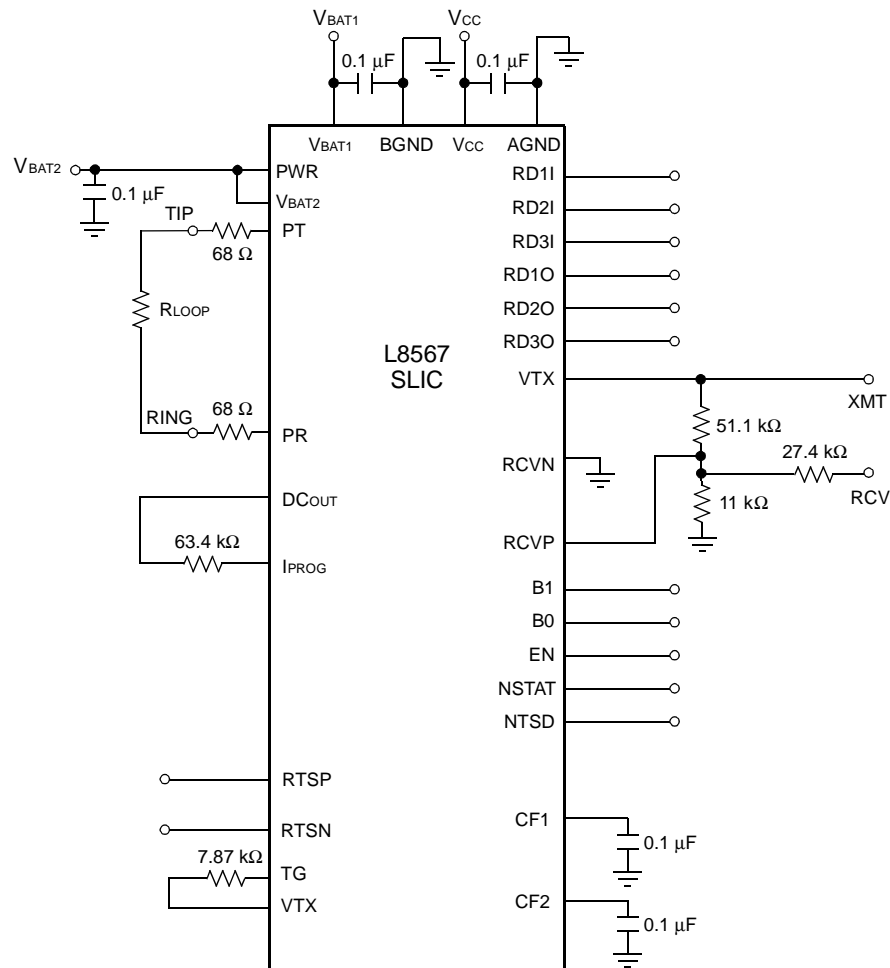


5-5808a

Figure 5. Timing Requirements



## Test Configurations



12-2578.e (F)

Figure 6. Basic Test Circuit

## Test Configurations (continued)

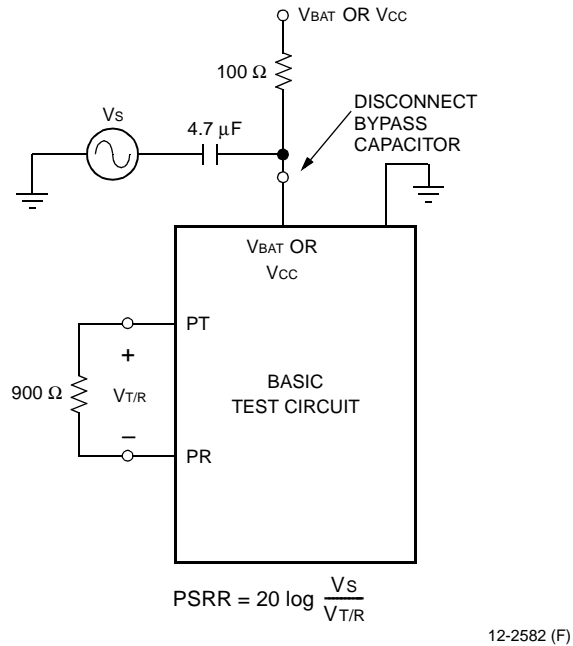


Figure 7. Metallic PSRR

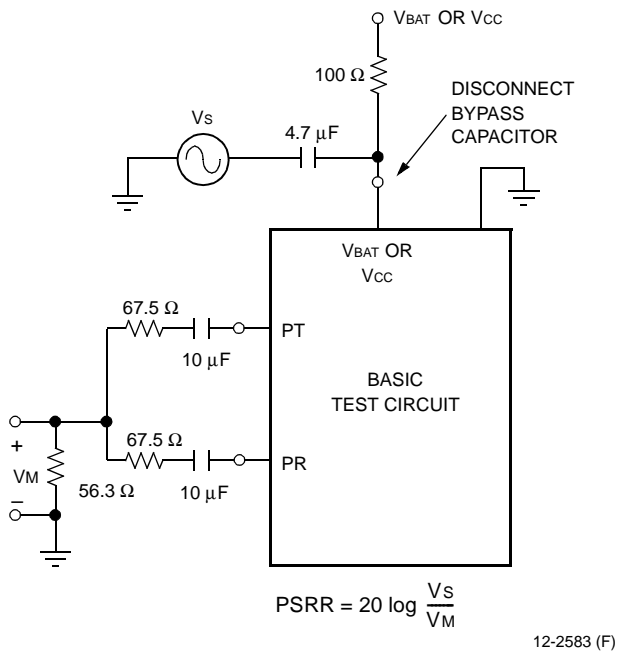


Figure 8. Longitudinal PSRR

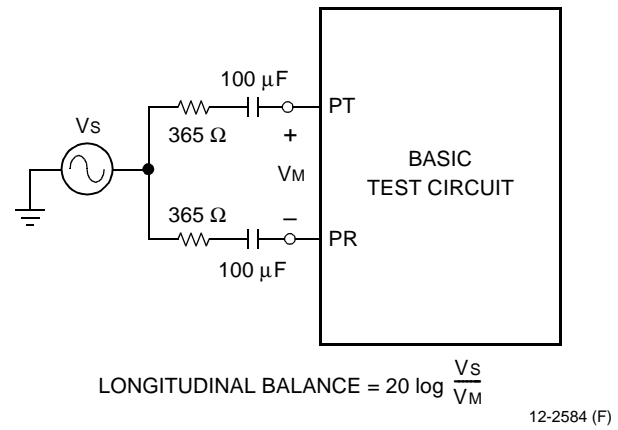


Figure 9. Longitudinal Balance

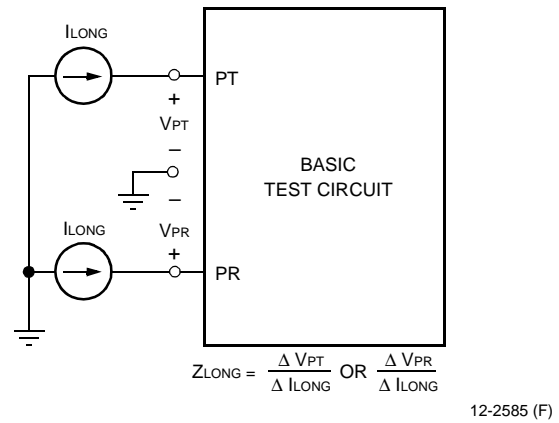


Figure 10. Longitudinal Impedance

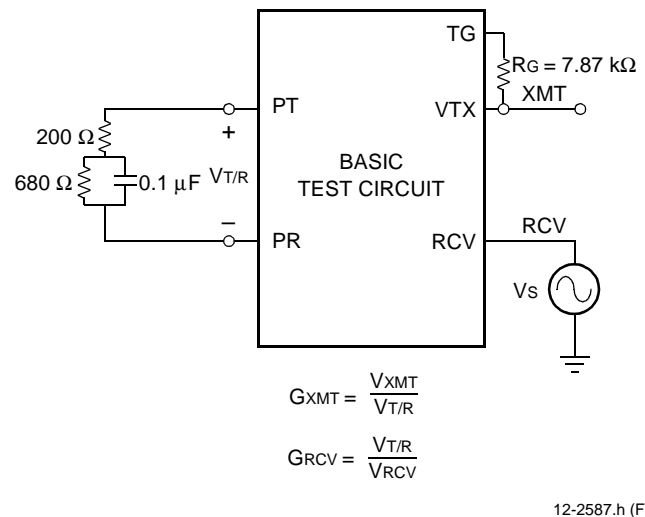
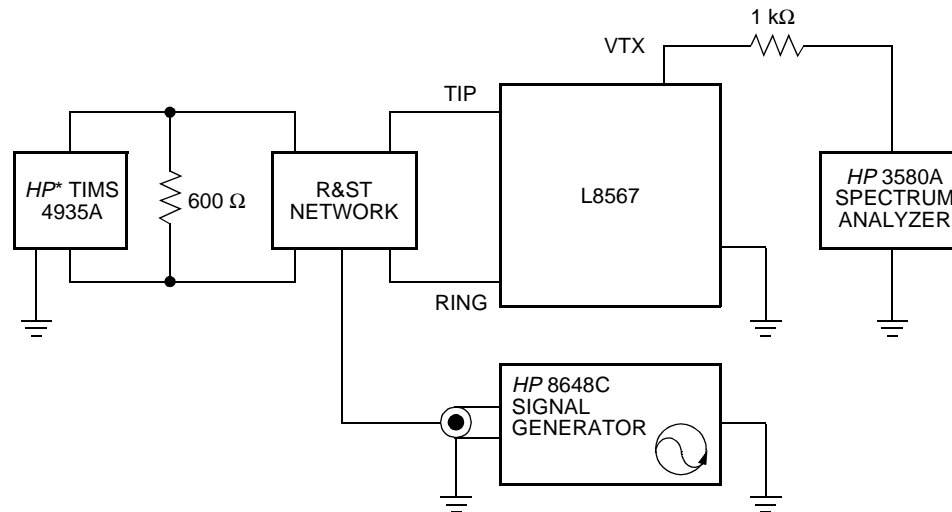


Figure 11. ac Gains

## Test Configurations (continued)

### RFI Rejection

Figures 12—14 show the typical RFI rejection performance of the L8567 under the various conditions listed within each figure title. The test circuit is shown below. The input signal is 100 kHz to 100 MHz, 1 Vrms and 2 Vrms, 80% AM, with 1 kHz side tone applied using an R&S T network (CDN). This test is performed to the IEC 801-6 (1994) specification. Note that all power supplies ( $V_{CC}$ ,  $V_{DD}$ ,  $V_{BAT}$ ) are bypassed to ground, as close as possible to the IC, with 1 nF capacitors, and all grounds are shorted on the bottom of the board as close as possible to the IC. Note that no RFI LP filter is used at tip and ring.



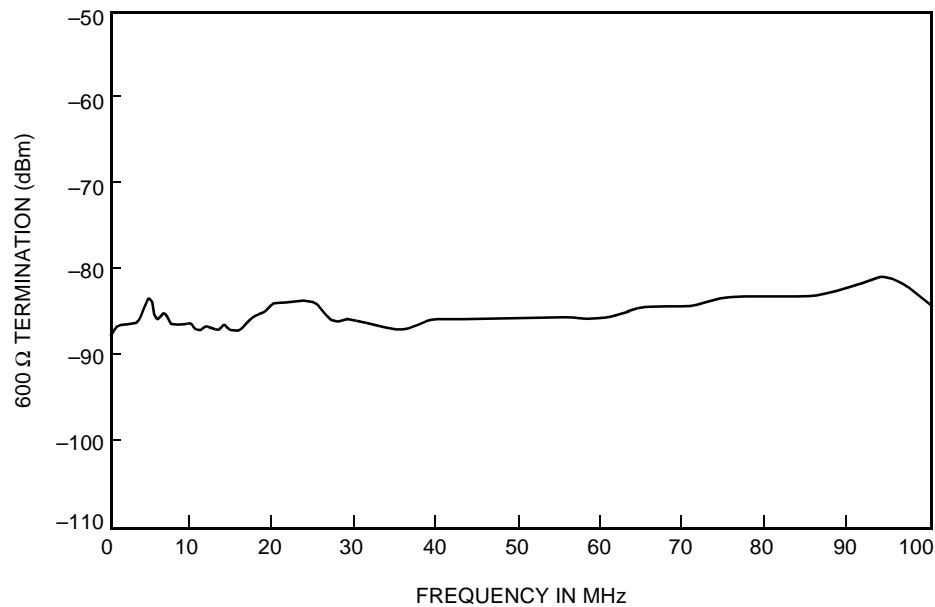
12-3456 (F)

\* HP is a registered trademark of Hewlett-Packard Company.

**Figure 12. RFI Rejection Test Circuit**

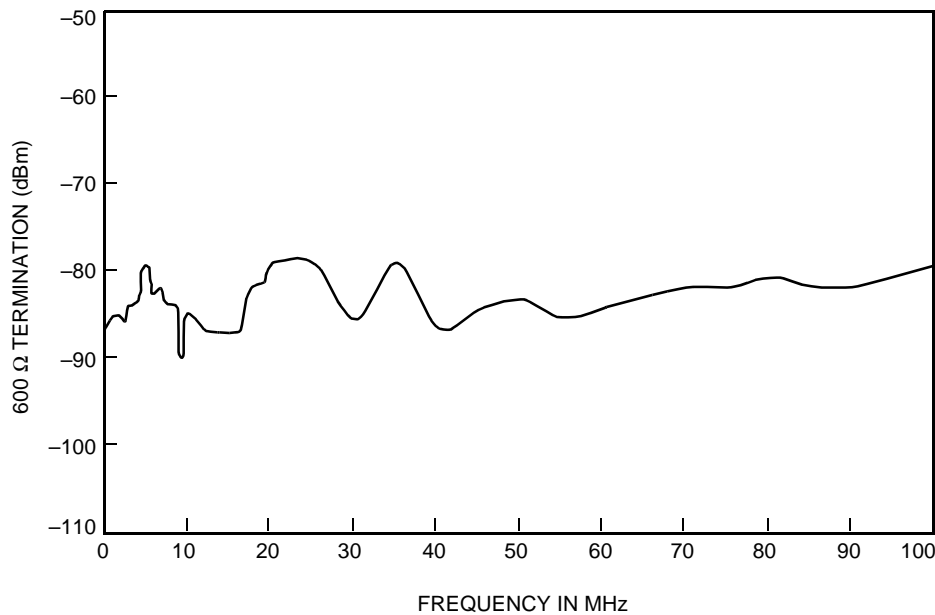
Test Configurations (continued)

RFI Rejection (continued)



12-3471a (F)

Figure 13. RFI Testing, Forward Battery, 600  $\Omega$  Loop, No Capacitor, 1 Vrms



12-3472a (F)

Figure 14. RFI Testing, Forward Battery, 600  $\Omega$  Loop, No Capacitor, 2 Vrms

## Functional Description

### General

The L8567 is a full-feature subscriber loop interface circuit (SLIC) designed to provide the battery feed and supervision functions to the tip/ring pair. The device uses a current sense/voltage feed architecture. That is, the device senses tip/ring current and supplies a precise voltage that is proportional to the tip/ring current at the VTX output. The overall transconductance (tip/ring current to VTX voltage gain) is set by a single external resistor,  $R_{TG}$ . The voltage at VTX is fed to the codec. The device feeds a precise differential voltage to tip and ring as a function of the signal voltages at the RCVN and RCVP inputs. The codec output is connected to the RCVN/RCVP SLIC inputs.

### Use with T7507 Codec for Use in People's Republic of China

The L8567 SLIC and Agere T7507 codec together form a matched device set designed to meet the specific MPT (Ministry of Post and Telecom) requirements for telephony in the People's Republic of China. The ac interface between the L8567 and the T7507 codec is extremely simple, requiring only a single dc blocking capacitor in the transmit direction, and a short-circuit connection between the codec and SLIC inputs RCVN and RCVP.

The T7507 codec has a fixed digital transmit gain stage and two digital gain stages in the receive direction. The choice of gain in the receive direction is user-selectable via a bit in the serial logic input bit stream. The transmit gain of the T7507 codec is such that when the tip/ring to VTX transconductance of the L8567 SLIC is set to  $39.75 \text{ V/A}$  ( $R_{TG} = 7.87 \text{ k}\Omega$ ), the overall tip/ring to PCM transmit gain is 0 dB into  $813 \Omega$ . (Note that  $813 \Omega$  is the equivalent resistance of the PRC complex impedance network of  $200 \Omega + 680 \Omega \parallel 100 \text{ nF}$  at 1000 Hz.) The receive gains of the T7507 codec are such that the overall PCM to tip/ring receive gain is user-selectable to either  $-3.5 \text{ dB}$  or  $-7.0 \text{ dB}$  into  $813 \Omega$ .

Note also that the T7507 codec will digitally synthesize a termination impedance of  $200 \Omega + 680 \Omega \parallel 100 \text{ nF}$ . In order to do this, the codec will assume use of  $50 \Omega$  series protection resistors, plus the resistance of the L758X Agere solid-state switch on both tip and ring. If the L758X switch is not used, the return loss performance will degrade slightly; however, it will still meet MPT standards. Gain flatness will not be affected; however, gain levels will shift less than 0.2 dB. To compensate (if desired), the resistance of the series protection resistor should be increased approximately  $20 \Omega$ , to account for the resistance of the switch.

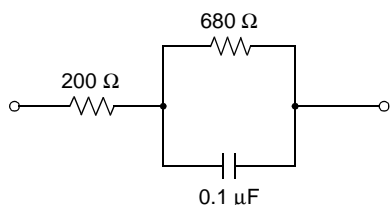
Hybrid cancellation is also done digitally by the T7507 codec, assuming a complex hybrid balance network of  $200 \Omega + 680 \Omega \parallel 100 \text{ nF}$ .

The T7507 codec operates off of a single 5 V power supply. Thus, a line card using the L8567 SLIC and T7507 codec does not require a  $-5 \text{ V}$  supply. Since the T7507 is a 5 V only device, the analog input and output of the T7507 is referenced to 2.5 V. However, the dynamic input range of the L8567 SLIC is high enough to accommodate ac signals referenced to 2.5 V, thus eliminating the need for an external dc blocking capacitor in the receive direction. The basic loop start schematic, using an L8567 SLIC, T7507 codec, and L7583 switch, for PRC termination, is shown in Figure 20.

The control logic interface of the L8567 SLIC is matched to the control logic of the T7507. The latched control inputs of the L8567 are designed to be driven by the T7507 control data outputs. The gated supervision outputs of the L8567 SLIC are designed to feed data inputs to the T7507 codec. The T7507 codec supplies the required EN pulses to the L8567 SLIC. Control data to the L8567 and supervision from the L8567 is received from, and passed to, the microcontroller at the serial data interface in the T7507 codec. See the T7507 data sheet for additional details.

## Chip Set Performance Specifications

When using the T7507 codec, L8567 SLIC, L7583 solid-state switch, and 50  $\Omega$  protection resistors, the following line card requirements are achieved; specified termination impedance is shown in Figure 15.



5-5324.a

Figure 15. Termination Impedance

## Gain

Table 12. Gain

Gain @ 1020 Hz	Min	Typ	Max	Unit
Transmit	-0.7	0	+0.3	dB
Receive*	-4.2	-3.5	-3.2	dB
Receive*	-7.7	-7.0	-6.7	dB

\* -3.5 or -7.0 gain mode programmable via the T7507 serial data interface.

## Gain Flatness—In Band

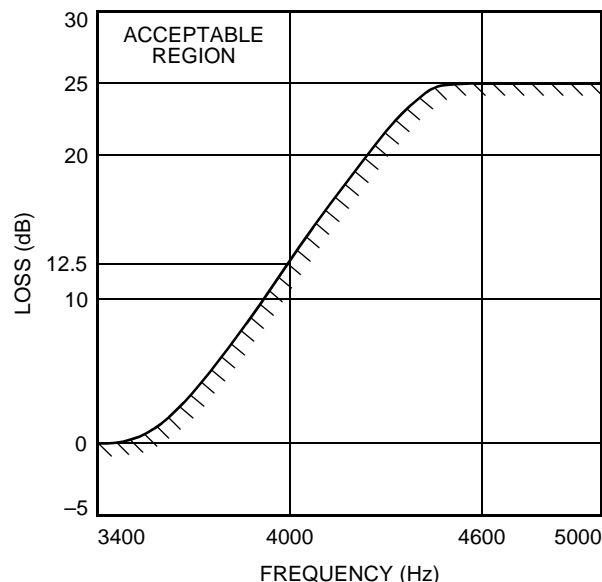
Table 13. Gain Flatness—In Band

The in-band frequency-dependent loss relative to gain at frequency = 1020 Hz, for the transmit and receive directions. This specification is met by using the T7507 codec, L8567 SLIC, L7583 solid-state switch, and 50  $\Omega$  protection resistors (200  $\Omega$  + 6800  $\Omega$  || 0.1  $\mu$ F termination).

Frequency (Hz)	Min	Max	Unit
300—400	-0.3	1.00	dB
400—600	-0.3	0.75	dB
600—2400	-0.3	0.35	dB
2400—3000	-0.3	0.55	dB
3000—3400	-0.3	1.50	dB

## Gain Flatness—Out of Band—High Frequencies

The transmit and receive directions' frequency-dependent loss relative to gain at 3400 Hz is shown below. This specification is met by using the T7507 codec, L8567 SLIC, L7583 solid-state switch, and 50  $\Omega$  protection resistors (200  $\Omega$  + 680  $\Omega$  || 0.1  $\mu$ F termination).



5-5340

Figure 16. Transmit and Receive Direction Frequency-Dependent Loss Relative to Gain at 3400 Hz

The loss for frequencies 3400 Hz < f < 4600 Hz is given by:

$$b = 12.5 \left[ 1 - \sin \frac{\pi(4000 - f)}{1200} \right] \text{dB}$$

## Gain Flatness—Out of Band—Low Frequencies

Table 14. Gain Flatness—Out of Band—Low Frequencies

Transmit direction only, loss relative to 1020 Hz. This specification is met by using the T7507 codec, L8567 SLIC, L7583 solid-state switch, and 50  $\Omega$  protection resistors (200  $\Omega$  + 680  $\Omega$  || 0.1  $\mu$ F termination).

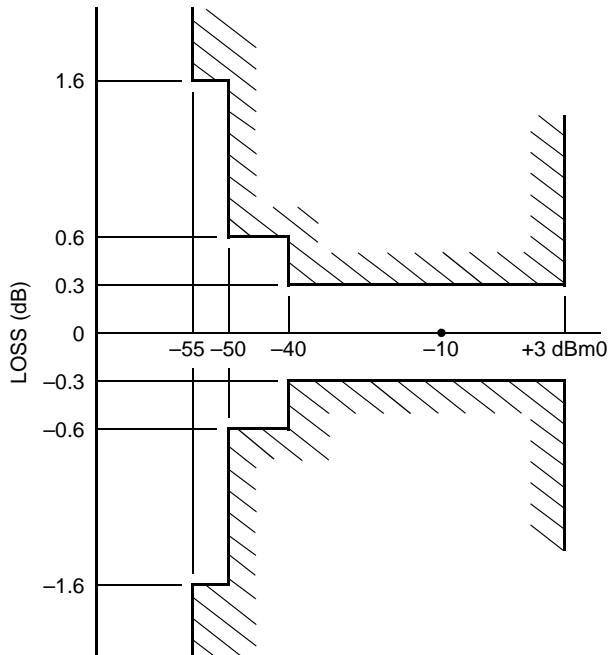
Frequency (Hz)	Min Loss (dB)
16.67	30
40	26
50	30
60	30

## Chip Set Performance Specifications

(continued)

### Loss vs. Level Relative to Loss at -10 dBm Input at 1020 Hz

This specification is met by using the T7507 codec, L8567 SLIC, L7583 solid-state switch, and 50  $\Omega$  protection resistors (200  $\Omega$  + 680  $\Omega$  || 0.1  $\mu$ F termination).

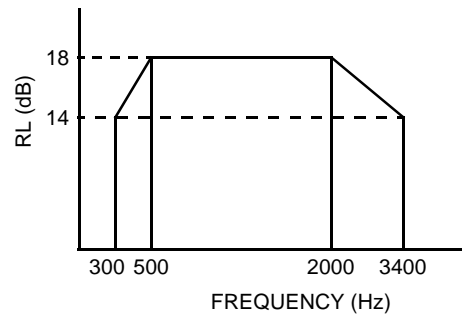


5-5341

Figure 17. Loss vs. Level

## Return Loss

The following template is achieved.

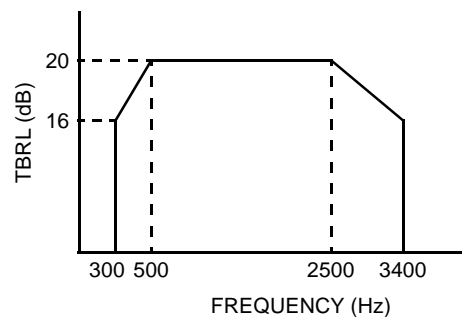


5-5325

Figure 18. Return Loss

## Hybrid Balance

The following template is achieved.



5-5326

Figure 19. Hybrid Balance

[illegible]

12-3366a (F)



**Applications** (continued)**Table 15. Parts List for Loop Start Application**

Name	Value	Function
<b>Integrated Circuits</b>		
SLIC	L8567	Subscriber loop interface circuit (SLIC).
Protector	Crowbar Protector <sup>1</sup>	Secondary protection.
Ringing and Test Access	L7583B	Switches ringing signals and test buses.
Codec	T7507	Transmit/receive gains, termination impedance, hybrid balance, D/A, A/D, and filtering.
<b>Overvoltage Protection</b>		
R <sub>PT</sub>	50 $\Omega$	Protection resistor. PTC or fusible.
R <sub>PR</sub>	50 $\Omega$	Protection resistor. PTC or fusible.
<b>Power Supply</b>		
C <sub>BAT1/CBAT2</sub>	0.1 $\mu$ F, 20%, 100 V	V <sub>BAT</sub> filter capacitors.
C <sub>CC</sub>	0.1 $\mu$ F, 20%, 10 V	V <sub>CC</sub> filter.
C <sub>DD</sub>	0.1 $\mu$ F, 20%, 10 V	V <sub>DD</sub> filter.
C <sub>F1</sub>	0.47 $\mu$ F, 20%, 100 V	With C <sub>F2</sub> , improves idle-channel noise.
C <sub>F2</sub>	0.1 $\mu$ F, 20%, 100 V	With C <sub>F1</sub> , improves idle-channel noise.
<b>dc Profile</b>		
R <sub>PROG</sub>	63.4 k $\Omega$ , 1%, 1/16 W	Sets dc loop current limit.
R <sub>PWR</sub> (with single battery supply)	2.2 k $\Omega$ , 5%, 2 W	Limits power dissipated on the SLIC, provides dc power to the loop.
<b>ac Characteristics</b>		
C <sub>B2</sub>	0.1 $\mu$ F, 20%, 100 V	ac/dc separation capacitor.
R <sub>TG</sub>	7.87 k $\Omega$ , 1%, 1/16 W	Sets SLIC transconductance.
<b>Supervision</b>		
R <sub>TS1</sub>	402 $\Omega$ , 5%, 2 W	Ringing source series resistor.
R <sub>TS2</sub>	274 k $\Omega$ , 1%, 1/16 W	With C <sub>RTS2</sub> , forms first pole of a double pole, 2 Hz ring trip sense filter.
C <sub>RTS1</sub>	0.022 $\mu$ F, 20%, 5 V	With R <sub>TSN</sub> , R <sub>TSP</sub> , forms second 2 Hz filter pole.
C <sub>RTS2</sub>	0.27 $\mu$ F, 20%, 100 V	With R <sub>TS2</sub> , forms first 2 Hz filter pole.
R <sub>TSN</sub>	2 M $\Omega$ , 1%, 1/16 W	With C <sub>RTS1</sub> , R <sub>TSP</sub> , forms second 2 Hz filter pole.
R <sub>TSP</sub>	2 M $\Omega$ , 1%, 1/16 W	With C <sub>RTS1</sub> , R <sub>TSN</sub> , forms second 2 Hz filter pole.

1. Contact your Agere account representative for protector recommendations. Choice of this (and all) component(s) should be evaluated and confirmed by the customer prior to use in any field or laboratory system. Agere does not recommend use of this part in the field without performance verification by the customer. This device is suggested by Agere for customer evaluation. The decision to use a component should be based solely on customer evaluation.

## Applications (continued)

### Design Considerations

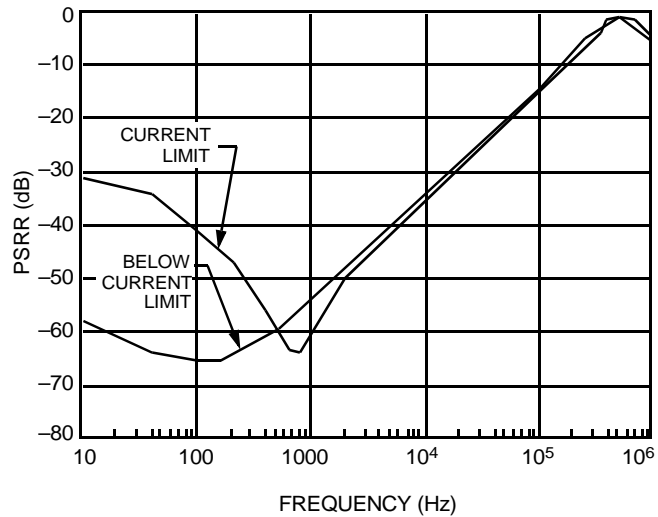
Table 16 shows the design parameters of the application circuit shown in Figure 20. Components that are adjusted to program these values are also shown.

**Table 16.  $200\ \Omega + 680\ \Omega \parallel 0.1\ \mu\text{F}$  Design Parameters**

Design Parameter	Parameter Value	Components Adjusted
Loop Closure Threshold	11 mA	—
dc Loop Current Limit	40 mA	R <sub>PROG</sub>
dc Feed Resistance	246 $\Omega$	R <sub>PT</sub> , R <sub>PR</sub> , L7583
2-wire Signal Overload Level	3.17 dBm	—
ac Termination Impedance	$200\ \Omega + 680\ \Omega \parallel 0.1\ \mu\text{F}$	Set via T7507
Hybrid Balance Line Impedance	$200\ \Omega + 680\ \Omega \parallel 0.1\ \mu\text{F}$	Set via T7507
Transmit Gain	0 dB	Set via T7507
Receive Gain	–3.5 dB/–7.0 dB	Set via T7507

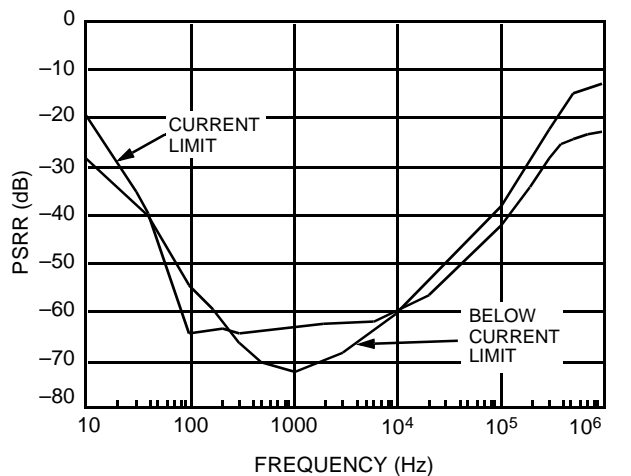
## Applications (continued)

### Characteristic Curves



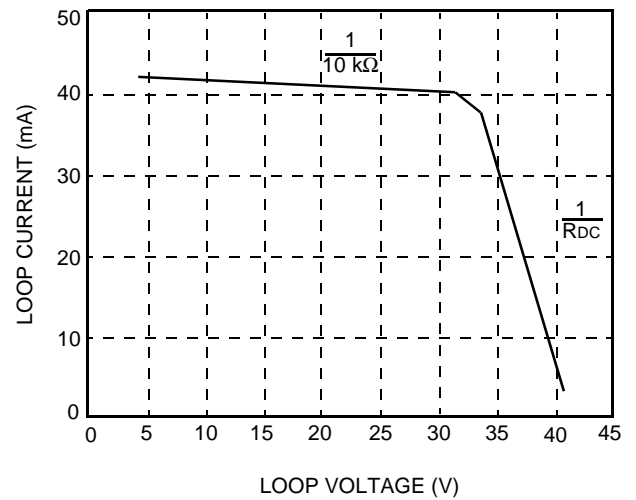
12-2830 (F)

**Figure 21. L8567 Typical  $V_{CC}$  Power Supply Rejection**



12-2871 (F)

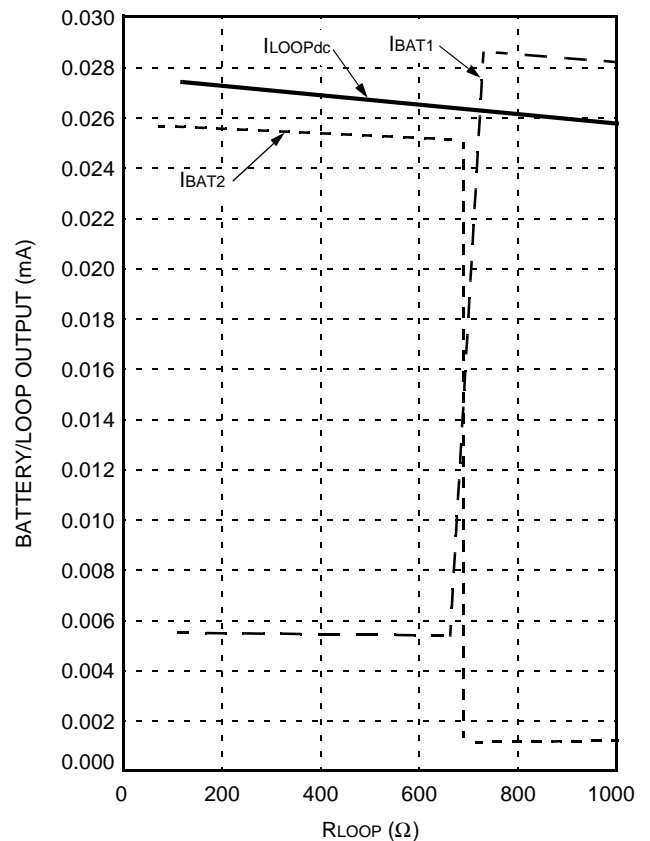
**Figure 22. L8567 Typical  $V_{BAT}$  Power Supply Rejection**



12-3050.g (F)

$V_{BAT1} = V_{BAT2} = -48$  V.  
 $I_{LIM} = 40$  mA ( $R_{PROG} = 66.5$  k $\Omega$ ).

**Figure 23. L8567 Loop Current vs. Loop Voltage**

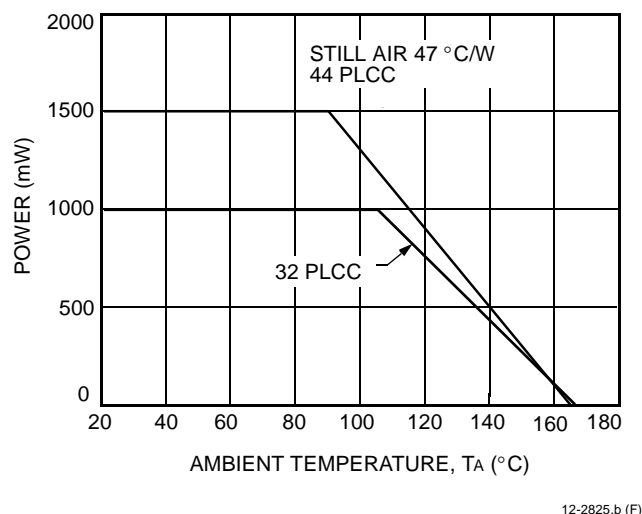


12-3470 (F)

**Figure 24. L8567 Loop/Battery Current (with Battery Switch) vs. Loop Resistance**

## Applications (continued)

### Characteristic Curves (continued)



Note: Curve is relevant only to portion of total power dissipation that is actually dissipated on the SLIC.

Figure 25. Power Derating

## Power Control

The total power drawn from the talk battery during an off-hook state is the product of the battery voltage times the total dc loop current, plus the SLIC quiescent power dissipation. Note that during the on-hook state, the power is simply the SLIC quiescent power.

$$P_{TOTAL(off-hook)} = V_{BAT} \cdot I_{LOOP} + P_{SLIC(quietent)}$$

A portion of the total power is dissipated in the subscriber loop, and a portion of the total power is dissipated in the SLIC itself. The loop power is used to drive the handset and is given by:

$$P_{LOOP} = I_{LOOP}^2 \cdot R_{LOOP}$$

$I_{LOOP}$  is the dc loop current. In the short dc loops, the dc loop current will be limited by the SLIC. In the case of the L8567 SLIC, the dc loop current is determined by external resistor  $R_{PROG}$ .  $R_{LOOP}$  is the sum of the actual loop resistance (wire resistance and dc handset resistance) plus any protection or other series resistance.

The active or off-hook power dissipated in the SLIC is simply the difference of the total power drawn from the talk battery, less the loop power, less the SLIC quiescent or on-hook power.

$$P_{SLIC(active)} = P_{TOTAL} - P_{LOOP} - P_{SLIC(on-hook)}$$

If the active power dissipated in the SLIC is too high, the SLIC temperature will rise above the thermal shutdown threshold and the SLIC will be driven into a thermal shutdown state. The worst case is under short dc loops at elevated ambient temperatures. The power dissipated on the SLIC must be controlled to avoid forcing the SLIC into thermal shutdown during an active phone conversation.

With the L8567 SLIC, short-loop power dissipation may be controlled using several user-selectable techniques. The first involves use of a lower-voltage auxiliary battery. This will reduce the total short-loop off-hook power. This has the advantage of not only controlling the SLIC temperature rise, but also minimizing total power drawn from the talk battery.

If the user chooses not to provide an auxiliary battery, the power dissipated by the SLIC must be controlled in some other manner. With the L8567 SLIC, this may be done in two ways. One technique involves the use of a single external power control resistor. This technique does not minimize total power dissipation; rather it controls the power that it is dissipating through the SLIC package by removing some power from the SLIC through the resistor, thus avoiding excess temperature rise. Because of the higher thermal impedance associated with the 32-pin PLCC, this technique may be necessary with the 32-pin PLCC package option.

The other technique is simply to choose the 44-pin PLCC package option. The thermal resistance of the 44-pin PLCC is low enough to ensure, under most conditions, that the thermal shutdown temperature of the SLIC is not exceeded. Power dissipation calculations should be made to assess design margin.

For the three configurations discussed above, connections to the  $V_{BAT1}$ ,  $V_{BAT2}$ , and  $PWR$  nodes are outlined in the table below.

Table 17. Power Connections

Option	Connections to Power Mode		
	$V_{BAT1}$	$V_{BAT2}$	$PWR$
32 PLCC with auxiliary battery	$V_{BAT1}$	$V_{BAT2}$	$V_{BAT2}$
32 PLCC with high-voltage battery and power resistor	$V_{BAT1}$	$V_{BAT1}$	$V_{BAT1}$ through power control resistor
44 PLCC with high-voltage battery	$V_{BAT1}$	$V_{BAT1}$	$V_{BAT1}$

## Applications (continued)

### Power Control—Auxiliary Battery

With the auxiliary battery technique under long loops, the entire L8567 draws power from the higher-voltage battery. As the loop length decreases and the loop current increases or limits, the final output drive stage of the L8567 SLIC will draw power from the lower-voltage auxiliary battery. Thus, for a given loop, with a given loop current requirement, the minimum battery voltage is used by the L8567 SLIC, which minimizes the total power consumed. During on-hook or open-circuit conditions, the high battery is seen at tip and ring.

All circuits on the L8567, other than the final output drive stage, are powered by the higher-voltage battery regardless of dc loop length. Thus, SLIC quiescent power will be determined solely by the high-voltage battery and will not be reduced under short dc loops.

Tip/ring voltage varies as a function of loop length, decreasing with decreasing loop length. The battery transition will occur when the tip/ring voltage is less than  $V_{BAT2}$  by a diode drop and a  $V_{CE(SAT)}$ , or about 1 V.

Thus, the transition point from  $V_{BAT1}$  to  $V_{BAT2}$  may be controlled by the choice of  $V_{BAT2}$ . The relationship is given below:

$$V_{BAT2} = T_{OH} + R_{DC(TIP)} \cdot I_{LOOP} + 2 \cdot R_{PROT} \cdot I_{LOOP} + R_{LOOP} \cdot I_{LIM} + R_{DC(RING)} \cdot I_{LIM} + (V_{DIODE} + V_{CE(SAT)})$$

where:

$V_{BAT2}$  = magnitude of auxiliary battery.

$T_{OH}$  = overhead voltage tip to ground, typically 2.5 V.

$R_{DC(TIP)}$  = dc feed resistance on tip, typically 55  $\Omega$ .

$I_{LOOP}$  = loop current.  $V_{BAT2}$  will switch under short-loop conditions where it is likely that the SLIC will be current limiting; thus,  $I_{LOOP} = I_{LIM}$ .

$R_{PROT}$  = series protection resistance plus L758X resistance, nominal 68  $\Omega$ .

$R_{LOOP}$  = loop resistance for transition from  $V_{BAT1}$  to  $V_{BAT2}$ .

$I_{LIM}$  = SLIC current limit set per resistor  $R_{LIM}$ .

$R_{DC(RING)}$  = dc feed resistance on ring, typically 55  $\Omega$ .

$(V_{DIODE} + V_{CE(SAT)})$  = internal voltage drop associated with battery switch circuit, typically 1 V.

Thus, the equation may be rewritten:

$$V_{BAT2} = 2.5 \text{ V} + 55 I_{LIM} + 132 I_{LIM} + R_{LOOP} I_{LIM} + 55 I_{LIM} + 1 \text{ V}$$

$$R_{LOOP} = \frac{V_{BAT2} - 3.5}{I_{LIM}} - 242 \Omega$$

Thus, for example, for a nominal loop transition at 700  $\Omega$ , with a 25 mA current limit,  $V_{BAT2}$  should be nominal 27 V.

### Power Control—32-Pin PLCC with Power Control Resistor

This section is applicable if the user chooses to use a single high-voltage battery with an external power control resistor. The power resistor is used in conjunction with the 32-pin PLCC package.

Resistor  $R_{PWR}$  is connected from pin PWR to the battery supply. This resistor limits the power that is dissipated on the SLIC. dc loop current is shared between the SLIC and  $R_{PWR}$ , thus controlling the actual power that is dissipated on the SLIC. The value and power rating of  $R_{PWR}$  is determined by the thermal capabilities of the L8567's 32-pin PLCC package. The value and power rating of  $R_{PWR}$  is calculated as shown below.

The relationship for the power dissipated in the SLIC is given by:

$$P_{SLIC} = P_{TOTAL} + P_Q - P_{PROT} - P_{PWR} - P_{LOOP} \quad (1)$$

Where:

$P_{SLIC}$  = the power dissipated in the SLIC.

$P_{TOTAL}$  = the total off-hook power dissipation.

$P_Q$  = the SLIC quiescent or on-hook power dissipation.

$P_{PROT}$  = the power dissipated in the protection resistors (and L758X switch).

$P_{PWR}$  = the power dissipated in  $R_{PWR}$ .

$P_{LOOP}$  = the power dissipated in the subscriber loop.

The relationships for the individual power dissipation components are:

$$P_{TOTAL} = I_{LOOP} \cdot |V_{BAT}| \quad (2)$$

$P_Q$  is the active state open loop power dissipation of the L8567 SLIC and is specified in Table 4 on page 12.

$$P_{PROT} = (I_{LOOP})^2 \cdot 2R_P \quad (3)$$

$$P_{PWR} = \frac{(|V_{BAT}| - V_{ROH} - V_{LOOP})^2}{(R_{PWR})} \quad (4)$$

$$P_{LOOP} = V_{LOOP} \cdot I_{LOOP} \quad (5)$$

Where:

$I_{LOOP}$  is the maximum dc loop current which is the dc loop current limit that is set by resistor  $R_{PROG}$ .

$R_P$  is the value of the protection resistor plus the resistance of the L758X switch.

$|V_{BAT}|$  is the magnitude of the maximum battery voltage.

$V_{ROH}$  is the overhead voltage associated with the ring lead.

$V_{LOOP}$  is the ring/tip loop voltage. This voltage is a function of the dc loop length or resistance. It will decrease with decreasing loop resistance.

$R_{PWR}$  is the resistance of the external resistor  $R_{PWR}$ .

## Applications (continued)

### Power Control—32-Pin PLCC with Power Control Resistor (continued)

The maximum power that may be dissipated in the SLIC,  $P_{SLIC(MAX)}$  is given by

$$T_{TSD} - T_A = T_{RISE} \quad (6)$$

$$P_{SLIC(MAX)} = \frac{T_{RISE}}{\Theta_{JA}} \quad (7)$$

Where:

$T_{TSD}$  is the thermal protection shutdown temperature and is specified in Table 4.

$T_A$  is the maximum ambient operating temperature.

$T_{RISE}$  is the maximum allowed SLIC temperature rise to avoid driving the SLIC into thermal shutdown.

$P_{SLIC(MAX)}$  is the maximum allowed power that is dissipated on the SLIC to avoid driving the SLIC into thermal shutdown.

$\Theta_{JA}$  is the thermal resistance, junction to ambient of the 32-pin PLCC package; it is specified in Table 4 on page 12.

The approach to choosing the value and rating of  $R_{PWR}$  follows. First use equations 6 and 7 to determine the maximum allowed power that may be dissipated on the SLIC without driving the SLIC into thermal shutdown.

Next consider equations 1 and 4. In both equation 1 and 4, pick a value of  $R_{PWR}$  and for this value, or  $R_{PWR}$ , vary  $V_{LOOP}$  from the open-circuit (on-hook) state voltage to the voltage seen at the minimum expected dc loop length (100  $\Omega$ ). The idea is to use the SLIC power dissipation value from equation 1,  $P_{SLIC}$ , to ensure that the maximum SLIC power dissipation value from equation 7,  $P_{SLIC(MAX)}$ , is not exceeded for any value of loop length. At the same time, using equation 4, try to minimize the power dissipated in  $R_{PWR}$  so as to choose the minimum power rating of the resistor to minimize cost associated with this resistor. This technique is illustrated in the following design example.

## Power Considerations

$R_{PWR}$  Design Example:

Assume  $I_{LOOP} = 45$  mA. This assumes that a 40 mA current limit is programmed by resistor  $R_{PROG}$  set at 63.4 k $\Omega$ , plus a worst-case 15% tolerance that is specified in Table 5.

$$|V_{BAT}| = 56 \text{ V.}$$

$2R_P = 136 \Omega$ . This assumes use of 50  $\Omega$  PTC in both the tip and ring lead associated with the L7583 ON resistance.

$$V_{ROH} = 4 \text{ V (typical).}$$

$P_Q = 165$  mW as nominally specified in Table 4.

$T_{TSD} = 165$  °C per Table 4.

$$T_A = 85 \text{ °C.}$$

$$\Theta_{JA} = 60 \text{ °C/W per Table 4.}$$

$V_{LOOP}$  is varied from the open-circuit voltage of approximately 50 V to the voltage at a 100  $\Omega$  loop length, approximately 5 V.

First, using equations 6 and 7, calculate the maximum allowed power dissipation in the SLIC.

$$T_{TSD} - T_A = T_{RISE} \quad (6)$$

$$165 \text{ °C} - 85 \text{ °C} = 80 \text{ °C}$$

$$P_{SLIC(MAX)} = \frac{T_{RISE}}{\Theta_{JA}} \quad (7)$$

$$P_{SLIC(MAX)} = \frac{80 \text{ °C}}{60 \text{ °C}} = 1.33 \text{ W}$$

Given the choice of  $R_{PWR}$  chosen, the value of  $P_{SLIC}$  in equation 8 must be less than 1.33 W for all loop lengths (all values of  $V_{LOOP}$  in equation 1). At the same time,  $R_{PWR}$  should be chosen to minimize  $P_{PRW}$  from equation 4.

Inserting values into equation 1:

$$P_{SLIC} \leq P_{TOTAL} + P_Q - P_{PROT} - P_{PWR} - P_{LOOP} \quad (8)$$

From equation 2, 3, 4, 5

$$P_{SLIC} \leq I_{LOOP} \cdot |V_{BAT}| + P_Q - (I_{LOOP})^2 \cdot$$

$$2R_P - \frac{(|V_{BAT}| - V_{ROH} - V_{LOOP})^2}{R_{PWR}} - V_{LOOP} \cdot I_{LOOP}$$

Inserting values:

$$1.33 \text{ W} < (0.045)(56) + 0.165 \text{ W} - [(0.045)^2 \cdot$$

$$2(50 + 18)] - \frac{(|56| - 4 - V_{LOOP})^2}{R_{PWR}} -$$

$$(V_{LOOP})(0.045 \text{ mA}) \quad (9)$$

## Applications (continued)

### Power Considerations (continued)

Inserting values into equation 4:

$$P_{PWR} = \frac{(|V_{BAT}| - V_{ROH} - V_{LOOP})^2}{R_{PWR}}$$

$$P_{PWR} = \frac{(|56| - 4 - V_{LOOP})^2}{R_{PWR}} \quad (10)$$

At this point, the idea is to choose a value of  $R_{PWR}$ , and vary  $V_{LOOP}$  from the on-hook value of approximately 50 V to the very short loop (~100  $\Omega$ ) value of 5 V in both equations 9 and 10. For the choice of  $R_{PWR}$ , the relationship in equation 9 must be met to ensure that sufficient power is dissipated in  $R_{PWR}$  to ensure that L8567 SLIC is not driven into thermal shutdown.

At the same time, for the choice of  $R_{PWR}$ , equation 10 will tell what the power rating of  $R_{PWR}$  needs to be. Obviously, it is desirable to minimize  $P_{PWR}$  in equation 10 to minimize the cost associated with component  $R_{PWR}$ .

An easy way to vary  $V_{LOOP}$  for various values of  $R_{PWR}$  is to use a computer-based spreadsheet program.

Table 18 shows a spreadsheet for the choice of  $R_{PWR} = 2600 \Omega$ . As shown, for this choice of resistor under short loop conditions, the power dissipated in the SLIC exceeds 1.33 W; thus, the SLIC may be driven into thermal shutdown. Therefore, 2600  $\Omega$  is not an appropriate choice of  $R_{PWR}$ .

In Table 19,  $R_{PWR}$  was reduced to 2200  $\Omega$ . As shown in this spreadsheet, under no loop conditions does the SLIC power dissipation exceed 1.33 W. Thus, in terms of SLIC power dissipation, 2200  $\Omega$  is an appropriate choice. Looking at the power dissipated in resistor  $R_{PWR}$ , the maximum power dissipation is 0.96 W, which says a rating of 2 W (with margin) is appropriate for 2200  $\Omega$ .

In Table 20,  $R_{PWR}$  was further reduced to 1800  $\Omega$ . Again, with this choice, the SLIC power does not exceed 1.33 W, so in terms of SLIC power dissipation, 1800  $\Omega$  is also an appropriate choice. However, with 1800  $\Omega$ , the power dissipated in  $R_{PWR}$  under short loop conditions exceeds 1 W, which suggests that for 1800  $\Omega$ , the power rating of  $R_{PWR}$  should be greater than 2 W. Thus, while 1800  $\Omega$  ensures the SLIC will not be driven into thermal shutdown, because of the higher power rating required compared to 2200  $\Omega$ , 2200  $\Omega$  is a better choice.

In Table 21,  $R_{PWR}$  was increased to 4400  $\Omega$ . This is the minimum value to get the power rating of  $R_{PWR}$  to a 0.5 W resistor. However, with this choice of resistor, the

SLIC power will exceed 1.33 W; thus, 4400  $\Omega$  is not appropriate. This result suggests that the minimum power rating of  $R_{PWR}$  under the assumed conditions is 1 W.

Table 22 and Table 23 show results for 2200  $\Omega$  with a +5% and -5% variation, respectively. These tables suggest that a 5% tolerance is adequate for  $R_{PWR}$ .

**Table 18.  $R_{PWR} = 2600 \Omega$**

PSLIC (W)	VLOOP (V)	RPWR ( $\Omega$ )	PPWR (W)
1.334985	5	2600	0.849615
1.281138	10	2600	0.678462
1.208062	15	2600	0.526538
1.115754	20	2600	0.393846
1.004215	25	2600	0.280385
0.873446	30	2600	0.186154
0.723446	35	2600	0.111154
0.554215	40	2600	0.055385
0.365754	45	2600	0.018846
0.158062	50	2600	0.001538

**Table 19.  $R_{PWR} = 2200 \Omega$**

PSLIC (W)	VLOOP (V)	RPWR ( $\Omega$ )	PPWR (W)
1.180509	5	2200	1.004091
1.157782	10	2200	0.801818
1.112327	15	2200	0.622273
1.044145	20	2200	0.465455
0.953236	25	2200	0.331364
0.8396	30	2200	0.22
0.703236	35	2200	0.131364
0.544145	40	2200	0.065455
0.362327	45	2200	0.022273
0.157782	50	2200	0.001818

**Table 20.  $R_{PWR} = 1800 \Omega$**

PSLIC (W)	VLOOP (V)	RPWR ( $\Omega$ )	PPWR (W)
0.957378	5	1800	1.227222
0.9796	10	1800	0.98
0.974044	15	1800	0.760556
0.940711	20	1800	0.568889
0.8796	25	1800	0.405
0.790711	30	1800	0.268889
0.674044	35	1800	0.160556
0.5296	40	1800	0.08
0.357378	45	1800	0.027222
0.157378	50	1800	0.002222

## Applications (continued)

### Power Considerations (continued)

Table 21. RPWR = 4400  $\Omega$

PSLIC (W)	VLOOP (V)	RPWR ( $\Omega$ )	PPWR (W)
1.682555	5	4400	0.502045
1.558691	10	4400	0.400909
1.423464	15	4400	0.311136
1.276873	20	4400	0.232727
1.118918	25	4400	0.165682
0.9496	30	4400	0.11
0.768918	35	4400	0.065682
0.576873	40	4400	0.032727
0.373464	45	4400	0.011136
0.158691	50	4400	0.000909

Table 22. RPWR = 2310  $\Omega$  (RPWR = 2200  $\Omega$  + 5%)

PSLIC (W)	VLOOP (V)	RPWR ( $\Omega$ )	PPWR (W)
1.228323	5	2310	0.956277
1.195964	10	2310	0.763636
1.141959	15	2310	0.592641
1.06631	20	2310	0.44329
0.969016	25	2310	0.315584
0.850076	30	2310	0.209524
0.709492	35	2310	0.125108
0.547262	40	2310	0.062338
0.363388	45	2310	0.021212
0.157868	50	2310	0.001732

Table 23. RPWR = 2090  $\Omega$  (RPWR = 2200  $\Omega$  - 5%)

PSLIC (W)	VLOOP (V)	RPWR ( $\Omega$ )	PPWR (W)
1.127662	5	2090	1.056938
1.115581	10	2090	0.844019
1.079576	15	2090	0.655024
1.019648	20	2090	0.489952
0.935796	25	2090	0.348804
0.828021	30	2090	0.231579
0.696322	35	2090	0.138278
0.5407	40	2090	0.0689
0.361155	45	2090	0.023445
0.157686	50	2090	0.001914

## Power Control—44-Pin PLCC Package

With the 44-pin PLCC, the thermal impedance of the package is probably enough to ensure the SLIC thermal shutdown temperature is not exceeded. Power calculations, as illustrated below, should be made to ensure design margin.

The still-air thermal resistance of the 44-pin PLCC is 47  $^{\circ}\text{C}/\text{W}$ ; however, this number implies zero airflow as if the L8567 were totally enclosed in a box. A more realistic number would be 43  $^{\circ}\text{C}/\text{W}$ . This is an experimental number that represents a thermal impedance with no forced airflow (i.e., from a muffin fan), but from the natural airflow as seen in a typical switch cabinet.

The SLIC will enter the thermal shutdown state at typically 165  $^{\circ}\text{C}$ . The thermal shutdown design should ensure that the SLIC temperature does not reach 165  $^{\circ}\text{C}$  under normal operating conditions.

Assume a maximum ambient operating temperature of 85  $^{\circ}\text{C}$ , a maximum current limit of 45 mA, and a maximum battery of -52 V. Further, assume a (worst case) minimum dc loop of 100  $\Omega$  and that 100  $\Omega$  protection resistors are used at both tip and ring.

1.  $T_{\text{TSD}} - T_{\text{A(max)}} = \text{allowed thermal rise.}$   
165  $^{\circ}\text{C} - 85^{\circ}\text{C} = 80^{\circ}\text{C}$
2. Allowed thermal rise = package thermal impedance • SLIC power dissipation.  
80  $^{\circ}\text{C} = 43^{\circ}\text{C}/\text{W} \bullet \text{SLIC power dissipation}$   
SLIC power dissipation ( $P_{\text{D}}$ ) = 1.9 W

Thus, if the total power dissipated in the SLIC is less than 1.9 W, it will not enter the thermal shutdown state. Total SLIC power is calculated as:

$$\text{Total } P_{\text{D}} = \text{Maximum battery} \bullet \text{Maximum current limit} + \text{SLIC quiescent power.}$$

For the L8567, SLIC quiescent power ( $P_{\text{Q}}$ ) is approximated at 0.167 W. Thus,

$$\text{Total } P_{\text{D}} = (-52 \text{ V} \bullet 45 \text{ mA}) + 0.167 \text{ W}$$

$$\text{Total } P_{\text{D}} = 2.34 \text{ W} + 0.167 \text{ W}$$

$$\text{Total } P_{\text{D}} = 2.507 \text{ W}$$

The power dissipated in the SLIC is the total power dissipation less the power that is dissipated in the loop.

$$\text{SLIC } P_{\text{D}} = \text{Total power} - \text{Loop power}$$

$$\text{Loop power} = (I_{\text{LIM}})^2 \bullet (R_{\text{dcLOOP min}} + 2R_{\text{P}})$$

$$\text{Loop power} = (45 \text{ mA})^2 \bullet (100 \Omega + 200 \Omega)$$

$$\text{Loop power} = 0.61 \text{ W}$$

$$\text{SLIC power} = 2.507 \text{ W} - 0.61 \text{ W}$$

$$\text{SLIC power} = 1.897 \text{ W} < 1.9 \text{ W}$$

Thus, in this example, the thermal design ensures that the SLIC will not enter the thermal shutdown state.



## dc Characteristics

The L8567 SLIC operates in a dc unbalanced mode. In the forward active state, under open-circuit (on-hook) conditions, the tip to ring voltage will be a nominal 7.1 V less than the battery. This is the overhead voltage. The tip and ring overhead is achieved by biasing ring a nominal 4.6 V above battery and by biasing tip a nominal 2.5 V below ground.

During off-hook conditions, some dc resistance will be applied to the subscriber loop as a function of the physical loop length, protection, and telephone handset. As the dc resistance decreases from infinity (on-hook) to some finite value (off-hook), the tip to ring voltage will decrease as shown below.

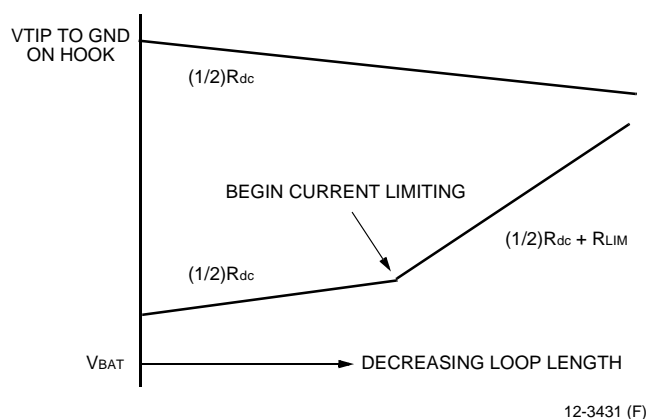


Figure 26. Tip/Ring Voltage Decrease

As illustrated above, as loop length decreases, the tip to ground voltage will decrease with a slope corresponding to one-half the internal dc feed resistance of the SLIC. (The L8567 dc feed resistance is a nominal 110 Ω.) The ring to ground voltage will also decrease with a slope corresponding to one-half the internal dc feed resistance of the SLIC, until the SLIC reaches the current-limit region of operation. At that point, the slope of the ring to ground voltage will increase to the sum of one-half the internal dc feed resistance of the SLIC plus approximately 10 kΩ, which is the slope of the I/V characteristic in the current-limit region.

The dc feed characteristic can be described by:

$$I_L = \frac{|V_{BAT}| - V_{OH}}{R_L + 2R_P + R_{dc}}$$

$$V_{T/R} = \frac{(|V_{BAT}| - V_{OH}) \times R_L}{R_L + 2R_P + R_{dc}}$$

Where:

$I_L$  = dc loop current.

$V_{T/R}$  = dc loop voltage.

$|V_{BAT}|$  = battery voltage magnitude.

$V_{OH}$  = overhead voltage. This is the difference between the battery voltage and the open loop tip/ring voltage.

$R_L$  = loop resistance, not including protection resistors.

$R_P$  = protection resistor value.

$R_{dc}$  = SLIC internal dc feed resistance.

The design begins by drawing the desired dc template.

Refer to Figures 23, 24, and 26.

Starting from the on-hook condition and going through to a short circuit, the curve passes through two regions:

Region 1; On-hook and low loop currents: The slope corresponds to the dc resistance of the SLIC,  $R_{dc1}$  (plus any series resistance). The open-circuit voltage is the battery voltage less the overhead voltage of the device,  $V_{OH}$  (7.0 V typical).

Region 2; Current limit: The dc current is limited to a value determined by external resistor  $R_{PROG}$ . This region of the dc template has a high resistance (10 kΩ).

Calculate the external resistor as follows:

$$R_{PROG} (k\Omega) = 1.59 I_{LIM} (mA)$$

Notice that the I/V curve is uninterrupted when the power is shifted from the high-voltage battery to the low-voltage battery (if auxiliary battery option is used), if the transition occurs in the current-limit region of operation. This is shown in Figure 24.

## dc Characteristics (continued)

### Loop Range

The following equation is used to determine the dc loop range.

$$R_L = \frac{|V_{BAT}| - V_{OH}}{I_L} - 2R_P - R_{dc}$$

Where:

$R_L$  = dc loop range.

$|V_{BAT}|$  = magnitude of battery voltage.

$V_{OH}$  = SLIC overhead voltage.

$I_L$  = dc loop current.

$R_P$  = series protection resistor and resistance of L758X solid-state switch (if used).

$R_{dc}$  = SLIC dc feed resistance.

#### Example 1, Standard Loop:

Calculate loop range with battery voltage of 48 V, SLIC maximum overhead of 7.8 V, SLIC dc feed resistance of 65  $\Omega$ , 18 mA loop current requirement, worst-case resistance of L758X switch of 28  $\Omega$ , and 50  $\Omega$  protection resistor with worst-case 10% tolerance of 55  $\Omega$ .

$$R_L = \frac{48 \text{ V} - 7.8 \text{ V}}{0.018 \text{ A}} - (2 \times (55 + 28)) - 130$$

$$R_L = 1937 \text{ } \Omega > 1800 \text{ } \Omega$$

#### Example 2, Extended Loop:

With a -65 V battery voltage, assuming a SLIC nominal overhead of 7.1 V, SLIC dc feed resistance of 110  $\Omega$ , 18 mA loop current requirement, worst-case resistance of L758X switch of 28  $\Omega$ , and 50  $\Omega$  protection resistor with worst-case 10% tolerance of 55  $\Omega$ , what is the maximum loop length?

$$2941 \text{ } \Omega = \frac{65 \text{ V} - 7.1 \text{ V}}{0.018 \text{ A}} - (2 \times (55 + 28)) - 110$$

## dc Applications

### On-Hook Transmission

In order to drive an on-hook ac signal, the SLIC must set up the tip and ring voltage to a value less than the battery voltage. The amount that the open loop voltage is decreased relative to the battery is referred to as the overhead voltage. Expressed as an equation,

$$V_{OH} = |V_{BAT}| - (V_{PT} - V_{PR})$$

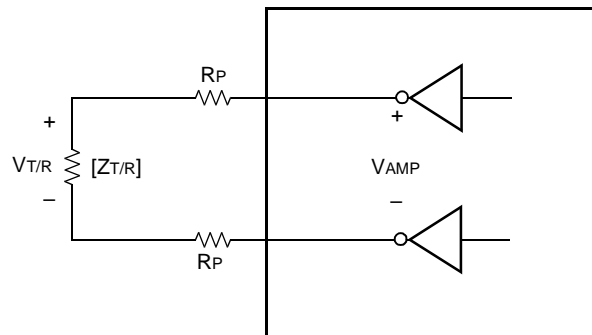
Without this buffer voltage, amplifier saturation will occur and the signal will be clipped. The L8567 is automatically set at the factory to allow undistorted on-hook transmission of a 3.17 dBm signal into a 900  $\Omega$  ac loop impedance.

The drive amplifiers are capable of 4 Vrms minimum ( $V_{AMP}$ ). So, the maximum signal the device can guarantee is:

$$V_{T/R} = 4 \text{ V} \left( \frac{|Z_{T/R}|}{|Z_{T/R}| + 2R_P} \right)$$

The peak voltage at output of tip and ring amplifiers is related to the peak signal voltage by:

$$\hat{V}_{amp} = \hat{V}_{T/R} \left( 1 + \frac{2R_P}{|Z_{T/R}|} \right)$$



12-2563 (F)

**Figure 27. SLIC 2-Wire Output Stage**

## dc Applications (continued)

### On-Hook Transmission (continued)

In addition to the required peak signal level, the SLIC needs about 2 V from each power supply to bias the amplifier circuitry. It can be thought of as an internal saturation voltage. Combining the saturation voltage and the peak signal level, the required overhead can be expressed as:

$$V_{OH} = V_{SAT} + \left(1 + \frac{2R_P}{|Z_{T/R}|}\right)^{\frac{1}{2}} V_{T/R}$$

where  $V_{SAT}$  is the combined internal saturation voltage between the tip/ring amplifiers and  $V_{BAT}$  (4.0 V typical).  $R_P$  ( $\Omega$ ) is the protection resistor value.  $Z_{T/R}$  ( $\Omega$ ) is the ac loop impedance.

#### Example:

Determine the required overhead to transmit on-hook ( $I_{LOOP} = 0$ ) a 3.17 dBm ac signal into a 900  $\Omega$  ac load. Assume use of 50  $\Omega$  protection resistors with a 10% tolerance or 55  $\Omega$  and an L7583 solid-state switch. The worst-case resistance of the switch is 28  $\Omega$ . Note the minimum overhead voltage of the L8567 is 6.4 V.

$$V_{ON} = 4.0 + \left(1 + \frac{2 \times [55 + 28]}{900}\right)^{\frac{1}{2}} \sqrt{2} (V_{rms})$$

$$3.17 \text{ dBm} = 20 \log \frac{\left(\frac{[V_{rms}]^2}{900}\right)}{10^{-3}}$$

$$V_{rms} = 1.296 \text{ V}$$

$$V_{ON} = 4.0 + \left(1 + \frac{2 \times [55 + 28]}{900}\right)^{\frac{1}{2}} \sqrt{2} (V_{rms})$$

$$V_{rms} = 1.296 \text{ V}$$

$$V_{ON} = 4.0 + \left(1 + \frac{2[55 + 28]}{900}\right)^{\frac{1}{2}} (\sqrt{2})(1.296)$$

$$V_{OH} = 6.17 \text{ V} < 6.4 \text{ V}$$

Thus, an overhead of 6.17 V is needed for on-hook transmission of a 3.17 dBm signal into a 900  $\Omega$  ac load. The L8567 has a minimum overhead of 6.4 V.

## Supervision

Both the loop closure and ring trip supervision functions are included on the L8567 SLIC. The outputs of these two supervision functions are internally wired-ORed together to form a single output NSTAT. The wired-OR connection of the loop supervision and ring trip detector is also available on pin NLED. This pin has sufficient drive capability to drive an LED. This pin is an open-collector output, so multiple pins can be used to drive a common LED. Also included is a SLIC thermal shutdown indicator, NTSD.

Note that the ring trip detector is not active in the low-power scan state. The ring trip detector must be active prior to applying power ringing to the subscriber loop. Activate the ring trip detector by putting the L8567 SLIC into the powerup mode before applying power ringing to the subscriber loop.

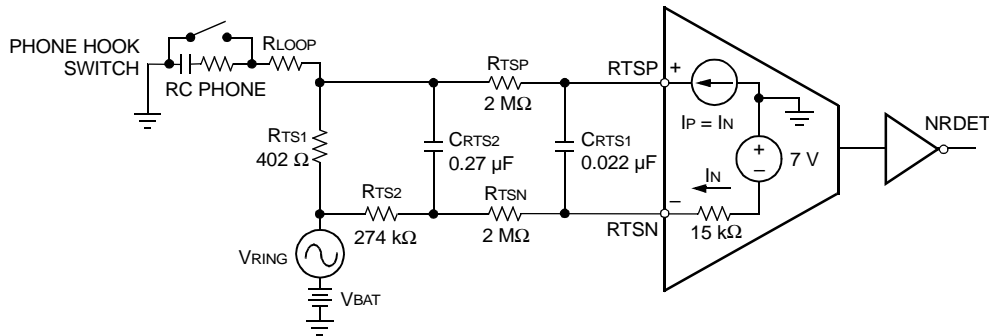
## Loop Closure

The on-hook to off-hook loop closure threshold is internally set to a nominal 11 mA at  $V_{BAT} = -48 \text{ V}$ . There is a nominal 2 mA hysteresis. This means that the off-hook to on-hook threshold will be a nominal 2 mA less than the on-hook to off-hook threshold. The loop closure threshold will track with battery voltage, increasing as the battery gets more negative. The loop closure comparator has built-in longitudinal rejection, eliminating the need for an external 50 Hz/60 Hz filter. The loop closure detector is valid during scan, forward, and reverse active states.

## dc Applications (continued)

### Ring Trip Detection

The ring trip circuit is a comparator that has a special input section optimized for this application. The equivalent circuit is shown in Figure 28, along with its use in an application using unbalanced, battery-backed ringing.



12-3014 (F)

**Figure 28. Ring Trip Equivalent Circuit and Equivalent Application**

The comparator input voltage compliance is  $V_{CC}$  to  $V_{BAT}$ , and the maximum current is 240  $\mu A$  in either direction. Its application is straightforward. A resistance ( $R_{TSN} + R_{TS2}$ ) in series with the  $R_{TSN}$  input establishes a current that is repeated in the  $R_{TSP}$  input. A slightly lower resistance ( $R_{TSP}$ ) is placed in series with the  $R_{TSP}$  input. When ringing is being injected, no dc current flows through  $R_{TS1}$ , and so the  $R_{TSP}$  input is at a lower potential than  $R_{TSN}$ . When enough dc loop current flows, the  $R_{TSP}$  input voltage increases to trip the comparator. In Figure 28, a low-pass filter with a double pole at 2 Hz was implemented to prevent false ring trip.

The following example illustrates how the detection circuit of Figure 28 will trip at 12.5 mA dc loop current using a -48 V battery.

$$I_N = \frac{-7 \text{ V} - (-48 \text{ V})}{2.289 \text{ M}\Omega} \\ = 17.9 \mu A$$

The current  $I_N$  is repeated as  $I_P$  in the positive comparator input. The voltage at comparator input  $R_{TSP}$  is:

$$V_{RTSP} = V_{BAT} + I_{LOOP(dc)} \times R_{TS1} + I_P \times R_{TSP}$$

Using this equation and the values in the example, the voltage at input  $R_{TSP}$  is -12 V during ringing injection ( $I_{LOOP(dc)} = 0$ ). Input  $R_{TSP}$  is, therefore, at a level of 5 V below  $R_{TSN}$ . When enough dc loop current flows through  $R_{TS1}$  to raise its dc drop to 5 V, the comparator will trip. In this example,

$$I_{LOOP(dc)} = \frac{5 \text{ V}}{402 \Omega} \\ = 12.5 \text{ mA}$$

### Other Supervision Functions

The L8567 has on-chip thermal shutdown circuitry. If the silicon die temperature exceeds a nominal 165 °C temperature, the SLIC will sense this temperature and enter the thermal shutdown mode, regardless of the logic inputs. The thermal shutdown mode is functionally similar to the disconnect state. When the die temperature cools, the SLIC will return to the reshot-down state. A hysteresis is included in the thermal shutdown mechanism.

The L8567 also has a logic input pin, NEXTSD, whose status is transferred to the serial output data bus. This pin may be connected to an external monitoring device.

An example is the thermal shutdown output pin of the L7583. If the L7583 enters the thermal shutdown mode, this is reflected in the TSD output pin of this device. The L8567 SLIC can accept this status pin and transfer the information on this pin to the serial output data bus.

## dc Applications (continued)

### Latched Parallel Data Interface

The L8567 uses a latched parallel data control scheme for both logic inputs and logic outputs. There is a latch enable (EN) pin associated with this control scheme. This data control scheme is designed to work in conjunction with the quad T7507 codec. The T7507 codec uses a serial data interface to receive and pass control information to and from the controlling processor. The T7507 controls the state of the L8567 SLIC via data inputs and outputs corresponding to those of the L8567 SLIC. The T7507 also provides the EN control signal.

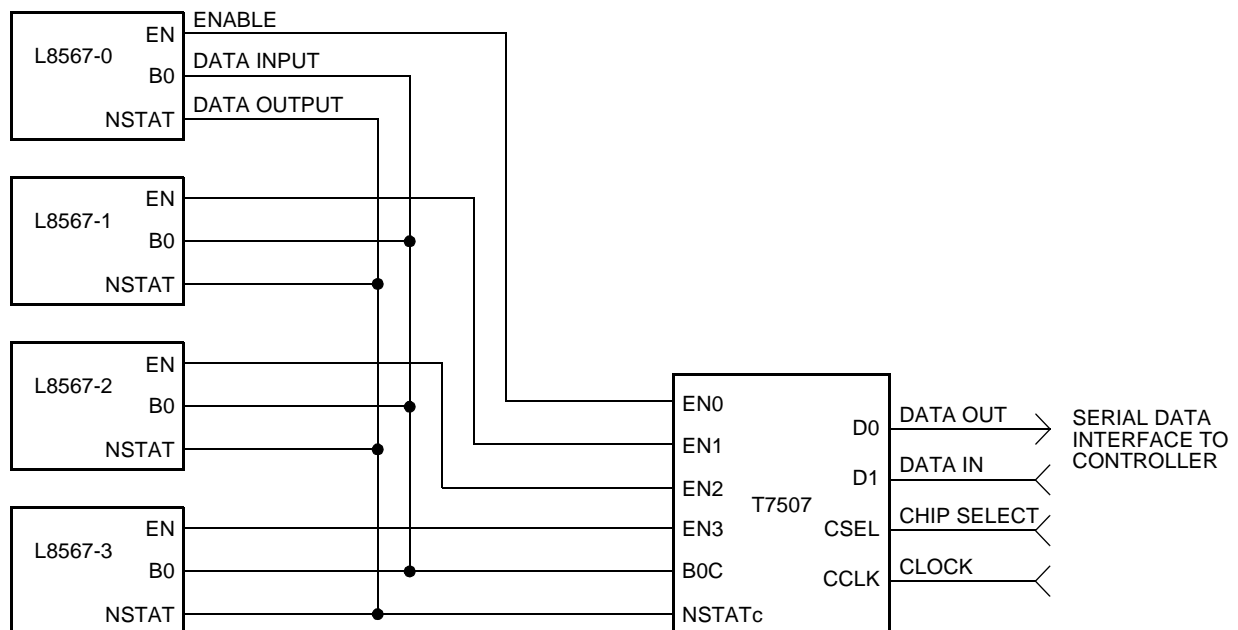
The T7507 is a quad codec; that is, four channels in a single package. Each quad codec is designed to control the four corresponding L8567 SLIC devices. Control inputs and outputs for the four channels are shared among the four SLICs. For example, there is only one B0 data output from the codec, and this control signal is passed to the B0 control input on the four associated SLICs. There are four EN outputs from the codec, one to each SLIC. Data on the shared input or output leads are valid to or from a given SLIC, depending on the state of EN pin associated with the individual SLIC. This is shown in Figure 29 below.

The control data inputs to the SLIC are B0 and B1, which set the state of the SLIC and RD1I, RD2I, and RD3I, which control the state of the EMR drivers. If an

L7583 solid-state switch is used instead of EMRs, the logic control outputs from the codec will go directly to the state control inputs of the switch. In this mode of operation, the relay drivers on the L8567 SLIC are not used. If this is the case, tie the logic inputs RD1I, RD2I, and RD3I to ground. This will force the drivers into the not-active state, which is the state with the lowest power consumption.

For the SLIC logic inputs, the latch is controlled by input EN. When EN is high, the input data latches are active; that is, data at the B0, B1, RD1I, RD2I, and RD3I inputs are latched. The latched data will control the state of the SLIC and drivers, and the SLIC and drivers will not respond to changes at the logic inputs while the level at EN is high. When EN is low, the input data latch is not active; that is, data at the logic inputs will flow through the latch and immediately determine the state of the SLIC and drivers.

Logic outputs NSTAT and NTSD are also latched. There is an internal pull-up associated with each of these logic outputs. The operation of EN with the logic outputs is slightly different from the operation of EN with the logic inputs. In order for valid data to be at the NSTAT and NTSD outputs, both the internal detector (i.e., an off-hook or thermal shutdown condition, respectively, exists) and pin EN must be low. Table 24 explains this.



12-3457(F)

Figure 29. Simplified Control Scheme

dc Applications (continued)

Latched Parallel Data Interface (continued)

Table 24. Valid Data at NSTAT and NTSD

EN	State	NSTAT
0	Off-hook—loop closure or ring trip	0
0	On-hook	1
1	Don't care	1
EN	State	NTSD
0	Device in thermal shutdown	0
0	Normal operation—device state determined by B0, B1, and RD1 inputs	1
1	Don't care	1

A simplified logic output latches schematic is shown in Figure 30.

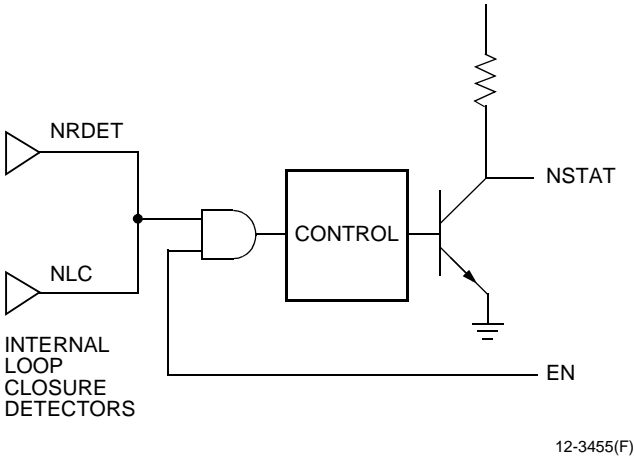


Figure 30. Logic Output Latches

Like NSTAT, output NLED also reflects loop closure and ring trip status. Output NLED is not latched. This output is an open-collector output with sufficient drive capability to drive an LED. Multiple NLED can be connected to a common LED. NLED is valid regardless of the state of EN. NLED can be used as an unlatched alternative to NSTAT for control logic.

ac Design

There are four key ac design parameters. **Termination impedance** is the impedance looking into the 2-wire port of the line card. It is set to match the impedance of the telephone loop in order to minimize echo return to the telephone set. **Transmit gain** is measured from the 2-wire port to the PCM highway, while **receive gain** is done from the PCM highway to the transmit port.

Finally, the **hybrid balance** network cancels the unwanted amount of the receive signal that appears at the transmit port.

First-Generation Codecs

These perform the basic filtering, A/D (transmit), D/A (receive), and  $\mu$ -law/A-law companding. They all have an op amp in front of the A/D converter for transmit gain setting and hybrid balance (cancellation at the summing node). Depending on the type, some have differential analog input stages, differential analog output stages, and  $\mu$ -law/A-law selectability. This generation of codecs is lower cost compared to second- and third-generation codecs, but needs the most complicated interface between the SLIC and codec. These codecs are most suitable for applications with fixed gains, termination impedance, and hybrid balance.

Second-Generation Codecs

This class of devices includes a microprocessor interface for software control of the gains and hybrid balance. The hybrid balance is included in the device. ac programmability adds application flexibility and saves several passive components and also adds several I/O latches that are needed in the application. However, there is no transmit op amp, since the transmit gain and hybrid balance are set internally.

Third-Generation Codecs

This class of devices includes the gains, termination impedance, and hybrid balance—all under microprocessor control. Depending on the device, it may or may not include latches. This generation of codec offers a very simple SLIC-codec interface with a minimal number of external components.

T7507 Codec

The T7507 provides third-generation codec functionality without the programmability. In the T7507, ac gain, termination impedance, and the hybrid balance network are set digitally; thus, the SLIC-codec interface requires virtually no external components.

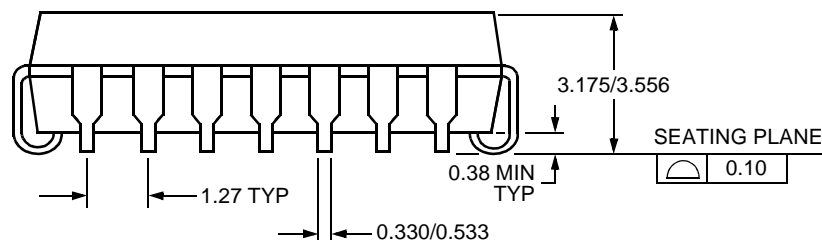
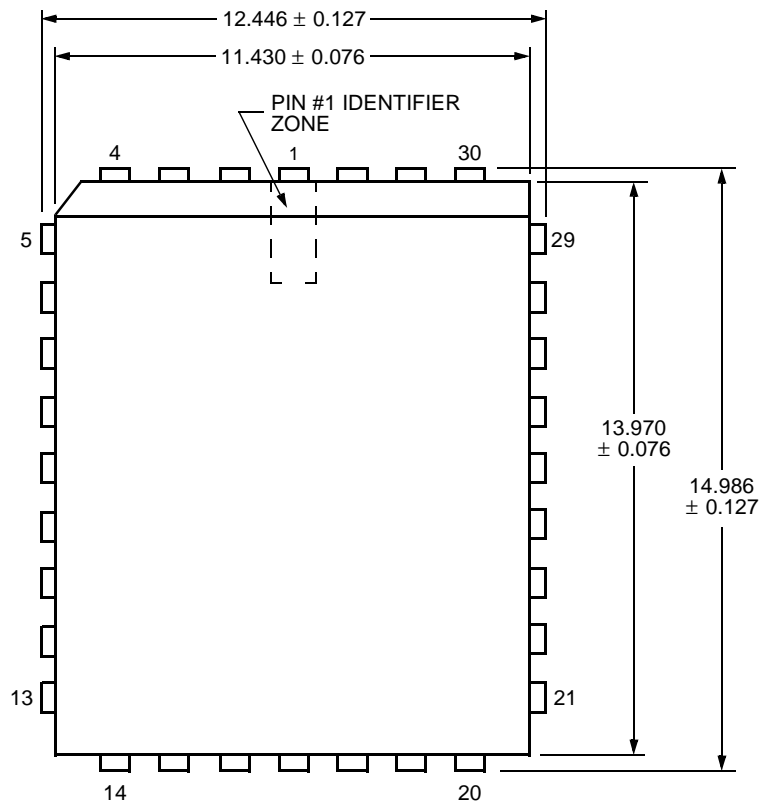
However, because all the ac parameters are fixed (and set for requirements in the PRC), the device is an extremely cost-effective solution.

## Outline Diagrams

### 32-Pin PLCC

Dimensions shown are metric.

**Note:** The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Sales Representative.



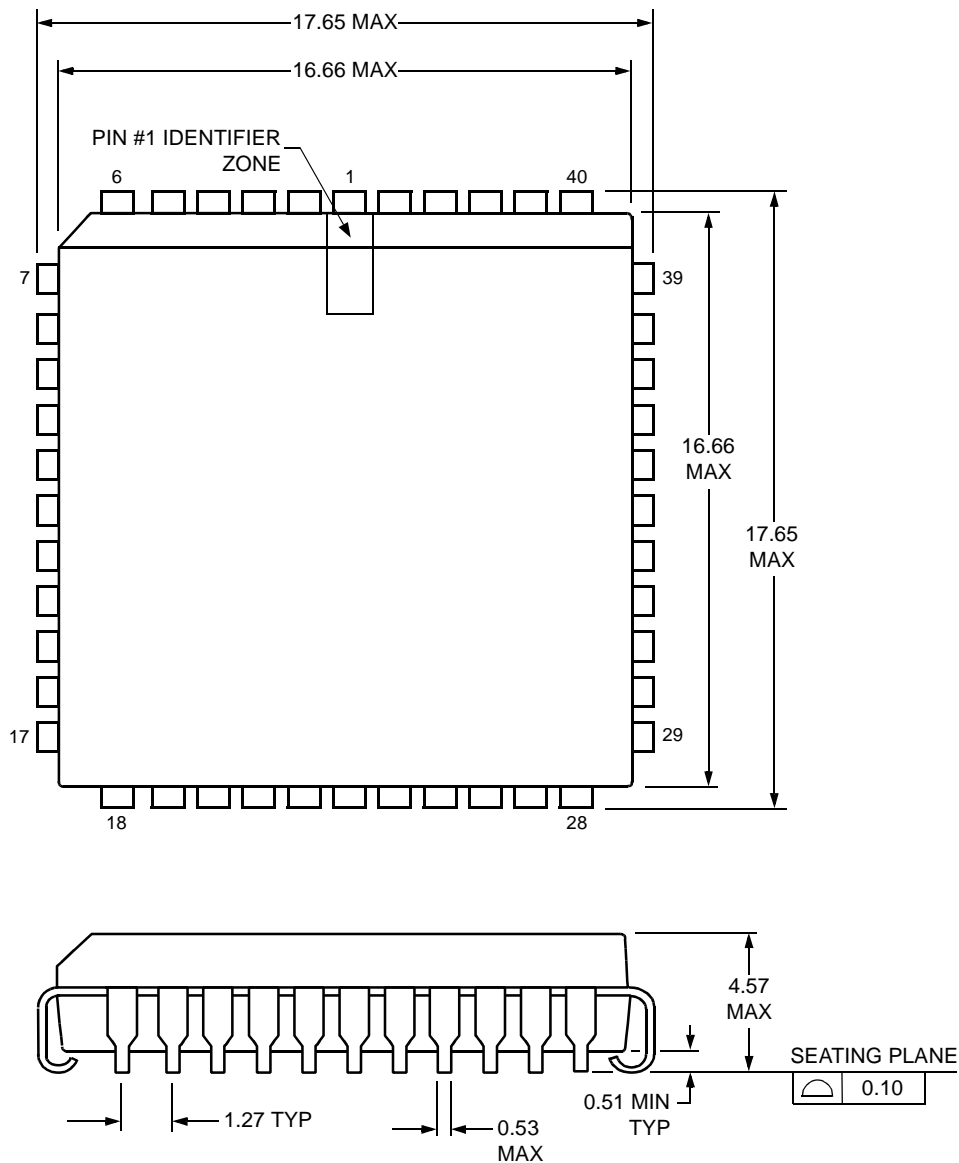
5-3813 (F)r01

## Outline Diagrams (continued)

### 44-Pin PLCC

Dimensions shown are metric.

**Note:** The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Sales Representative.



5-2506 (F) r07



## Ordering Information

Device Part No.	Description	Package	Comcode
LUCL8567AAU-D	PRC SLIC	32-Pin PLCC (Dry-bagged, Tube)	107891236
LUCL8567AAU-DT	PRC SLIC	32-Pin PLCC (Dry-bagged, Tape and Reel)	107891244
LUCL8567AP-D	PRC SLIC	44-Pin PLCC (Dry-bagged, Tube)	107957706
LUCL8567AP-DT	PRC SLIC	44-Pin PLCC (Dry-bagged, Tape and Reel)	107957714

---

For additional information, contact your Agere Systems Account Manager or the following:

INTERNET: **<http://www.agere.com>**

E-MAIL: **[docmaster@agere.com](mailto:docmaster@agere.com)**

N. AMERICA: Agere Systems Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18109-3286

**1-800-372-2447**, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)

ASIA: Agere Systems Hong Kong Ltd., Suites 3201 & 3210-12, 32/F, Tower 2, The Gateway, Harbour City, Kowloon

**Tel. (852) 3129-2000**, FAX (852) 3129-2020

CHINA: **(86) 21-5047-1212** (Shanghai), **(86) 10-6522-5566** (Beijing), **(86) 755-695-7224** (Shenzhen)

JAPAN: **(81) 3-5421-1600** (Tokyo), KOREA: **(82) 2-767-1850** (Seoul), SINGAPORE: **(65) 6778-8833**, TAIWAN: **(886) 2-2725-5858** (Taipei)

EUROPE: **Tel. (44) 7000 624624**, FAX (44) 1344 488 045

---

Agere Systems Inc. reserves the right to make changes to the product(s) or information contained herein without notice. No liability is assumed as a result of their use or application.