Data Sheet, Rev. 6
March 2006

USS810 USB 2.0 Full-Speed/Low-Speed Transceiver

1 Features

- Complies with *Universal Serial Bus Specification* Rev. 2.0.
- Can be used as a USB device transceiver or a USB host transceiver.
- Supports full-speed (12 Mbits/s) and low-speed (1.5 Mbits/s) serial data rates.
- Includes two single-ended receivers with hysteresis.
- Low-power operation helps maximize battery life of portable electronic devices.
- Available in a small MLCC16 package measuring 3 mm x 3 mm. (A lead-free package is also available. See Ordering Information on page 14.)
- Supports a digital I/O voltage range from 1.75 V to 3.3 V.
- Supports the full industrial operating temperature range, –40 °C to +85 °C.

2 Description

Agere's USS810 is a Universal Serial Bus (USB) transceiver that is fully compliant with the *Universal Serial Bus Specification* Rev. 2.0. The USS810 can transmit and receive serial data at full-speed (12 Mbits/s) and low-speed (1.5 Mbits/s) data rates and, therefore, can be used as either a USB device transceiver or a USB host transceiver.

Since the USS810 operates at digital I/O voltages between 1.75 V to 3.3 V, it is particularly suitable for portable electronic devices such as mobile phones, digital still cameras, personal digital assistants (PDAs), and a variety of information appliances. This transceiver provides an ideal interface to the physical layer of the universal serial bus for application-specific ICs (ASICs) and programmable logic devices (PLDs) with power supply voltages in the above range.

The USB transceiver is currently available in an MLCC16 package that supports single-ended input data interface.

3 Suitable Applications

Portable electronic devices, such as the following:

- Mobile phone
- Digital still camera
- Personal digital assistant (PDA)
- Information appliances

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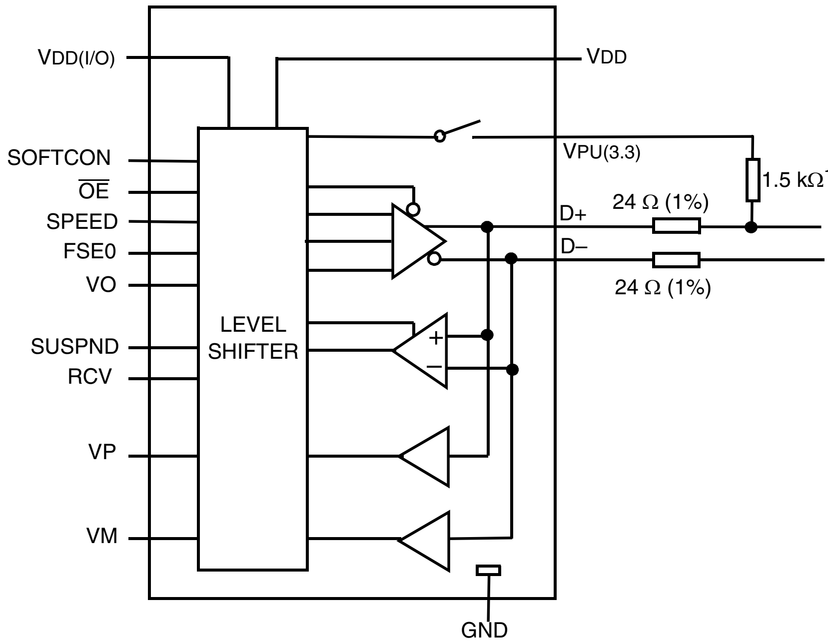

1. Connect pull-up to D– for low-speed operation.

Figure 1. USS810 Functional Diagram

5 Pin Information

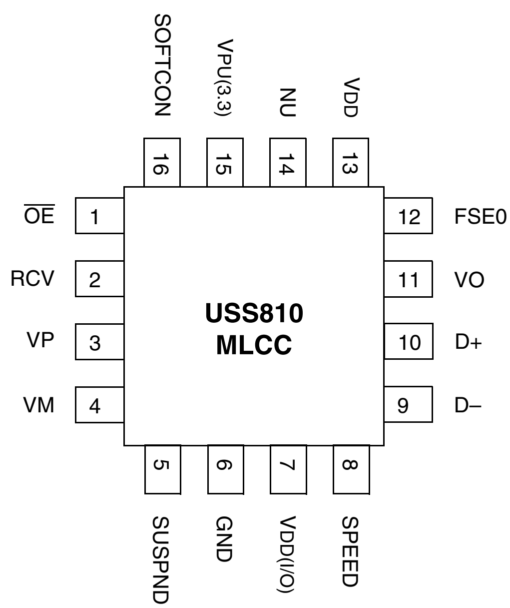

Figure 2. USS810 MLCC Pin Diagram (Top View)

5 Pin Information (continued)

5.1 Pin Descriptions

Table 1. USS810 Pin Description

Symbol	MLCC Pin	Type	Description
$V_{PU(3.3)}$	15	—	**Pull-Up Voltage Source.** Connect this pin through an external 1.5 kΩ resistor to D+ (for full-speed operation) or D– (for low-speed operation). This pin's function is controlled by the SOFTCON input pin. To ensure zero pull-up current, set SOFTCON = low to cause $V_{PU(3.3)}$ to float (high impedance); when SOFTCON = high, $V_{PU(3.3)}$ = 3.3 V.
SOFTCON	16	I	**Software-Controlled USB Connection.** This pin allows USB connect/disconnect signaling to be controlled by software. A high level on this pin applies 3.3 V to pin $V_{PU(3.3)}$, which is connected to an external 1.5 kΩ pull-up resistor.
$\overline{OE}$[1]	1	I	**Output Enable.** This active-low pin enables the transceiver to transmit data on the USB bus.
RCV	2	O	**Differential Data Receiver.** When the SUSPND input is high, this pin is driven low. The state of RCV is unknown when FSE0 = 1.
VP	3	O	**Single-Ended D+ Receiver.** The VP pin is used for external detection of single-ended zero (SE0), error conditions, and speed of connected device.
VM	4	O	**Single-Ended D– Receiver.** The VM pin is used for external detection of single-ended zero (SE0), error conditions, and speed of connected device.
SUSPND	5	I	**Suspend.** When SUSPND is high, it enables a low-power state while the USB is inactive and drives output RCV to a low level. No dc power is consumed when SUSPND is high.
GND	6	P	**Device Ground.**
$V_{DD(I/O)}$	7	P	**Power Supply for Digital I/O.** 1.75 V to 3.3 V.
SPEED	8	I	**Speed Selection.** This pin adjusts the slew rate of differential data outputs D+ and D–. Tie this pin low to enable low-speed data transmission (1.5 Mbits/s) and high to enable full-speed data transmission (12 Mbits/s).
D–	9	Analog I/O	**Negative USB Differential Data Bus.** If this device is used in a USB peripheral application, connect an external 24 Ω ± 1% resistor in series with this signal in order to meet the *USB Specification*, Rev. 2.0 impedance requirement. Connect this signal to pin $V_{PU(3.3)}$ via a 1.5 kΩ ± 5% resistor for low-speed USB peripheral applications.
D+	10	Analog I/O	**Positive USB Differential Data Bus.** If this device is used in a USB peripheral application, connect an external 24 Ω ± 1% resistor in series with this signal in order to meet the *USB Specification* Rev. 2.0 impedance requirement. Connect this signal to pin $V_{PU(3.3)}$ via a 1.5 kΩ ± 5% resistor for full-speed USB peripheral applications.
VO	11	I	**Single-Ended Data Input.** Refer to Table 3..
FSE0	12	I	**Single-Ended Zero Mode.** Refer to Table 3..
V_{DD}	13	P	**3.3 V Power Supply.** This voltage supply is used for the USB signals D+/D– and the internal level shifter.
NU	14	—	**Not Usable.** No external connections to this pin are allowed.

1. Symbol names with an overscore (e.g., $\overline{NAME}$) indicate active-low signals.

6 Functional Description

6.1 Function Selection

Table 2. Function Table

SUSPND	$\overline{OE}$	(D+, D–)	RCV	VP/VM	Function
L	L	Transmitting and Receiving	Active	Active	Normal transmit (differential receiver active)
L	H	Receiving[1]	Active	Active	Receiving
H	L	High-Z[3]	L[2]	Active	Transmitting during suspend (differential receiver inactive)
H	H	High-Z[3]	L[2]	Active	Low-power state

1. Signal levels on (D+, D–) are determined by other USB devices and external pull-up/down resistors.
2. In suspend mode (SUSPND = high), the differential receiver is inactive and output RCV is always low. Out-of-suspend (K) signaling is detected via the single-ended receivers VP and VM.
3. In suspend mode, the D+/D– output is tristated.

6.1 Operating Functions

Table 3. Transmit Function Using Single-Ended Input Data Interface ($\overline{OE}$ = L)

FSE0	VO	Data
L	L	Differential logic 0
L	H	Differential logic 1
H	L	SE0
H	H	SE0

Table 4. Receive Function ($\overline{OE}$ = H)

(D+, D–)	RCV	VP	VM
Differential Logic 0	L	L	H
Differential Logic 1	H	H	L
SE0	Unknown[1]	L	L

1. The state of RCV is unknown when FSE0 = 1.

7 Limiting Values

7.1 Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(I/O)}$	I/O Supply Voltage	—	1.7	3.3	V
$V_{DD(3.3)}$	3.3 V Supply Voltage	—	3.0	3.6	V
V_I	dc Input Voltage	—	–0.5	V_{DD} + 0.5	V
T_{stg}	Storage Temperature	—	–40	125	°C

Table 6. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
$V_{DD(I/O)}$	I/O Supply Voltage	—	1.75	—	3.3	V
$V_{DD(3.3)}$	3.3 V Supply Voltage	3.3 V operation	3.135	3.3	3.465	V
V_I	Input Voltage	—	0	—	3.3	V
$V_{I(AI/O)}$	Input Voltage on Analog I/O Pins (D+/D–)	—	0	—	$V_{DD(I/O)}$	V
T_{amb}	Operating Ambient Temperature	—	–40	—	85	°C

8 Static Characteristics

Table 7. Static Characteristics: Supply Pins

V_{DD} = 3.3 V; $V_{DD(I/O)}$ = 1.75 V to 3.3 V; V_{GND} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
I_{DD}	Operating Supply Current	Full-speed transmit and receive	—	5	8	mA
$I_{DD(I/O)}$	Operating I/O Supply Current	Full-speed transmit and receive at 12 Mbits/s	—	—	100	µA
$I_{DD(susp)}$	Suspend Supply Current	SUSPND = high	—	—	10	µA

8 Static Characteristics (continued)

Table 8. Static Characteristics: Digital Pins

$V_{DD(I/O)}$ = 1.75 V to 3.3 V; V_{GND} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
$V_{DD(I/O)}$ = 1.75 V to 3.3 V						
Input Levels:						
V_{IL}	Low-level Input Voltage	—	—	—	0.7	V
V_{IH}	High-level Input Voltage	—	1.7	—	—	V
Output Levels:						
V_{OL}	Low-level Output Voltage	$I_{OL} \le 6$ mA	—	—	0.4	V
V_{OH}	High-level Output Voltage	$I_{OH} \le 6$ mA	V_{DD} – 0.4	—	—	V

Table 9. Static Characteristics: Analog I/O Pins (D+, D–)

V_{DD} = 3.3 V; V_{GND} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
Input Levels						
Differential Receiver						
V_{DI}	Differential Input Sensitivity	$\lvert V_{I(D+)} - V_{I(D-)} \rvert$	0.2	—	—	V
V_{CM}	Differential Common-mode Voltage	Includes V_{DI} range	0	—	V_{DD}	V
Single-Ended Receiver						
V_{hys}	Hysteresis Voltage	—	0.3	—	—	V
Output Levels						
V_{OL}	Low-level Output Voltage	R_L = 1.5 kΩ to 3.6 V	—	—	0.3	V
V_{OH}	High-level Output Voltage	R_L = 15 kΩ to GND	2.8	—	3.6	V
Leakage Current						
I_{LZ}	High-impedance Leakage Current	$\overline{OE}$ = 1	–10	—	10	µA
Capacitance						
C_{IN}	Transceiver Capacitance	Pin to GND	—	—	3	pF

9 Dynamic Characteristics

Table 10. Dynamic Characteristics: Analog I/O Pins (D+, D–)[1]

V_{DD} = 3.3 V; $V_{DD(I/O)}$ = 1.75 V to 3.3 V; V_{GND} = 0 V; Tamb = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
Driver Characteristics						
Full-Speed Mode (Speed = 1)						
t_R	Rise Time	$\overline{OE}$ = 0, CL = 50 pF; 10% to 90% of $\lvert V_{OL} – V_{OH}\rvert$; see Figure 3..	4	—	20	ns
t_F	Fall Time	$\overline{OE}$ = 0, CL = 50 pF; 90% to 10% of $\lvert V_{OH} – V_{OL}\rvert$; see Figure 3.	4	—	20	ns
DRFM	Differential Rise/Fall Time Matching	$\overline{OE}$ = 0, CL = 50 pF.	90	100	110	%
V_{CRS}	Output Signal Crossover Voltage	$\overline{OE}$ = 0, CL = 50 pF: see Figures 4, 5, 6.	1.3	—	2.0	V
Low-Speed Mode (Speed = 0)						
t_R	Rise Time	$\overline{OE}$ = 0, CL = 50 pF or 350 pF; 10% to 90% of $\lvert V_{OL} – V_{OH}\rvert$; see Figure 3.	75	—	300	ns
t_F	Fall Time	$\overline{OE}$ = 0, CL = 50 pF or 350 pF; 90% to 10% of $\lvert V_{OH} – V_{OL}\rvert$; see Figure 3.	75	—	300	ns
DRFM	Differential Rise/Fall Time Matching	CL = 50 pF or 350 pF.	80	100	120	%
V_{CRS}	Output Signal Crossover Voltage	CL = 50 pF or 350 pF; see Figures 4, 5, 6.	1.3	—	2.0	V
Driver Timing						
Full-Speed Mode (Speed = 1)						
t_{PLH}	Driver Propagation Delay: Low-to-High (VO, FSE0 to D+, D–)	$\overline{OE}$ = 0, CL = 50 pF; see Figure 6.	—	—	18	ns
t_{PHL}	Driver Propagation Delay: High-to-Low (VO, FSE0 to D+, D–)	$\overline{OE}$ = 0, CL = 50 pF; see Figure 6.	—	—	18	ns
t_{PHZ}	Tristate Output Disable: High-to-Off ($\overline{OE}$ to D+, D–)	$\overline{OE}$ switching; see Figure 4.	—	—	2.5	ns
t_{PLZ}	Tristate Output Disable: Low-to-Off ($\overline{OE}$ to D+, D–)	$\overline{OE}$ switching; see Figure 4.	—	—	2.5	ns
t_{PZH}	Tristate Output Enable: Off-to-High ($\overline{OE}$ to D+, D–)	$\overline{OE}$ switching; see Figure 4.	—	—	20	ns
t_{PZL}	Tristate Output Enable: Off-to-Low ($\overline{OE}$ to D+, D–)	$\overline{OE}$ switching; see Figure 4.	—	—	20	ns

1. Test circuit: see Figure 7.

9 Dynamic Characteristics (continued)

Table 10. Dynamic Characteristics: Analog I/O Pins (D+, D–)[1] (continued)

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
Driver Timing (continued)						
Low-Speed Mode (SPEED = 0)						
t_{PLH}	Driver Propagation Delay: Low-to-High (VO, FSE0 to D+, D–)	$\overline{OE}$ = 0, CL = 50 pF; see Figure 6.	—	—	250	ns
t_{PHL}	Driver Propagation Delay: High-to-Low (VO, FSE0 to D+, D–)	$\overline{OE}$ = 0, CL = 50 pF; see Figure 6.	—	—	250	ns
t_{PHZ}	Tristate Output Disable: High-to-Off ($\overline{OE}$ to D+, D–)	$\overline{OE}$ switching; see Figure 4.	—	—	4	ns
t_{PLZ}	Tristate Output Disable: Low-to-Off ($\overline{OE}$ to D+, D–)	$\overline{OE}$ switching; see Figure 4.	—	—	4	ns
t_{PZH}	Tristate Output Enable: Off-to-High ($\overline{OE}$ to D+, D–)	$\overline{OE}$ switching; see Figure 4.	—	—	400	ns
t_{PZL}	Tristate Output Enable: Off-to-Low ($\overline{OE}$ to D+, D–)	$\overline{OE}$ switching; see Figure 4..	—	—	400	ns
Receiver Timing (Full-Speed and Low-Speed Mode)						
Differential Receiver						
$t_{PLH(dif)}$	Propagation Delay; Low-to-High (D+, D– to RCV)	See Figure 5..	—	—	5	ns
$t_{PHL(dif)}$	Propagation Delay; High-to-Low (D+, D– to RCV)	See Figure 5..	—	—	5	ns
Single-Ended Receiver						
$t_{PLH(se)}$	Propagation Delay; Low-to-High (D+, D– to VP, VM)	See Figure 5..	—	—	3	ns
$t_{PHL(se)}$	Propagation Delay; High-to-Low (D+, D– to VP, VM)	See Figure 5..	—	—	3	ns

1. Test circuit: see Figure 7

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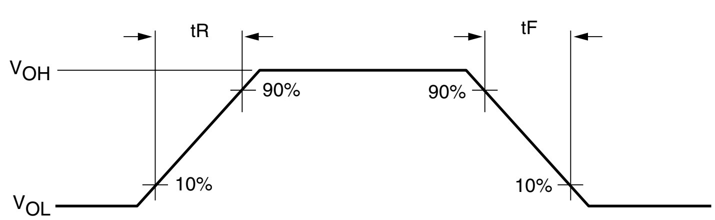


Figure 3. Rise and Fall Times

9 Dynamic Characteristics (continued)

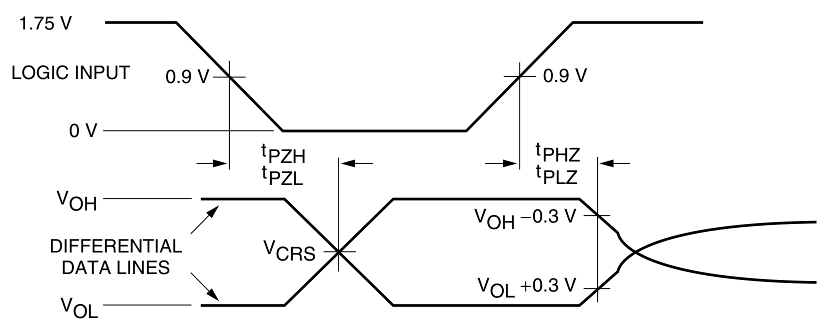


Figure 4. Timing of $\overline{OE}$ to D+, D–

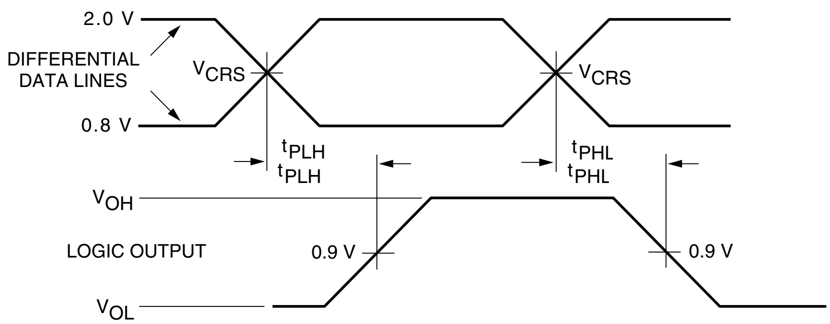


Figure 5. Timing of D+, D– to RCV, VP, VM

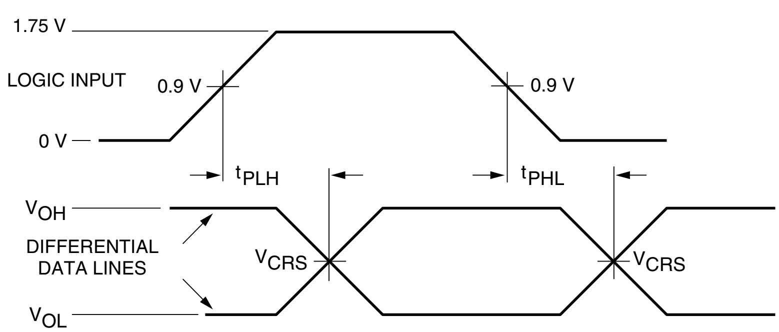
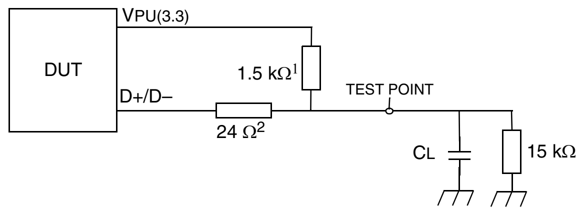


Figure 6. Timing of VO, FSE0 to D+, D–

10 Test Information



Load Capacitance:
  CL = 50 pF (full-speed mode).
  CL = 50 pF or 350 pF (low-speed mode).

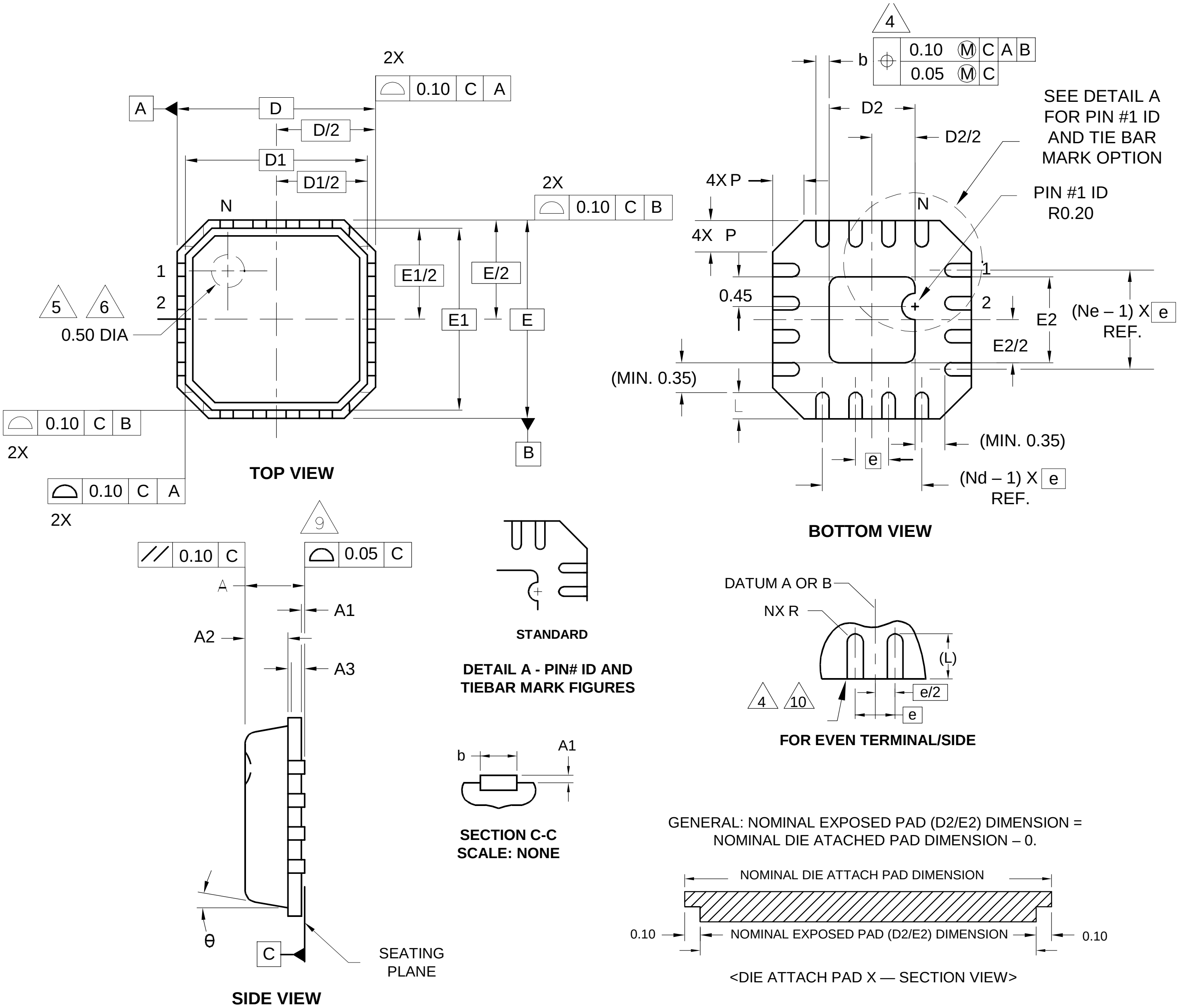
1. Full-speed mode: connected to D+, low-speed mode: connected to D–.
2. Complies with USB2.0.

Figure 7. Load for D+, D–

11 Package Outline Diagram

11.1 16-Pin MLCC, 3 mm x 3 mm

Dimensions are in millimeters.



Notes (Refer also to Tables 11 and 12):
1. Die thickness allowable is 0.305 mm maximum (0.012 inches maximum).
2. Dimensioning and tolerances conform to ASME Y14.5M-1994.
3. N is the number of terminals. Nd is the number of terminals in X direction, and Ne is the number of terminals in the Y direction.
4. Dimension b applies to plated terminal and is measured between 0.2 mm and 0.25 mm from terminal tip.
5. The pin #1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
6. Exact shape and size of this feature is optional.
7. All dimensions are in millimeters.
8. The shape shown on four corners is not actual I/O.
9. Bilateral coplanarity zone applies to the exposed pad as well as the terminals.
10. Applied only for terminals.
11. Q and R apply only for straight tie bar shapes.

11 Package Outline Diagram (continued)

Table 11. Pitch Variation

Symbol	Pitch Variation			Notes
	Min	Nom	Max	
e	0.5 BSC			—
N	16			3
Nd	4			3
Ne	4			3
L	0.3	0.4	0.5	—
b	0.18	0.23	0.3	4
D2	1.40	1.50	1.60	—
E2	1.40	1.50	1.60	—

Table 12. Common Dimensions

Symbol	Common Dimensions			Notes
	Min	Nom	Max	
A	0.8	0.85	0.9	—
A1	0.0	0.01	0.05	11
A2	0.6	0.65	0.70	—
A3	0.20 REF			—
D	3.0 BSC			—
D1	2.75 BSC			—
E	3.0 BSC			—
E1	2.75 BSC			—
θ	0	—	12	—
P	0.24	0.42	0.6	—
R	0.13	0.17	0.23	12

12 USB Application Support Contact Information

E-mail: usb@agere.com

13 Ordering Information

Device Code	Description	Package	Comcode
USS810M-D	USS810 in dry-packed tube	MLCC16	700057479
USS810M-DT	USS810 in dry-packed tape and reel	MLCC16	700058082
L-USS810M-D*†	Lead-free USS810 in dry-packed tube	MLCC16	700067200
L-USS810M-D*†	Lead-free USS810 in dry-packed tape and reel	MLCC16	700067201

* Lead-free: No intentional addition of lead, and less than 1000 ppm.

† Agere Systems lead-free devices are fully compliant with the Restriction of Hazardous Substances (RoHS) directive that restricts the content of six hazardous substances in electronic equipment in the European Union. Beginning July 1, 2006, electronic equipment sold in the European Union must be manufactured in accordance with the standards set by the RoHS directive.

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