



TSOT0410G SONET/SDH STS-192 Overhead Processor and Path Terminator

Features

General

- Section, line, and path overhead layer termination for a SONET STS-192 (SDH STM-64) or four STS-48 (STM-16) signals.
- Supports any valid mix of STS-1 and concatenated payloads from STS-3c to STS-192c.
- Microprocessor interface configurable to operate with most commercial microprocessors.
- *IEEE** 1149.1 port with memory BIST, scan, and boundary scan (JTAG).
- Low-power 2.5 V operation with 3.3 V (5 V tolerant) inputs and outputs.
- 600-pin LBGA package.
- -40 °C to +85 °C temperature range.

STS-192/STM-64

- Provides a 16-bit (or 4 × 4-bit) wide 622 MHz differential line interface.
- Synchronizes to the receive data frames and detects severely errored framing (SEF) and loss of frame (LOF). It also inserts the framing bytes (A1, A2) in the transmit data.
- Supports enhanced framing (A1, $\overline{A1}$, A2, $\overline{A2}$).
- Performs frame synchronous scrambling and descrambling of the STS-192/STS-48 data, and loss of signal (LOS) is detected.
- Extracts the 64-byte or 16-byte section trace message (J0) from the receive data and optionally stores it in, or compares it to, an internal register bank. Unstable or mismatched messages are detected and path AIS may be optionally inserted in the drop data.

- Optionally inserts a 64-byte or 16-byte section trace message or a fixed pattern in the J0 byte of the transmit data.
- Extracts, and outputs on a serial link, all transport overhead bytes in the receive data and inserts any or all transport overhead bytes in the transmit data using a corresponding serial input.
- Extracts, and outputs on serial links, the section user channel (F1), orderwire channels (E1, E2), and data communication channels (D1—D3 and D4—D12) for the receive data. Inserts corresponding serial input signals into the transmit data.
- Extracts, integrates, and stores the automatic protection switch (APS) channel bytes (K1, K2) for the receive data and detects protection switch failure alarms. Inserts APS bytes in the transmit data from internal registers or from overhead bytes in the add data.
- Detects line alarm indication signal (AIS) and remote defect indication (RDI) based on the K2 byte of the receive data. Inserts line AIS and RDI in the transmit data. Optionally inserts line RDI automatically due to LOS, LOF, or line AIS defects.
- Extracts, integrates, and stores the synchronization status byte (S1) for the receive data. Inserts the synchronization status byte into the transmit data from an internal register or from a value encoded on the transmit frame sync input.
- Calculates, detects, and counts section and line BIP-8 errors (B1, B2) for the receive data, and inserts BIP-8 in the transmit data. Supports either bit or block error accumulation, separately provisionable.
- Extracts and counts line remote errors (REI) for the receive data (M1), and inserts REI in the transmit data based on B2 errors (provisionable based on bit or block errors).

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Features (continued)

Add/Drop

- Provides sixteen 1-bit serial 622 MHz (STS-12) differential data links at the add and drop interfaces. Path overhead and SPE timing indication is provided by the drop interface. Clock recovery and data skew compensation provided at the add interface.
- Interprets the pointer bytes (H1, H2) for each receive STS and detects loss of pointer (LOP) and path AIS. Generates new pointer bytes in each drop STS to adapt the receive data to the drop frequency and phase. Pointer generation can be bypassed for synchronous applications.
- Optionally inserts path AIS in all drop STS pointer bytes during LOS, LOF, SEF, or line AIS defects. Optionally inserts path AIS in each drop STS due to LOP or path AIS defects in the corresponding receive STS, or under software control.
- Inserts pointer bytes in the transmit data based on values received in the transport overhead bytes of the add data. Optionally inserts path AIS in each transmit STS under control by software, or through bits in the transport overhead of the add data.
- Extracts the 64-byte or 16-byte path trace message (J1) from up to four selectable receive STS channels (one per STS-48), and stores it in an internal register bank. Optionally compares the message to an expected message stored in the internal register bank and detects an unstable or mismatched message.
- Calculates, detects, and accumulates path BIP-8 errors (B3) for each receive STS (provisionable based on bit or block errors). Provides signal fail detection with provisionable BER.
- Extracts and counts path REI for each receive STS (G1).
- Detects path unequipped, payload label mismatch (PLM), and optionally, payload defect indication (PDI) in the C2 byte of each receive STS. Optionally inserts unequipped signal in each transmit STS under software control.
- Detects 1-bit and enhanced path RDI in each receive STS (G1).
- Outputs path alarm information for each receive STS in the overhead bytes of the drop data (E1/F1).

Applications

- SONET/SDH add-drop multiplex equipment
- SONET/SDH terminal equipment
- SONET/SDH digital cross connect equipment
- SONET/SDH test equipment
- ATM or packet over SONET/SDH equipment

Description

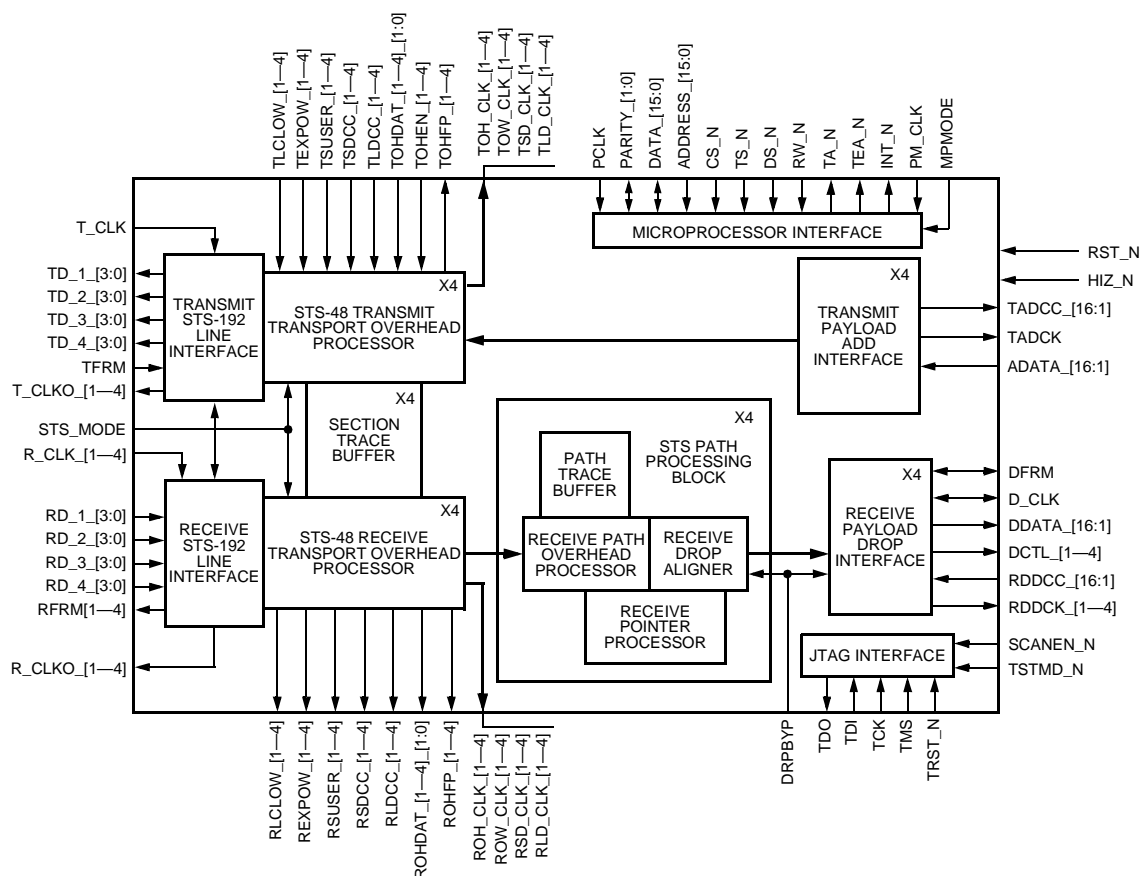
The TSOT0410G is used to terminate the transport overhead in a single SONET STS-192 (SDH STM-64) signal, or four SONET STS-48 (SDH STM-16) signals. It monitors the STS path pointers and overhead in the receive data, and provides timing signals for payload mapping devices on the equipment side. The TSOT0410G can be provisioned to support any mix of STS-1 (AU-3) or STS-Nc (AU-4-Xc) payloads from a single STS-192c (AU-4-64c) channel to 192 STS-1 (AU-3) channels. An overall block diagram is shown in Figure 1 on page 3.

The TSOT0410G is a 2.5 V, 0.25 μ m high-density device which is packaged in a 600-pin laminate ball grid array (LBGA). The I/O circuitry uses a 3.3 V 0.25 μ m technology (5 V tolerant).

The microprocessor interface allows an external processor to access the TSOT0410G for configuration and maintenance. The microprocessor interface is designed to support various 16-bit microprocessors with minimal glue logic.

The TSOT0410G includes an *IEEE* 1149.1 compliant JTAG port to support boundary scan and memory BIST testing of the device.

Block Diagram



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Figure 1. TSOT0410G Block Diagram

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