

# Hermetically Sealed, Low $I_F$ , Wide $V_{CC}$ , Logic Gate Optocouplers

## Technical Data

**HCPL-520x\***  
**5962-88768**  
**HCPL-523x**  
**HCPL-623x**  
**HCPL-625x**  
**5962-88769**

\*See matrix for available extensions.

### Features

- Dual Marked with Device Part Number and DSCC Standard Microcircuit Drawing
- Manufactured and Tested on a MIL-PRF-38534 Certified Line
- QML-38534, Class H and K
- Four Hermetically Sealed Package Configurations
- Performance Guaranteed over  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Wide  $V_{CC}$  Range (4.5 to 20 V)
- 350 ns Maximum Propagation Delay
- CMR:  $> 10,000 \text{ V}/\mu\text{s}$  Typical
- 1500 Vdc Withstand Test Voltage
- Three State Output Available
- High Radiation Immunity
- HCPL-2200/31 Function Compatibility
- Reliability Data Available
- Compatible with LSTTL, TTL, and CMOS Logic

### Applications

- Military and Space
- High Reliability Systems
- Transportation and Life Critical Systems
- High Speed Line Receiver

- Isolated Bus Driver (Single Channel)
- Pulse Transformer Replacement
- Ground Loop Elimination
- Harsh Industrial Environments
- Computer-Peripheral Interfaces

### Description

These units are single, dual and quad channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard product or with full MIL-PRF-38534 Class Level H or K testing or from the appropriate DSCC Drawing. All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DSCC Qualified Manufacturers List QML-38534 for Hybrid Microcircuits.

Each channel contains an AlGaAs light emitting diode which is optically coupled to an integrated high gain photon detector. The detector has a threshold with hysteresis which provides differential mode noise immunity and

eliminates the potential for output signal chatter. The detector in the single channel units has a tri-state output stage

### Truth Tables

(Positive Logic)

#### Multichannel Devices

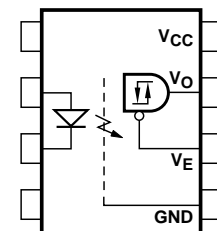
Input	Output
On (H)	H
Off (L)	L

#### Single Channel DIP

Input	Enable	Output
On (H)	H	Z
Off (L)	H	Z
On (H)	L	H
Off (L)	L	L

### Functional Diagram

Multiple Channel Devices Available



A 0.1  $\mu\text{F}$  bypass capacitor must be connected between  $V_{CC}$  and GND pins.

*CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

which allows for direct connection to data buses. The output is non-inverting. The detector IC has an internal shield that provides a guaranteed common mode transient immunity of up to 10,000 V/ $\mu$ s. Improved power supply rejection eliminates the need for special power supply bypass precautions.

Package styles for these parts are 8 pin DIP through hole (case outline P), 16 pin DIP flat pack (case outline F), and leadless

ceramic chip carrier (case outline 2). Devices may be purchased with a variety of lead bend and plating options, see Selection Guide Table for details. Standard Microcircuit Drawing (SMD) parts are available for each package and lead style.

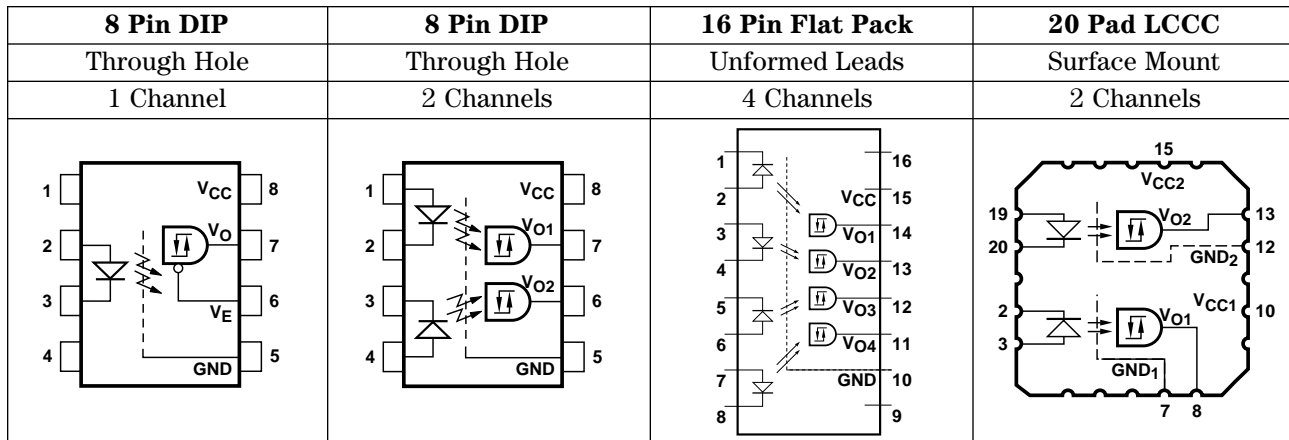
Because the same electrical die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical

specifications, and performance characteristics shown in the figures are identical for all parts. Occasional exceptions exist due to package variations and limitations and are as noted. Additionally, the same package assembly processes and materials are used in all devices. These similarities give justification for the use of data obtained from one part to represent other part's performance for die related reliability and certain limited radiation test results.

### Selection Guide—Package Styles and Lead Configuration Options

Package	8 Pin DIP	8 Pin DIP	16 Pin Flat Pack	20 Pad LCCC
Lead Style	Through Hole	Through Hole	Unformed Leads	Surface Mount
Channels	1	2	4	2
Common Channel Wiring	None	V <sub>CC</sub> , GND	V <sub>CC</sub> , GND	None
<b>Agilent Part # &amp; Options</b>				
Commercial	HCPL-5200	HCPL-5230	HCPL-6250	HCPL-6230
MIL-PRF-38534, Class H	HCPL-5201	HCPL-5231	HCPL-6251	HCPL-6231
MIL-PRF-38534, Class K	HCPL-520K	HCPL-523K	HCPL-625K	HCPL-623K
Standard Lead Finish	Gold Plate	Gold Plate	Gold Plate	Soldered Pads
Solder Dipped	Option #200	Option #200		
Butt Cut/Gold Plate	Option #100	Option #100		
Gull Wing/Soldered	Option #300	Option #300		
<b>Class H SMD Part #</b>				
Prescript for all below	5962-	5962-	5962-	5962-
Either Gold or Solder	8876801PX	8876901PX	8876903FX	88769022X
Gold Plate	8876801PC	8876901PC	8876903FC	
Solder Dipped	8876801PA	8876901PA		88769022A
Butt Cut/Gold Plate	8876801YC	8876901YC		
Butt Cut/Soldered	8876801YA	8876901YA		
Gull Wing/Soldered	8876801XA	8876901XA		
<b>Class K SMD Part #</b>				
Prescript for all below	5962-	5962-	5962-	5962-
Either Gold or Solder	8876802KPX	8876904KPX	8876906KFX	8876905K2X
Gold Plate	8876802KPC	8876904KPC	8876906KFC	
Solder Dipped	8876802KPA	8876904KPA		8876905K2A
Butt Cut/Gold Plate	8876802KYC	8876904KYC		
Butt Cut/Soldered	8876802KYA	8876904KYA		
Gull Wing/Soldered	8876802KXA	8876904KXA		

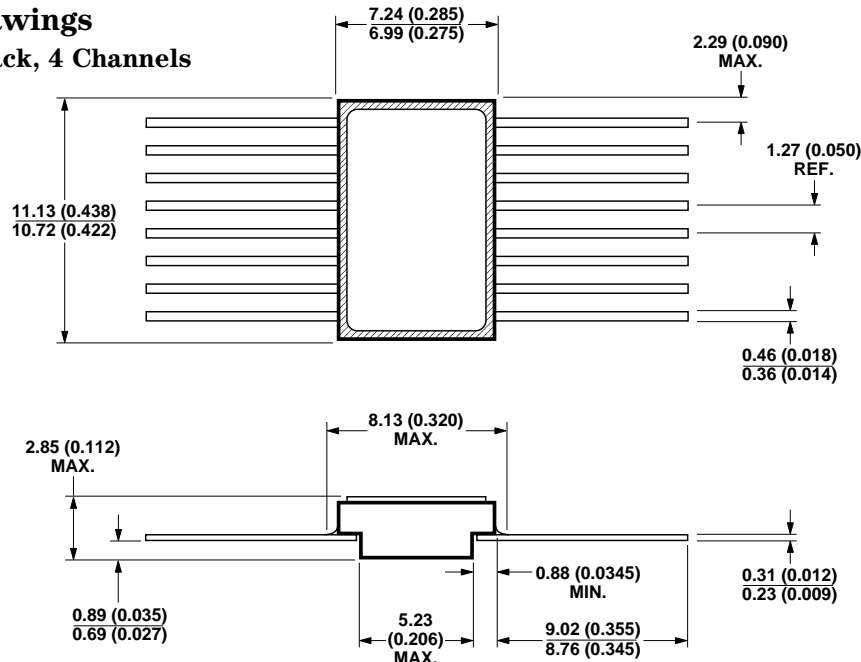
## Functional Diagrams



**Note:** Multichannel DIP and flat pack devices have common  $V_{CC}$  and ground. Single channel DIP has an enable pin 6. LCCC (leadless ceramic chip carrier) package has isolated channels with separate  $V_{CC}$  and ground connections.

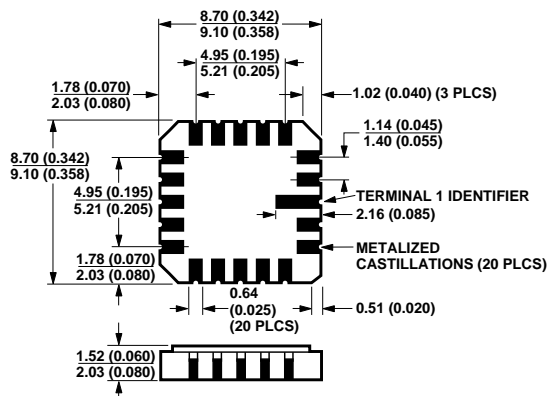
## Outline Drawings

16 Pin Flat Pack, 4 Channels



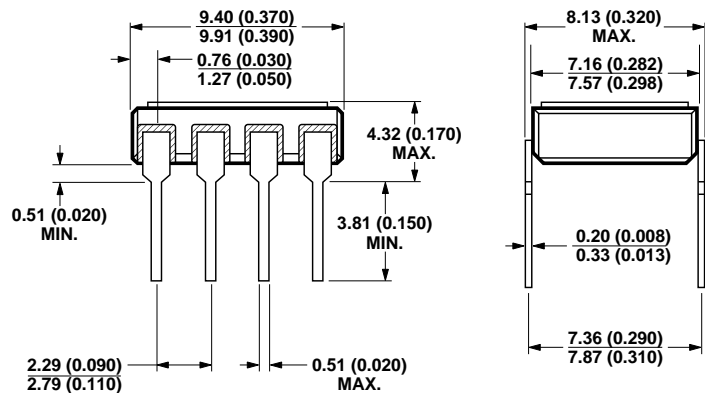
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

20 Terminal LCCC Surface Mount, 2 Channels



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).  
SOLDER THICKNESS 0.127 (0.005) MAX.

8 Pin DIP Through Hole, 1 and 2 Channel



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

## Leaded Device Marking

Agilent LOGO →	A QYYWWZ	← COMPLIANCE INDICATOR,*
Agilent P/N →	XXXXXX	← DATE CODE, SUFFIX (IF NEEDED)
DSCC SMD* →	XXXXXXXX	
DSCC SMD* →	XXX XXX	← COUNTRY OF MFR.
PIN ONE/ESD IDENT →	• 50434	← Agilent FSCN*

\*QUALIFIED PARTS ONLY

## Leadless Device Marking

Agilent LOGO →	A QYYWWZ	← COMPLIANCE INDICATOR,*
Agilent P/N →	XXXXXX	← DATE CODE, SUFFIX (IF NEEDED)
PIN ONE/ESD IDENT →	• XXXX	← DSCC SMD*
COUNTRY OF MFR. →	XXXXXXXX	← DSCC SMD*
	XXX 50434	← Agilent FSCN*

\*QUALIFIED PARTS ONLY

## Hermetic Optocoupler Options

Option	Description
100	<p>Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product in 8 pin DIP (see drawings below for details).</p> <p>NOTE: DIMENSIONS IN MILLIMETERS (INCHES).</p>
200	<p>Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product in 8 pin DIP. DSCC Drawing part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder dipped terminals as a standard feature.</p>
300	<p>Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product in 8 pin DIP (see drawings below for details). This option has solder dipped leads.</p> <p>NOTE: DIMENSIONS IN MILLIMETERS (INCHES).</p>

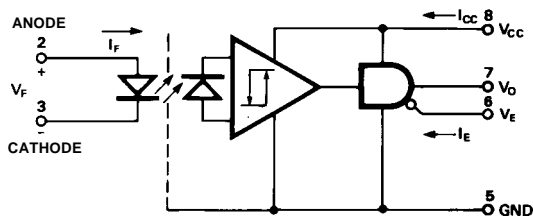
## Absolute Maximum Ratings

Storage Temperature Range, $T_S$ .....	-65°C to +150°C
Operating Temperature, $T_A$ .....	-55°C to +125°C
Case Temperature, $T_C$ .....	+170°C
Junction Temperature, $T_J$ .....	+175°C
Lead Solder Temperature .....	260°C for 10 s
Average Forward Current, $I_{F\text{ AVG}}$ (each channel) .....	8 mA
Peak Input Current, $I_{F\text{ PK}}$ (each channel) .....	20 mA <sup>[1]</sup>
Reverse Input Voltage, $V_R$ (each channel) .....	3 V
Supply Voltage, $V_{CC}$ .....	0.0 V min., 20 V max.
Average Output Current, $I_O$ (each channel) .....	15 mA
Output Voltage, $V_O$ (each channel) .....	-0.3 V min., 20 V max.
Package Power Dissipation, $P_d$ (each channel) .....	200 mW

## Single Channel Product Only

Tri-State Enable Voltage, $V_E$ .....	-0.3 V min., 20 V max.
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## 8 Pin Ceramic DIP Single Channel Schematic



Note enable pin 6. An external 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$  bypass capacitor is recommended between  $V_{CC}$  and ground for each package type.

## ESD Classification

(MIL-STD-883, Method 3015)

HCPL-5200/01/0K, HCPL-6230/31/3K .....	( $\Delta$ ), Class 1
HCPL-5230/31/3K, HCPL-6250/51/5K .....	(Dot), Class 3

## Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	$V_{CC}$	4.5	20	V
Input Current, High Level, Each Channel	$I_{FH}$	2	8	mA
Input Voltage, Low Level, Each Channel	$V_{FL}$	0	0.8	V
Fan Out (TTL Load) Each Channel	N		4	

## Single Channel Product Only

High Level Enable Voltage	$V_{EH}$	2.0	20	V
Low Level Enable Voltage	$V_{EL}$	0	0.8	V

## Electrical Characteristics

$T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $4.5\text{ V} \leq V_{CC} \leq 20\text{ V}$ ,  $2\text{ mA} \leq I_{F(\text{ON})} \leq 8\text{ mA}$ ,  $0\text{ V} \leq V_{F(\text{OFF})} \leq 0.8\text{ V}$ , unless otherwise specified.

Parameter		Sym.	Test Conditions		Group A <sup>[11]</sup> Subgroups	Limit			Units	Fig.	Notes	
						Min.	Typ.*	Max.				
Logic Low Output Voltage		V <sub>OL</sub>	I <sub>OL</sub> = 6.4 mA (4 TTL Loads)		1, 2, 3			0.5	V	1,3	2	
Logic High Output Voltage		V <sub>OH</sub>	I <sub>OH</sub> = -2.6 mA (*V <sub>OH</sub> = V <sub>CC</sub> - 2.1 V)		1, 2, 3	2.4	**		V	2,3	2	
			I <sub>OH</sub> = -0.32 mA		NA		3.1					
Output Leakage Current (V <sub>OUT</sub> > V <sub>CC</sub> )		I <sub>OHH</sub>	V <sub>O</sub> = 5.5 V	I <sub>F</sub> = 8 mA	1, 2, 3			100	μA		2	
			V <sub>O</sub> = 20 V	V <sub>CC</sub> = 4.5 V				500				
Logic Low Supply Current	Single Channel	I <sub>CCL</sub>	V <sub>CC</sub> = 5.5 V	V <sub>F</sub> = 0 V	1, 2, 3		4.5	6	mA			
	Dual Channel		V <sub>CC</sub> = 20 V	V <sub>E</sub> = Don't Care			5.3	7.5				
			V <sub>CC</sub> = 5.5 V	V <sub>F1</sub> = V <sub>F2</sub> = 0 V			9.0	12				
			V <sub>CC</sub> = 20 V				10.6	15				
			Quad Channel			V <sub>CC</sub> = 5.5 V	V <sub>F1</sub> = V <sub>F2</sub> = V <sub>F3</sub> = V <sub>F4</sub> = 0 V					14
	V <sub>CC</sub> = 20 V					17	30					
Logic High Supply Current	Single Channel	I <sub>CCH</sub>	V <sub>CC</sub> = 5.5 V	I <sub>F</sub> = 8 mA V <sub>E</sub> = Don't Care	1, 2, 3		2.9	4.5	mA			
	Dual Channel		V <sub>CC</sub> = 20 V			3.3	6					
			V <sub>CC</sub> = 5.5 V	I <sub>F1</sub> = I <sub>F2</sub> = 8 mA			5.8	9				
			V <sub>CC</sub> = 20 V				6.6	12				
			V <sub>CC</sub> = 5.5 V			I <sub>F1</sub> = I <sub>F2</sub> =		9				18
			Quad Channel			V <sub>CC</sub> = 20 V	I <sub>F3</sub> = I <sub>F4</sub> = 8 mA					11
Logic Low Short Circuit Output Current		I <sub>OSL</sub>	V <sub>O</sub> = V <sub>CC</sub> = 5.5 V	V <sub>F</sub> = 0 V	1, 2, 3	20			mA		2, 3	
			V <sub>O</sub> = V <sub>CC</sub> = 20 V			35						
Logic High Short Circuit Output Current		I <sub>OSH</sub>	V <sub>CC</sub> = 5.5 V	I <sub>F</sub> = 8 mA V <sub>O</sub> = GND	1, 2, 3			-10	mA		2, 3	
			V <sub>CC</sub> = 20 V					-25				
Input Forward Voltage		V <sub>F</sub>	I <sub>F</sub> = 8 mA		1, 2, 3	1.0	1.3	1.8	V	4	2	
Input Reverse Breakdown Voltage		BV <sub>R</sub>	I <sub>R</sub> = 10 μA		1, 2, 3	3			V		2	
Input-Output Insulation Leakage Current		I <sub>I-O</sub>	V <sub>I-O</sub> = 1500 Vdc, t = 5s RH = 45%, T <sub>A</sub> = 25°C		1			1.0	μA		4, 5	
Logic High Common Mode Transient Immunity		CM <sub>H</sub>	I <sub>F</sub> = 2 mA, V <sub>CM</sub> = 50 V <sub>P-P</sub>		9, 10, 11	1000	10,000		V/μs	9	2, 6, 12	
Logic Low Common Mode Transient Immunity		CM <sub>L</sub>	I <sub>F</sub> = 0 mA, V <sub>CM</sub> = 50 V <sub>P-P</sub>		9, 10, 11	1000	10,000		V/μs	9	2, 6, 12	
Propagation Delay Time to Logic Low		t <sub>PHL</sub>			9, 10, 11		173	350	ns	5, 6	2, 7	
Propagation Delay Time to Logic High		t <sub>PLH</sub>			9, 10, 11		118	350	ns	5, 6	2, 7	

### Electrical Characteristics Single Channel Product Only

$T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $4.5\text{ V} \leq V_{CC} \leq 20\text{ V}$ ,  $2\text{ mA} \leq I_{F(\text{ON})} \leq 8\text{ mA}$ ,  $0\text{ V} \leq V_{F(\text{OFF})} \leq 0.8\text{ V}$ ,  $2.0\text{ V} \leq V_{EH} \leq 20\text{ V}$ ,  $0\text{ V} \leq V_{EL} \leq 0.8\text{ V}$ , unless otherwise specified.

Parameter	Sym.	Test Conditions		Group A <sup>[11]</sup> Subgroups	Limits			Units	Fig.	Notes
					Min.	Typ.*	Max.			
High Impedance State Output Current	$I_{OZL}$	$V_O = 0.4\text{ V}$	$V_{EN} = 2\text{ V}$ , $V_F = 0\text{ V}$	1, 2, 3			-20	$\mu\text{A}$		
	$I_{OZH}$	$V_O = 2.4\text{ V}$	$V_{EN} = 2\text{ V}$ , $I_F = 8\text{ mA}$	1, 2, 3			20	$\mu\text{A}$		
		$V_O = 5.5\text{ V}$					100			
		$V_O = 20\text{ V}$					500			
Logic High Enable Voltage	$V_{EH}$			1, 2, 3	2.0			V		
Logic Low Enable Voltage	$V_{EL}$			1, 2, 3			0.8	V		
Logic High Enable Current	$I_{EH}$	$V_{EN} = 2.7\text{ V}$	1, 2, 3				20	$\mu\text{A}$		
		$V_{EN} = 5.5\text{ V}$					100			
		$V_{EN} = 20\text{ V}$					0.004 250			
Logic Low Enable Current	$I_{EL}$	$V_{EN} = 0.4\text{ V}$		1, 2, 3			-0.32	mA		

\*All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $I_{F(\text{ON})} = 5\text{ mA}$  unless otherwise specified.

### Typical Characteristics

All typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ ,  $I_{F(\text{ON})} = 5\text{ mA}$  unless otherwise specified.

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Notes
Input Current Hysteresis	$I_{HYS}$	0.07	mA	$V_{CC} = 5\text{ V}$	3	2
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	-1.25	mV/°C	$I_F = 8\text{ mA}$		2
Resistance (Input-Output)	$R_{I-O}$	$10^{13}$	$\Omega$	$V_{I-O} = 500\text{ Vdc}$		2, 8
Capacitance (Input-Output)	$C_{I-O}$	2.0	pF	$f = 1\text{ MHz}$		2, 8
Input Capacitance	$C_{IN}$	20	pF	$V_F = 0\text{ V}$ , $f = 1\text{ MHz}$		2, 10
Output Rise Time (10-90%)	$t_r$	45	ns		5, 7	2
Output Fall Time (90-10%)	$t_f$	10	ns		5, 7	2

### Typical Characteristics (cont'd.)

All typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$ ,  $I_{F(ON)} = 5\text{ mA}$ , unless otherwise specified.

#### Single Channel Product Only

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Notes
Output Enable Time to Logic High	$t_{PZH}$	30	ns		8	
Output Enable Time to Logic Low	$t_{PZL}$	30	ns		8	
Output Disable Time from Logic High	$t_{PHZ}$	45	ns		8	
Output Disable Time from Logic Low	$t_{PLZ}$	55	ns		8	

#### Dual and Quad Channel Products Only

Input-Input Insulation Leakage Current	$I_{I-I}$	0.5	nA	$RH = 45\%$ , $T_A = 25^\circ\text{C}$ , $V_{I-I} = 500\text{ V}$ , $t = 5\text{ s}$		9
Resistance (Input-Input)	$R_{I-I}$	$10^{13}$	$\Omega$	$V_{I-I} = 500\text{ V}$		9
Capacitance (Input-Input)	$C_{I-I}$	1.5	pF	$f = 1\text{ MHz}$		9

#### Notes:

1. Peak Forward Input Current pulse width  $< 50\text{ }\mu\text{s}$  at 1 KHz maximum repetition rate.
2. Each channel of a multichannel device.
3. Duration of output short circuit time not to exceed 10 ms.
4. All devices are considered two-terminal devices: measured between all input leads or terminals shorted together and all output leads or terminals shorted together.
5. This is a momentary withstand test, not an operating condition.
6.  $CM_L$  is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ( $V_o < 0.8\text{ V}$ ).  $CM_H$  is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ( $V_o > 2.0\text{ V}$ ).
7.  $t_{PHL}$  propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The  $t_{PLH}$  propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
8. Measured between each input pair shorted together and all output connections for that channel shorted together.
9. Measured between adjacent input pairs shorted together for each multichannel device.
10. Zero-bias capacitance measured between the LED anode and cathode.
11. Standard parts receive 100% testing at  $25^\circ\text{C}$  (Subgroups 1 and 9). SMD, Class H and Class K parts receive 100% testing at 25, 125, and  $-55^\circ\text{C}$  (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
12. Parameters are tested as part of device initial characterization and after design and process changes. Parameters guaranteed to limits specified for all lots not specifically tested.

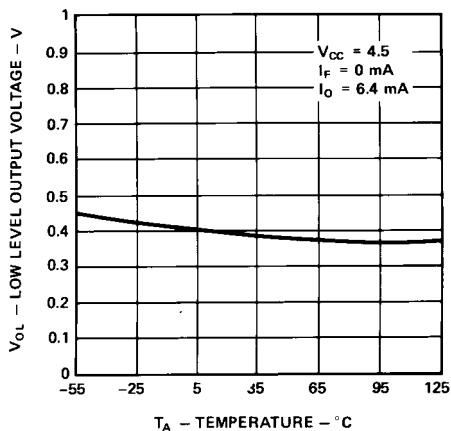


Figure 1. Typical Logic Low Output Voltage vs. Temperature.

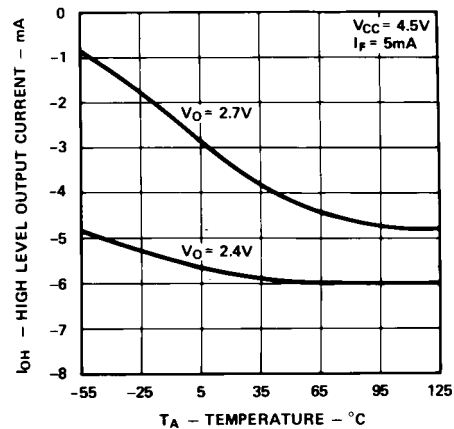


Figure 2. Typical Logic High Output Current vs. Temperature.



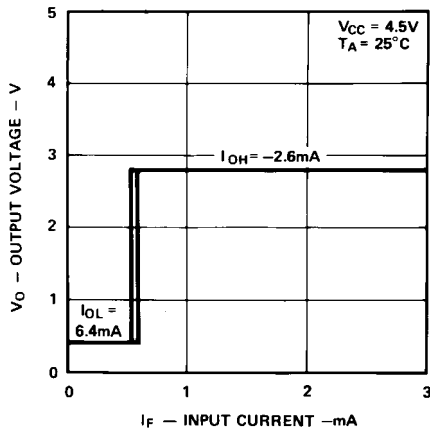


Figure 3. Output Voltage vs. Forward Input Current.

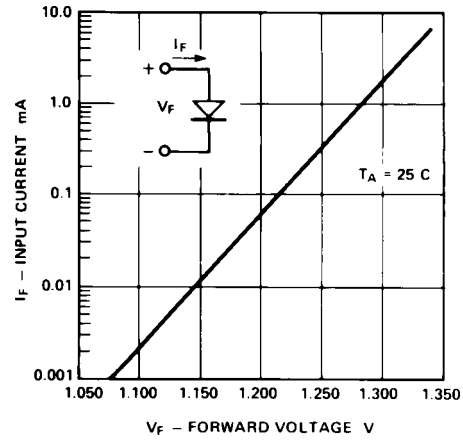


Figure 4. Typical Diode Input Forward Characteristic.

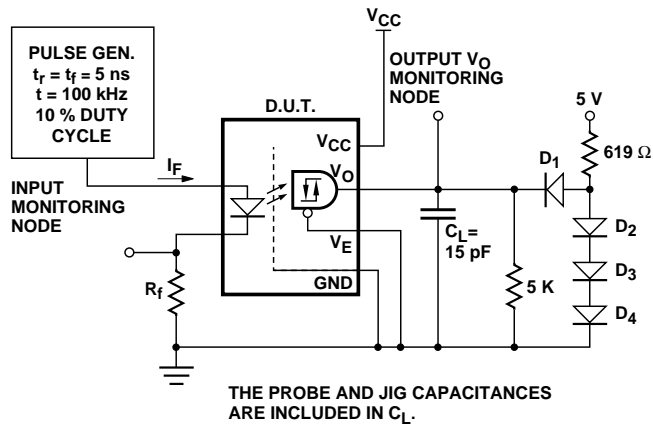


Figure 5. Test Circuit for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$ , and  $t_f$ .

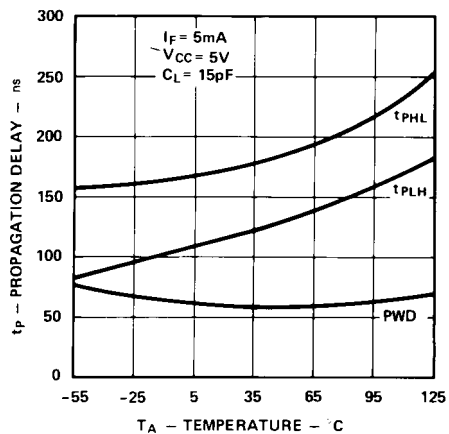
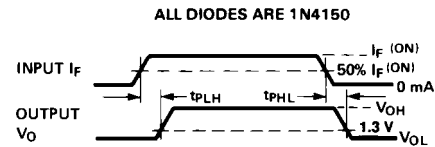


Figure 6. Typical Propagation Delay vs. Temperature.

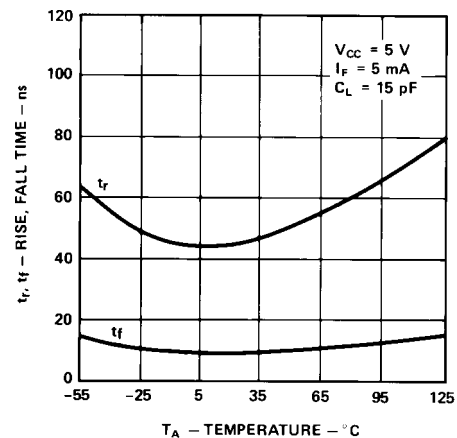


Figure 7. Typical Rise, Fall Time vs. Temperature.

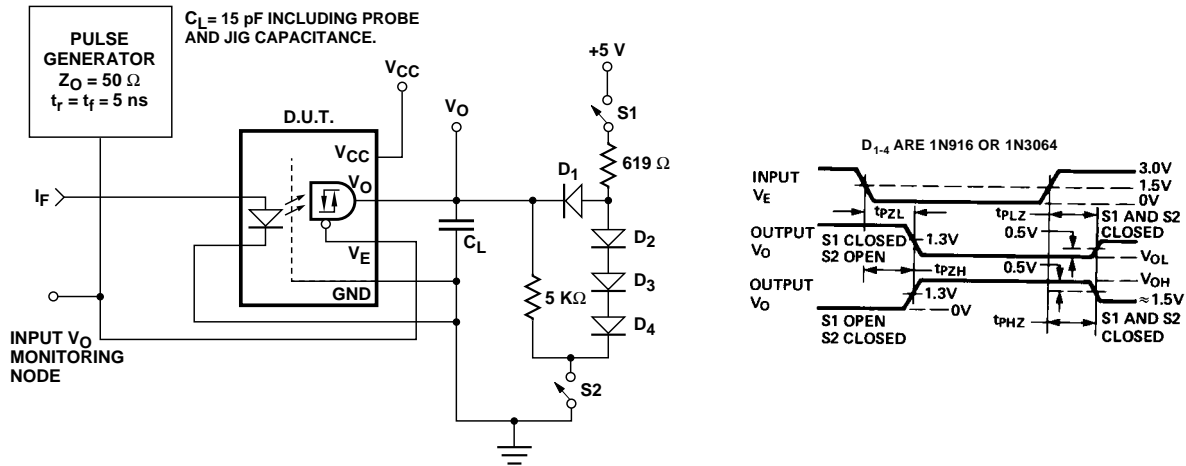


Figure 8. Test Circuit for  $t_{PHZ}$ ,  $t_{PZH}$ ,  $t_{PLZ}$ , and  $t_{PZL}$ .

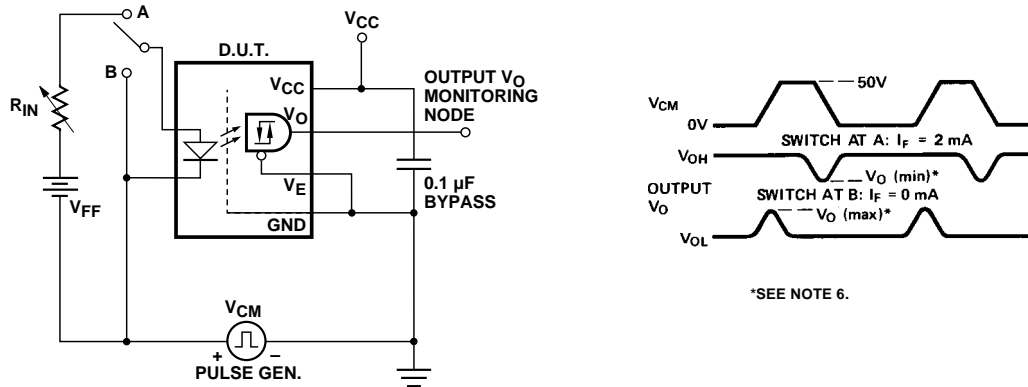


Figure 9. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

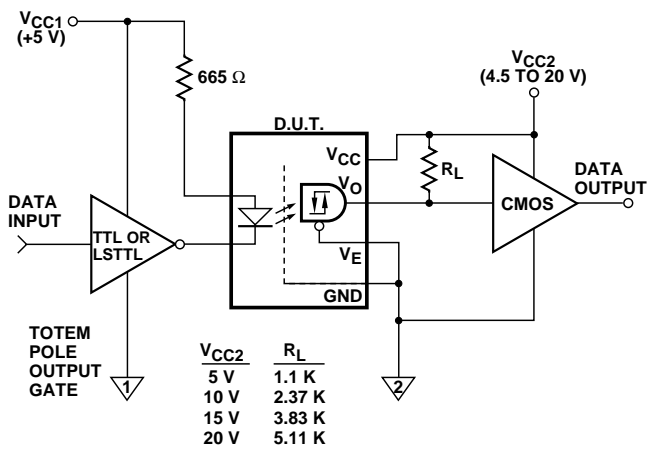


Figure 10. LSTTL to CMOS Interface Circuit.

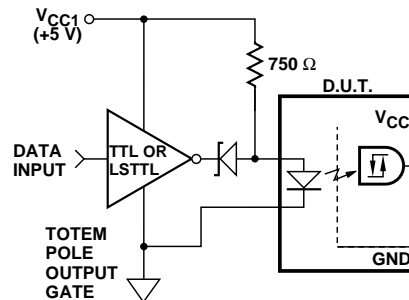


Figure 11. Recommended LED Drive Circuit.

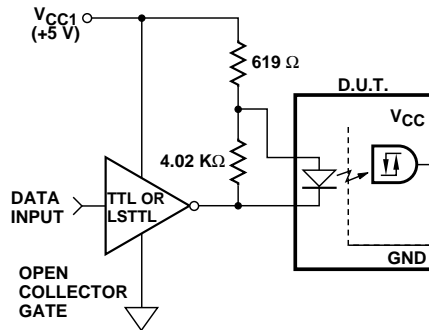


Figure 12. Series LED Drive with Open Collector Gate  
(4.02 k $\Omega$  Resistor Shunts  $I_{OH}$  from the LED).

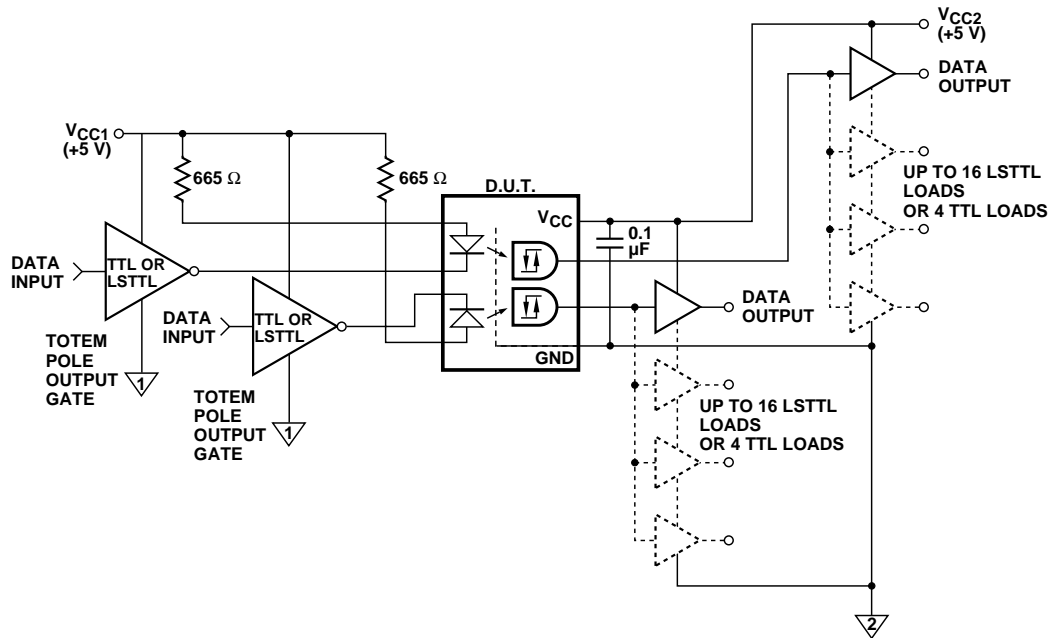
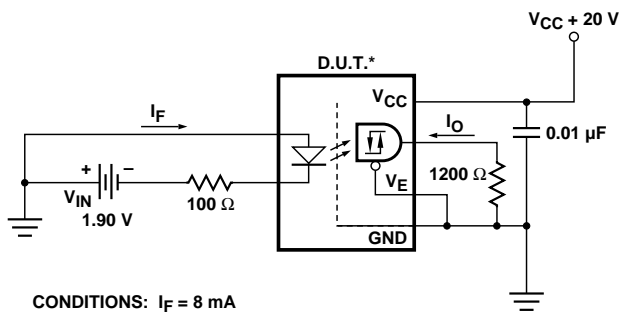


Figure 13. Recommended LSTTL to LSTTL Circuit.



CONDITIONS:  $I_F = 8 \text{ mA}$   
 $I_O = -14 \text{ mA}$

$T_A = +125^\circ\text{C}$

\*ALL CHANNELS TESTED SIMULTANEOUSLY.

Figure 14. Single Channel Operating Circuit for Burn-in and Steady State Life Tests.

## **MIL-PRF-38534 Class H, Class K, and DSCC SMD Test Program**

Agilent's Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Classes H and K. Class H and Class K devices are also in compliance with DSCC drawings 5962-88768 and 5962-88769.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.