

# 21–23 GHz GaAs MMIC Medium Power Amplifier



AA022P2-00

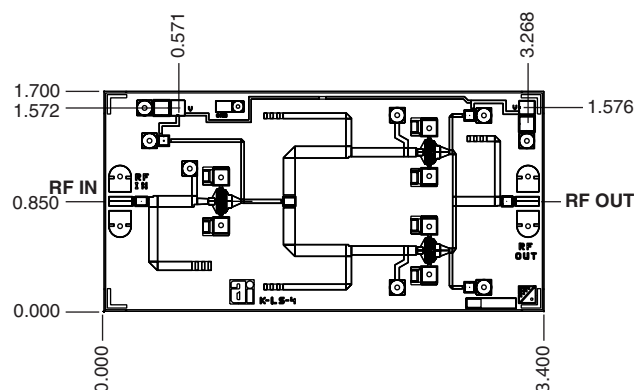
## Features

- Single Bias Supply Operation (6 V)
- 22 dBm Typical  $P_{1\text{ dB}}$  Output Power at 23 GHz
- 14 dB Typical Small Signal Gain
- 0.25  $\mu\text{m}$  Ti/Pd/Au Gates
- 100% On-Wafer RF and DC Testing
- 100% Visual Inspection to MIL-STD-883 MT 2010

## Description

Alpha's two-stage balanced K band GaAs MMIC power amplifier has a typical  $P_{1\text{ dB}}$  of 22 dBm with 13 dB associated gain guaranteed across frequency range 21–23 GHz. The chip uses Alpha's proven 0.25  $\mu\text{m}$  MESFET technology, and is based upon MBE layers and electron beam lithography for the highest uniformity and repeatability. The FETs employ surface passivation to ensure a rugged reliable part with through-substrate via holes and gold-based backside metallization to facilitate a conductive epoxy die attach process. All chips are screened for small signal S-parameters and power characteristics prior to shipment for guaranteed performance.

## Chip Outline



Dimensions indicated in mm.

All DC (V) pads are 0.1 x 0.1 mm and RF In, Out pads are 0.07 mm wide.

Chip thickness = 0.1 mm.

## Absolute Maximum Ratings

| Characteristic                   | Value             |
|----------------------------------|-------------------|
| Operating Temperature ( $T_C$ )  | -55°C to +90°C    |
| Storage Temperature ( $T_{ST}$ ) | -65°C to +150°C   |
| Bias Voltage ( $V_D$ )           | 7 V <sub>DC</sub> |
| Power In ( $P_{IN}$ )            | 19 dBm            |
| Junction Temperature ( $T_J$ )   | 175°C             |

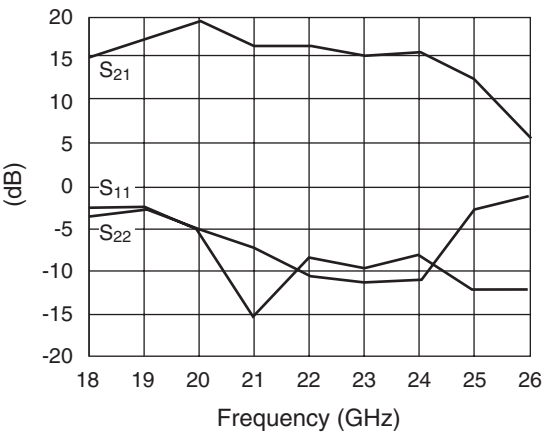
## Electrical Specifications at 25°C ( $V_{DS} = 6\text{ V}$ )

| Parameter                             | Condition     | Symbol            | Min. | Typ. <sup>2</sup> | Max. | Unit |
|---------------------------------------|---------------|-------------------|------|-------------------|------|------|
| Drain Current (at Saturation)         |               | $I_{DS}$          |      | 280               | 300  | mA   |
| Small Signal Gain                     | F = 21–23 GHz | G                 | 12   | 14                |      | dB   |
| Input Return Loss                     | F = 21–23 GHz | $RL_I$            |      | -8                | -6   | dB   |
| Output Return Loss                    | F = 21–23 GHz | $RL_O$            |      | -9                | -7   | dB   |
| Output Power at 1 dB Gain Compression | F = 23 GHz    | $P_{1\text{ dB}}$ | 19   | 22                |      | dBm  |
| Saturated Output Power                | F = 23 GHz    | $P_{SAT}$         | 21   | 23.5              |      | dBm  |
| Gain at Saturation                    | F = 23 GHz    | $G_{SAT}$         |      | 11                |      | dB   |
| Thermal Resistance <sup>1</sup>       |               | $\Theta_{JC}$     |      | 69                |      | °C/W |

1. Calculated value based on measurement of discrete FET.

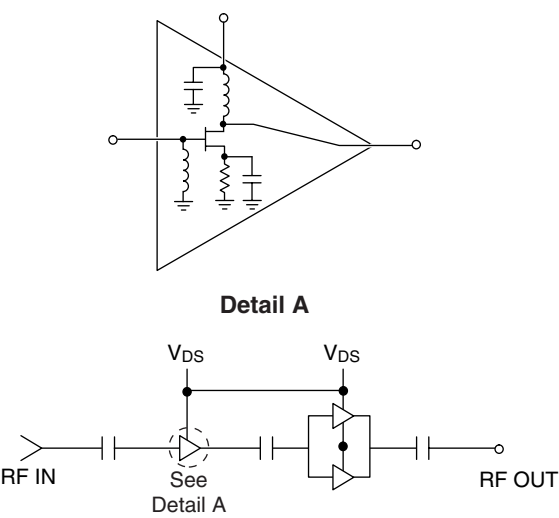
2. Typical represents the median parameter value across the specified frequency range for the median chip.

Typical Performance Data

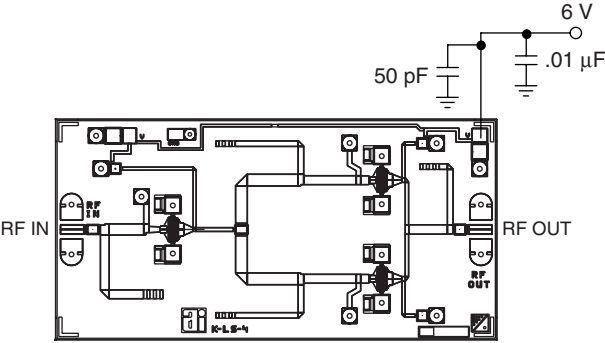


Typical Small Signal Performance  
S-Parameters ( $V_{DS} = 6\text{ V}$   $I_{DS} = 240\text{ mA}$ ,  
 $T_A = 25^\circ\text{C}$ )

Circuit Schematic



Bias Arrangement



For biasing on, adjust  $V_{DS}$  from zero to the desired value (6 V recommended). For biasing off, reverse the biasing on procedure.