

### DESCRIPTION

The S3019 evaluation board provides a flexible platform for verifying the operation of the S3019 transceiver interface circuit. This document provides information on the board contents. It should be used in conjunction with the S3019 data sheet, which contains full technical details on the chips operation.

Figure 1 shows the outline of the S3019 evaluation board. Figure 2 shows the block diagram of how the S3019 evaluation board should be connected to test equipment for Bit Error Rate (BER) testing. Figure 3 shows the test setup for BER measurements and jitter testing.

**Figure 1. S3019 Evaluation Board Top View**

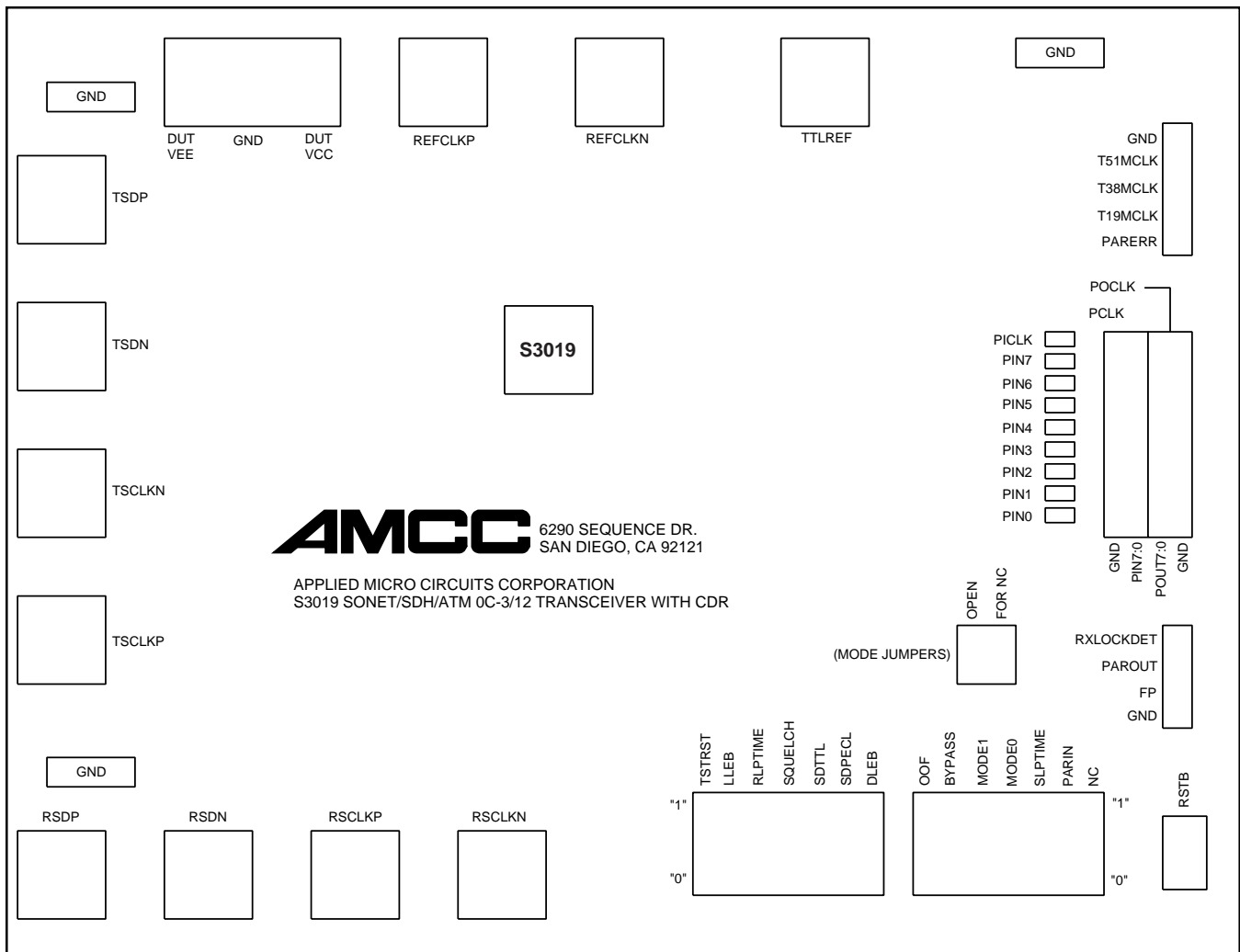
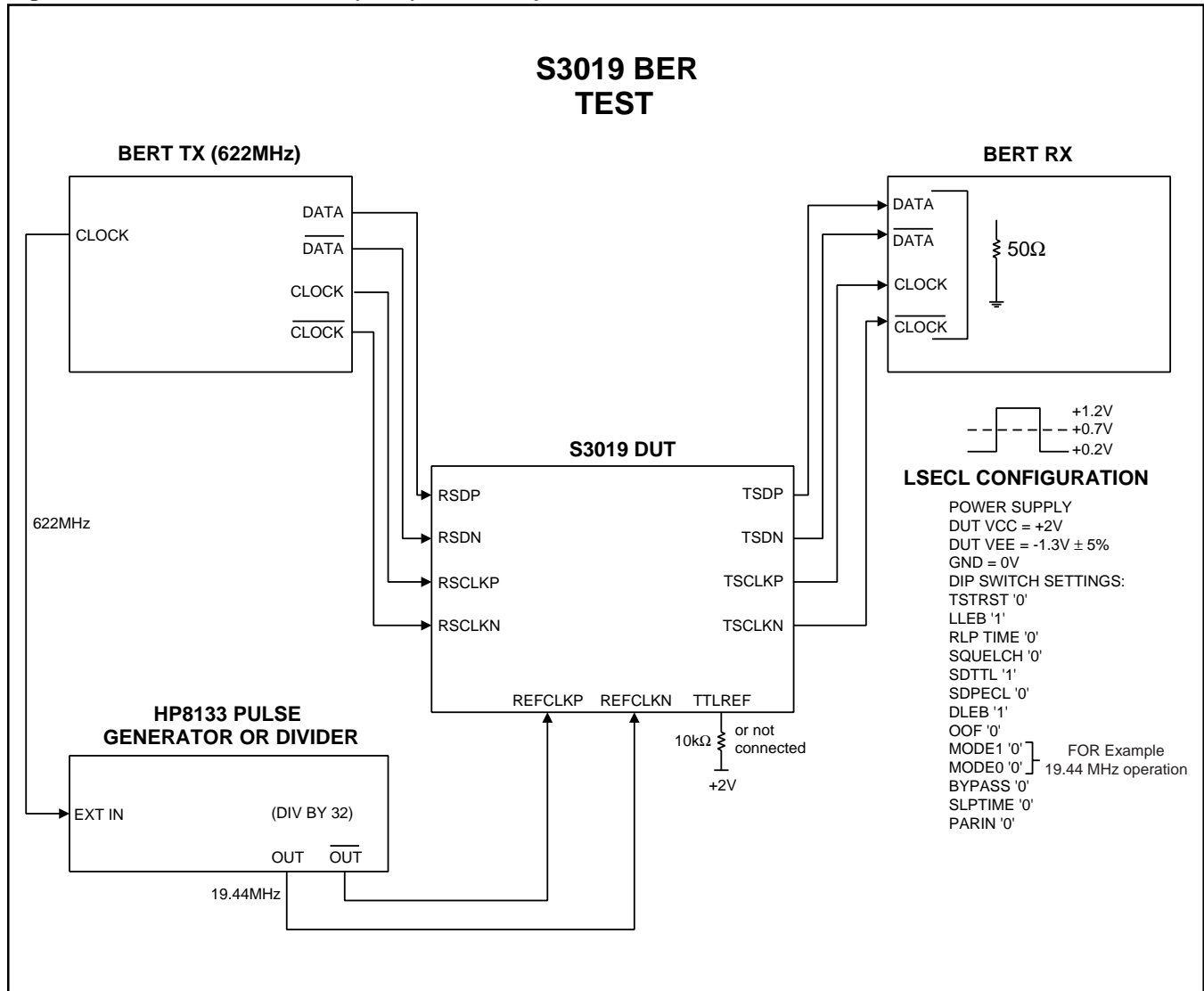


Figure 2 depicts how the S3019 evaluation board can be connected for BER measurements, and shows all of the DIP switch settings. In addition, it shows the Level Shifted ECL (LSECL) power supply requirements for use with test equipment that utilizes 50  $\Omega$  to ground termination. In this configuration the S3019 is configured for use with the internal S3019 Clock Recovery Unit (CRU), using a 19.44 MHz reference and operating at STS-12.

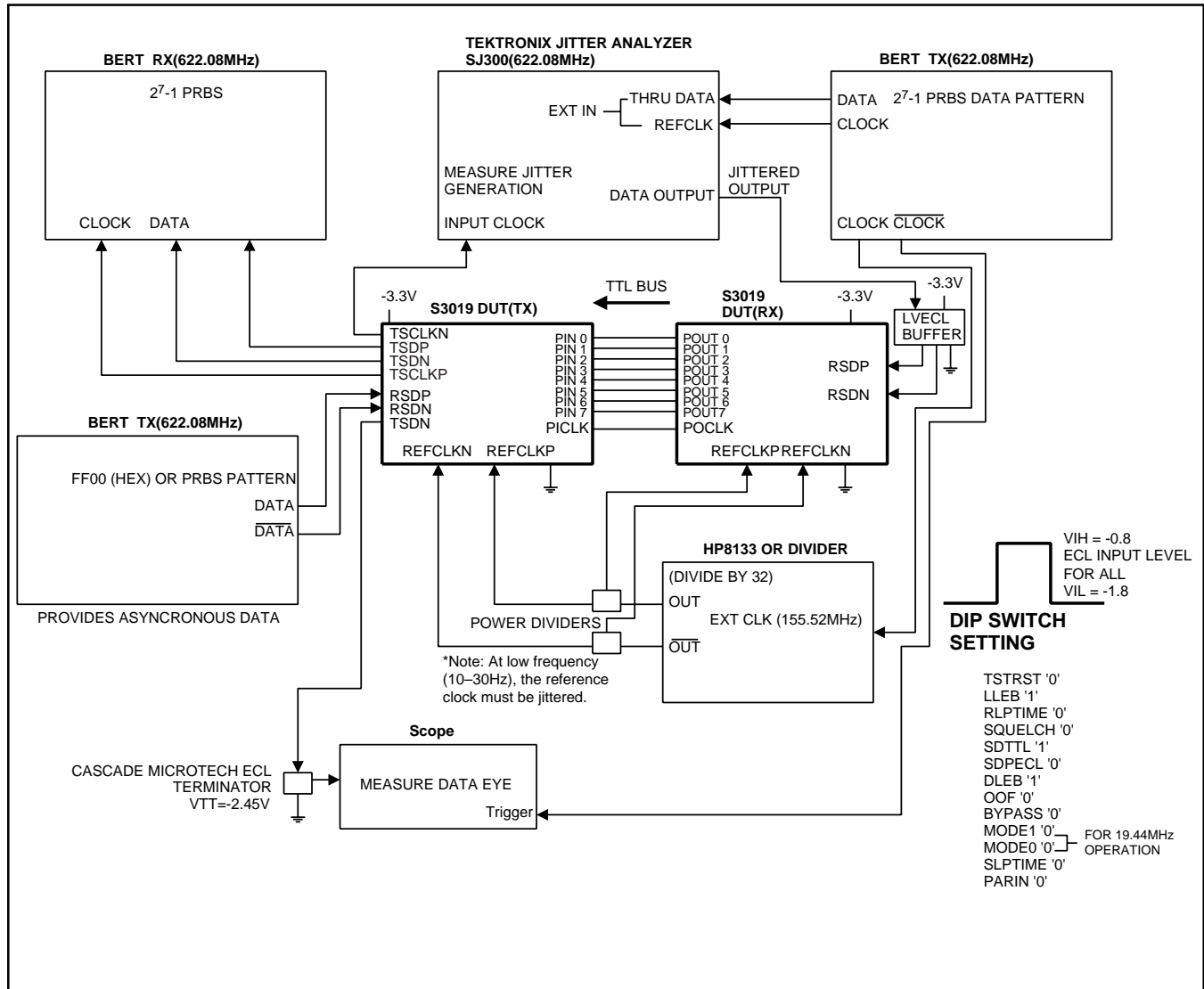
**Figure 2. S3019 Bit Error Rate (BER) Test Setup**



Note: When using the internal CRU, CLOCK and  $\overline{\text{CLOCK}}$  does not need to be connected to RSCLKP and RSCLKN.

Figure 3 depicts how two S3019 evaluation boards can be connected for BER measurements and jitter testing, and shows all of the DIP switch settings. In addition, it shows the power supply requirements for use with test equipment that utilizes 50  $\Omega$  to -2V termination. These settings are for STS-12 testing.

Figure 3. S3019 Evaluation Board BER Measurement and Jitter Testing Setup



### ELECTRICAL CONNECTIONS

#### Power Connections

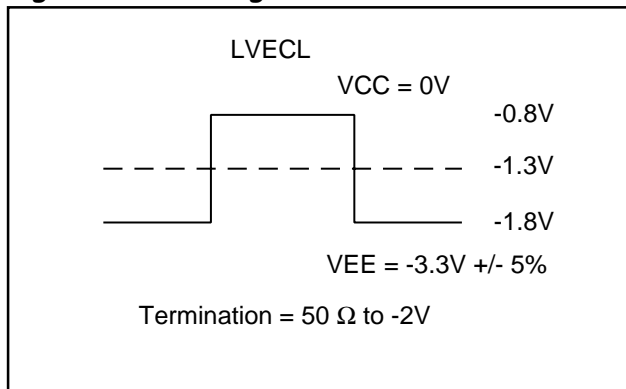
Terminal posts are provided at the top edge of the board for VCC and VEE. The S3019 evaluation board can be configured with ECL, PECL and Level Shifted (LSECL) I/O, so the board can be configured to operate with different types of standard test equipment. Figures 4 through 6 demonstrate the different types of input and output waveforms that the S3019 evaluation board can operate with the different voltage settings of VCC and VEE per Table 1. Note the TTL I/O's voltage level will change to non-standard levels when the S3019 evaluation board is powered by the different voltage.

The external test equipment environment or other standard ECL and/or +3.3V referenced ECL systems can interface to the S3019 evaluation board. The board as shown by Figures 1 through 3 can be powered to allow easy connection to the 50  $\Omega$  to ground inputs of high performance oscilloscopes and spectrum analyzers as well as the standard ECL I/O of serial Bit Error Rate Testers (BERT) and jitter analyzers. Table 1 illustrates the nominal input voltages for the DUT VCC and VEE voltage levels shown in Figures 4 through 6. Figures 4 and 5 show that the voltages track with VEE, and Figure 6 shows that the voltages track with VCC.

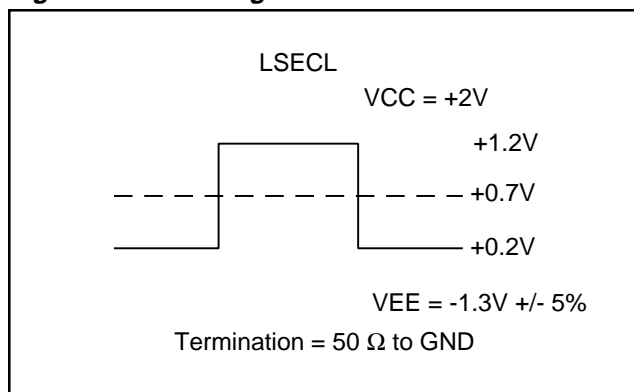
**Table 1. Power Connections for DUT and Test Equipment Interface**

Power Supply	Nominal Input Voltage	Type of Signal	ECL Output Termination
DUT VCC DUT VEE	+3.3V 0V	LVPECL	50 $\Omega$ to VCC -2V
DUT VCC DUT VEE	0V -3.3V	LVECL	50 $\Omega$ to -2V
DUT VCC DUT VEE	+2V -1.3V	LSECL	50 $\Omega$ to GND

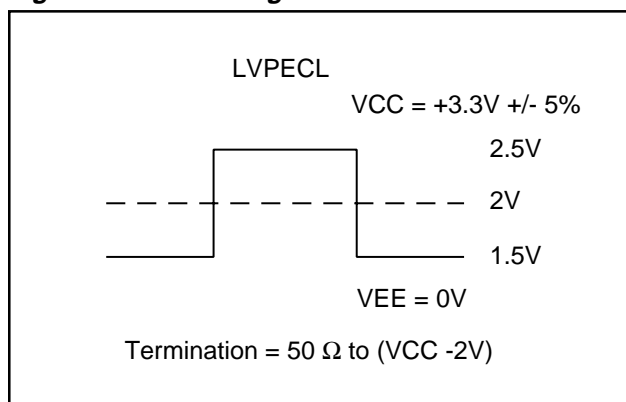
**Figure 4. LVECL Signal Waveform**



**Figure 5. LSECL Signal Waveform**



**Figure 6. LVPECL Signal Waveform**



### SMA Connectors

SMA connectors are provided for the differential serial data input/output signals and output clocks. Additional SMA connectors are provided for an optional differential serial input clock, the external TTL reference clock and the optional external parallel input clock.

**Receive Serial Data [RSDP/N]** — Differential LVPECL inputs. Serial data inputs of the S3019.

**Receive Serial Clock [RSCLKP/N]** — Differential LVPECL inputs. These inputs are used in bypass mode to supply a clock input for the RSDP/N. This should be tied to a logic zero when not in bypass mode.

**Transmit Serial Data Out [TSDP/N]** — Differential LVPECL outputs. The serial output data stream from the transmitter section of the S3019. The outputs can drive PECL, ECL, or ground terminated instrument inputs depending on the power supply voltages applied to the S3019 evaluation board.

**Transmit Clock Output [TSCLKP/N]** — Differential LVPECL outputs. The transmit serial clock that can be used to re-time the TSDP/N signal. The outputs can drive PECL, ECL, or ground terminated instrument inputs depending on the power supply voltages applied to the S3019 evaluation board. This clock will be 622.08 MHz or 155.52 MHz, depending on the operating mode.

**Reference Clock [REFCLKP/N]** — Differential LVPECL inputs. These inputs must be provided with a differential level (depending on the power supply voltages) clock of 19.44 MHz, 38.8 MHz, 51.84 MHz or 77.76 MHz as selected by the MODE[1:0] switches of the DIP switch. These inputs must be connected to a logic one state (REFCLKP = "1", & REFCLKN = "0") if TTLREF is used.

**TTL Reference Clock [TTLREF]** — LVTTTL input. These inputs must be provided with a TTL (swing levels dependent on the power supply voltages) clock of 19.44 MHz, 38.88 MHz, 51.84 MHz or 77.76 MHz as selected by the MODE[1:0] switches of the DIP switch. These inputs must be tied high if REFCLKP/N is used.

### Parallel I/O Header Terminals

The parallel input (PIN[7:0]) and output (POUT[7:0]) data to and from the S3019 transceiver are available at a 4 x 9 pin header array at the right edge of the evaluation board. Ground pin columns are also provided to allow connection with 0.1" grid shielded ribbon cable to parallel data sources and data analyzers.

User selectable jumpers also allow the parallel output data (POUT[7:0]) and the output byte clock (POCLK) to be directly connected to the transmitter parallel data inputs (PIN[7:0]) and the Parallel Input Clock (PICLK). Note: The board must be supplied with an external reference via REFCLKP/N for proper operation. (See Figure 2.)

**Parallel Clock [PCLK]** — LVTTTL output. The word rate output reference from the transmitter PLL. This output is used to coordinate byte-wide transfers via the parallel data bus.

A separate 5-pin header is also provided for four additional signals. The four signals are identified below:

**19 MHz Clock Output [T19MCLK]** — LVTTTL output. A 19.44 MHz output derived from the S3019 PLL available at the header pin for monitoring.

**38 MHz Clock Output [T38MCLK]** — LVTTTL output. A 38.88 MHz output derived from the S3019 PLL available at the header pin for monitoring.

**51 MHz Clock Output [T51MCLK]** — LVTTL output. A 51.84 MHz output derived from the S3019 PLL available at the header pin for monitoring.

**Parity Error [PARERR]** — LVTTL output. Indicates that a parity error has been detected on the PIN[7:0] data bus and the Parity Input (PARIN) for the previous data bus.

A separate 4-pin header is also provided for control of the No Connect (NC) of the MODE[1:0] DIP switch setting. This allows the S3019 evaluation board to run in STS-3 mode with different reference voltages as outlined in the S3019 data sheet. The No Connect (NC) is obtained by removing the header shorting jumper. There are two of these jumpers, one for each MODE[1:0] signal. For proper operation at least one of these jumpers must remain connected.

A separate 4-pin header is provided for three additional signals identified below:

**Frame Pulse [FP]** — LVTTL output. Indicates frame boundaries in the incoming data stream (RSDP/N).

**Parity Output [PAROUT]** — LVTTL output. Odd parity is calculated on the POUT[7:0] output.

**Lock Detect [RXLOCKDET]** — LVTTL output. Indicates that the CRU has locked onto the incoming data stream. This signal is set high when the CRU is locked.

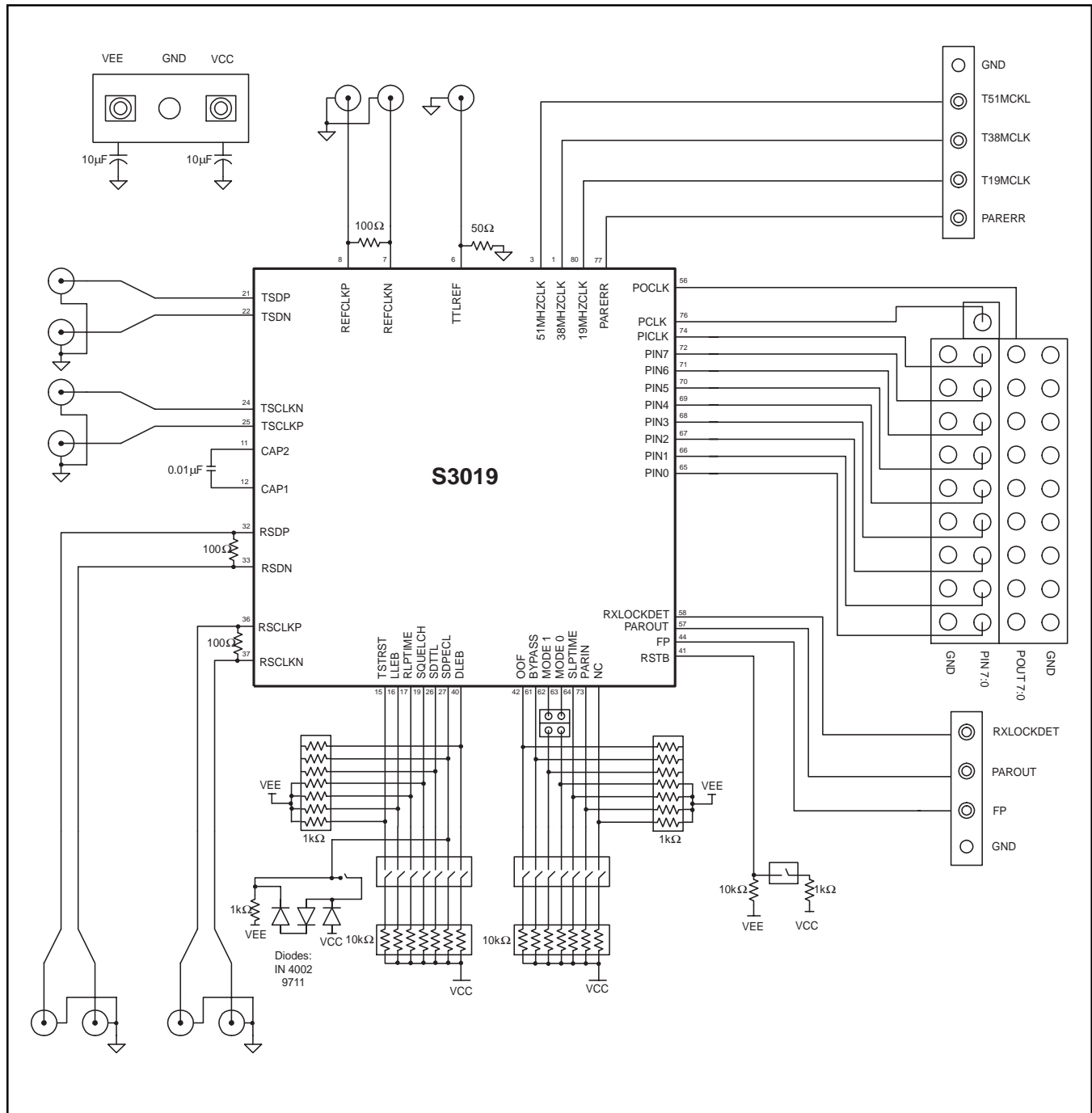
## **DIP SWITCHES**

The evaluation board is equipped with two DIP switches, to control the static control functions of the on-board device. For both arrays the OFF (open = "0") condition of the DIP switch asserts a logic low on the assigned signal, and the ON (closed = "1") condition asserts a logic high. Figures 2 and 3 show the particular DIP switch settings that are needed for a particular test case.

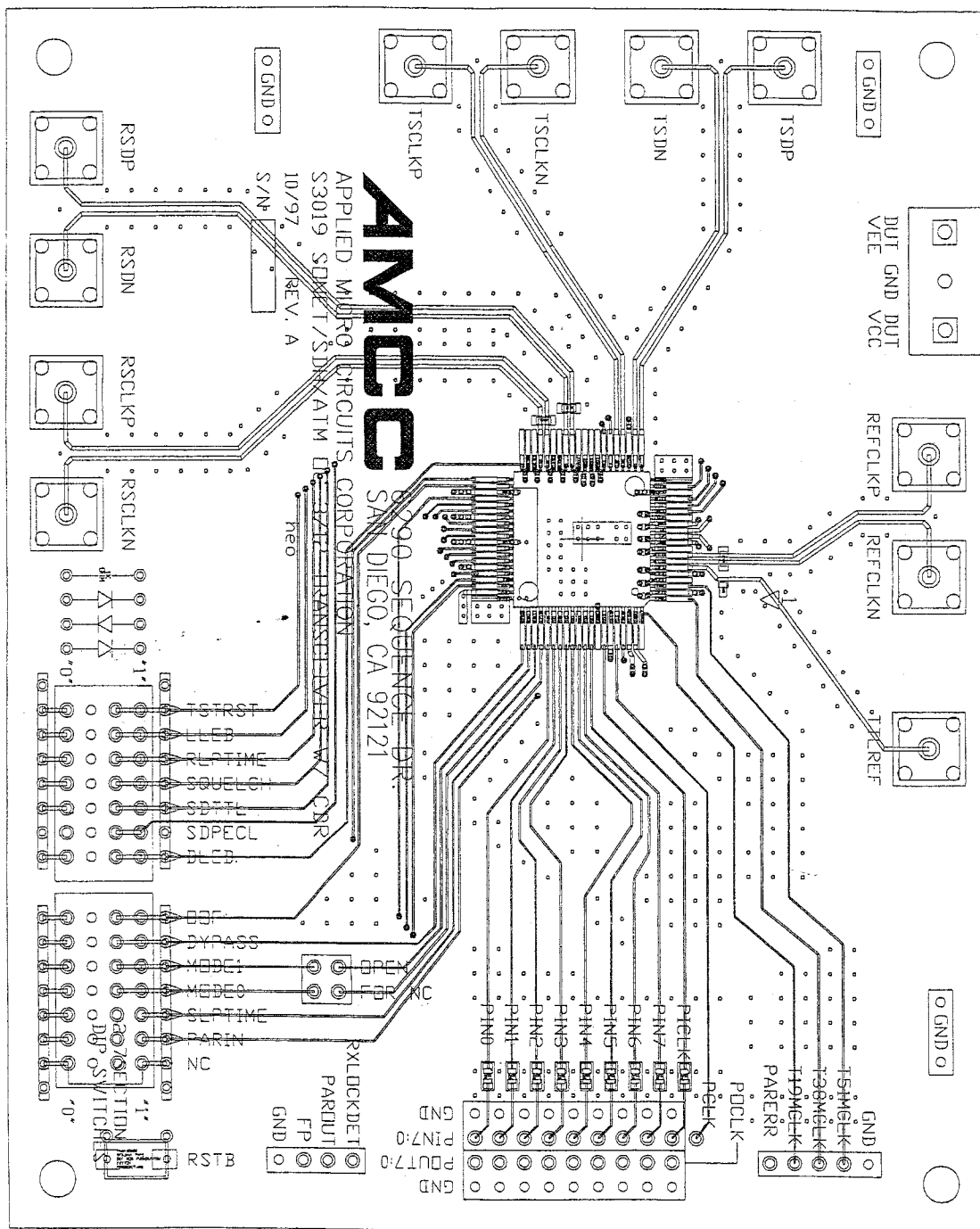
**RSTB Pushbutton Switch** — This momentary contact switch controls the master reset of the S3019.

Please refer to the S3019 data sheet for details of the specific control functions. Normal mode for this master reset input is High. Depressing the switch connects this input to a logic zero and resets the S3019.

Figure 7. S3019 Evaluation Board Schematic

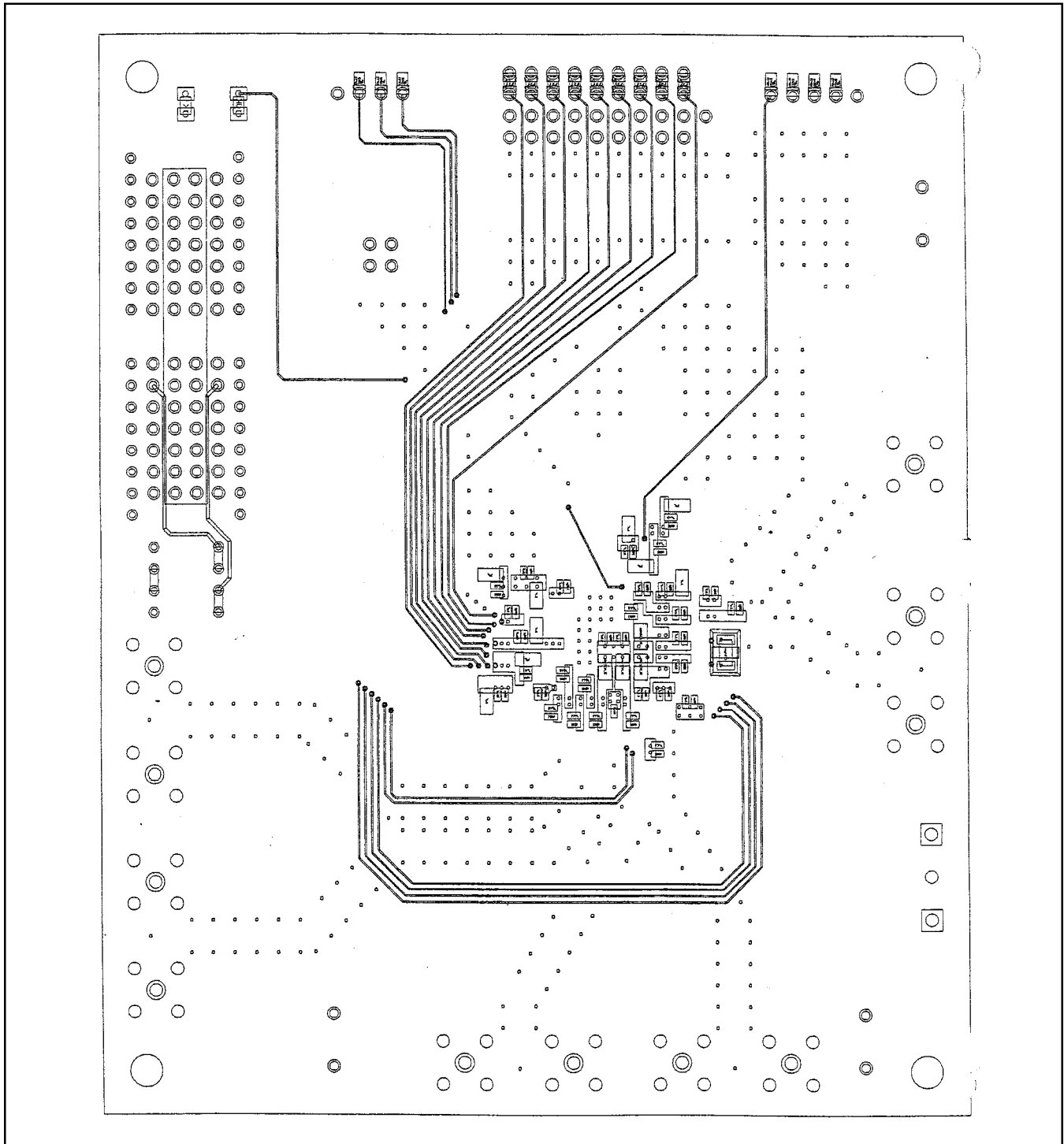


**Figure 8. Evaluation Board Layout Top View**





*Figure 9. Evaluation Board Layout Bottom View*



**Ordering Information**

PREFIX	DEVICE	PACKAGE
EV – Evaluation Board	3019	A – 80 PQFP

XX  
Prefix

XXXX  
Device

X  
Package



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