

FEATURES

- Complies with Bellcore and ITU-T specifications for jitter tolerance, jitter transfer and jitter generation
- On-chip high frequency PLL with internal loop filter for clock recovery
- Supports clock recovery for OC-12/STM-4 (622.08 Mbit/s) or OC-3/STM-1 (155.52 Mbit/s) NRZ data
- 19.44 MHz reference frequency
- Lock detect—monitors frequency
- 260mW typical power dissipation
- Low-jitter LVPECL interface
- Maintains downstream clock in absence of data inputs
- 3.3V supply
- Available in a 20 TSSOP package
- Active Low LVPECL Signal Detect

GENERAL DESCRIPTION

The function of the S3023 clock recovery unit is to derive high speed timing signals for SONET/SDH-based equipment. The S3023 is implemented using AMCC's proven Phase Locked Loop (PLL) technology.

The S3023 receives either an OC-12/STM-4 or OC-3/STM-1 scrambled NRZ signal and recovers the clock from the data. The chip outputs a differential LVPECL bit clock and retimed data. Figure 1 shows a typical network application.

The S3023 utilizes an on-chip PLL which consists of a phase detector, a loop filter, and a voltage controlled oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the reference frequency. A loop filter converts the phase detector output into a smooth DC voltage, and the DC voltage is input to the VCO whose frequency is varied by this voltage. A block diagram is shown in Figure 2.

Figure 1. System Block Diagram

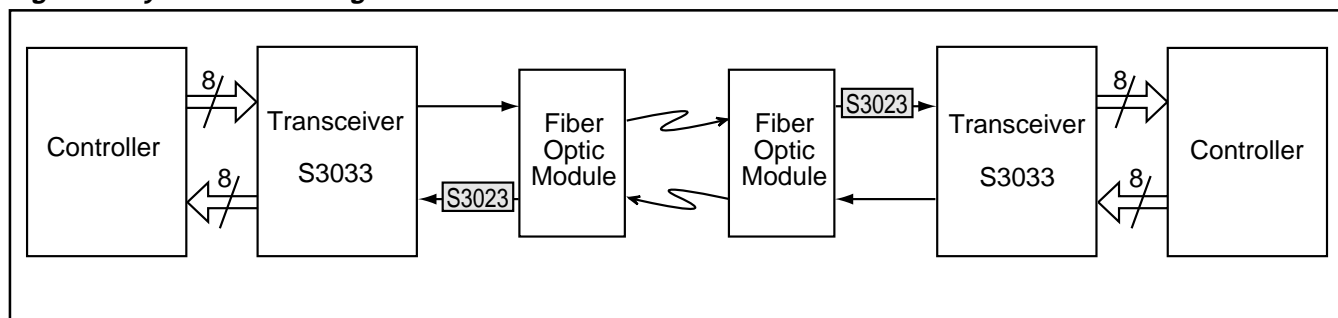
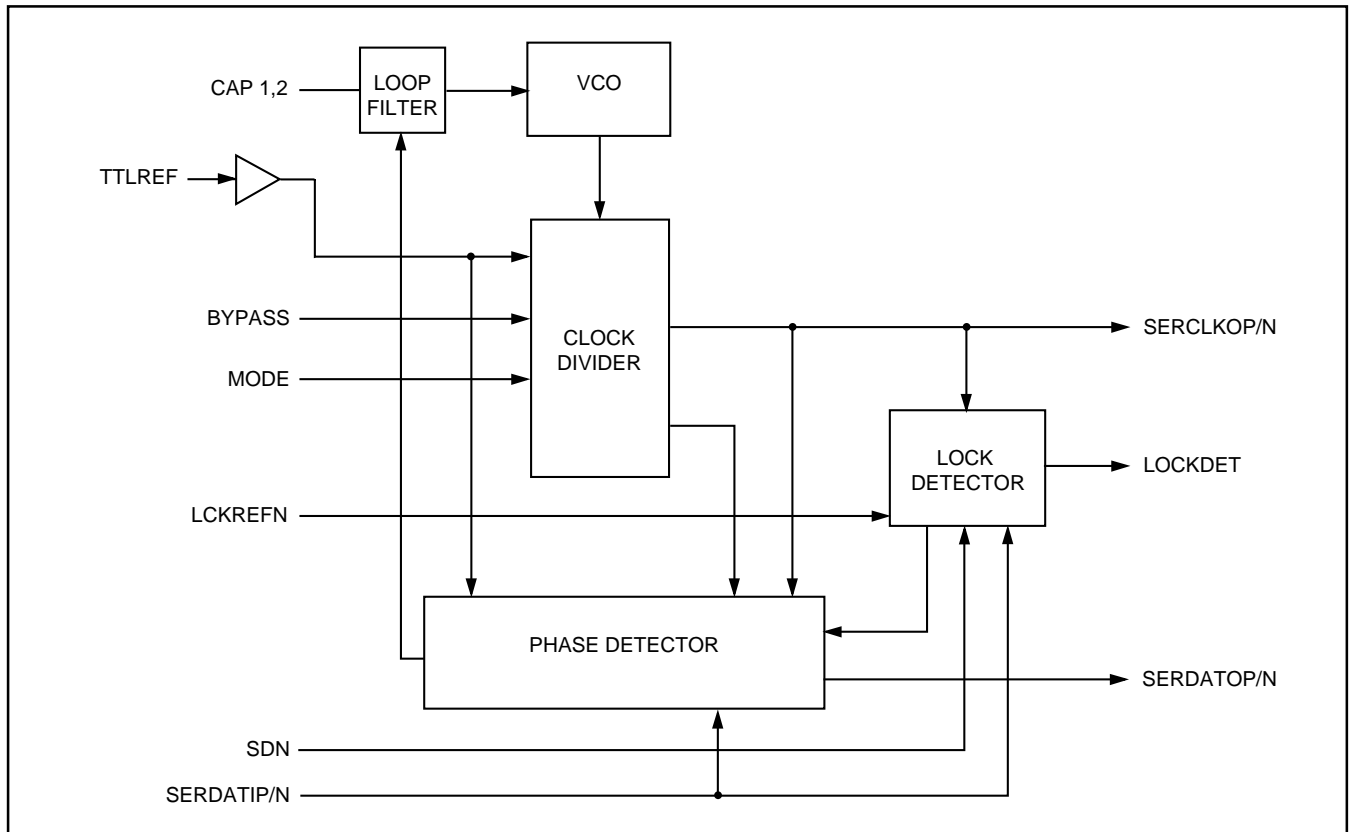


Figure 2. Functional Block Diagram



OVERVIEW

The S3023 supports clock recovery for the OC-12/STM-4 or OC-3/STM-1 data rates. Differential serial data is input to the chip at the specified rate and clock recovery is performed on the incoming data stream. An external crystal is required to minimize the PLL lock time and provide a stable output clock source in the absence of serial input data. Retimed data and clock are output from the S3023.

CHARACTERISTICS

Performance

The S3023 PLL complies with the jitter specifications proposed for SONET/SDH equipment defined by the T1X1.6/91-022 document, when used with differential inputs and outputs as shown in Figure 3.

Jitter Transfer

The jitter transfer function is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. Jitter transfer requirements are shown in Figure 5. The measurement condition is that input sinusoidal jitter up to the mask level in Figure 4 be applied for each of the OC-N/STS-N rates.

Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. SONET input jitter tolerance requirements are shown in Figure 4. The measurement condition is the input jitter amplitude which causes an equivalent of 1 dB power penalty.

Serial Data Output Set-up and Hold Time

The output set-up and hold times are represented by the waveforms shown in Figure 3.

Jitter Generation

The jitter generation of the serial clock and serial data outputs shall not exceed 0.01 UI when a serial data input with less than 14ps (OC-12) or 56ps (OC-3) rms jitter is presented to the serial data inputs.

Figure 3. Clock Output to Data Transition Delay

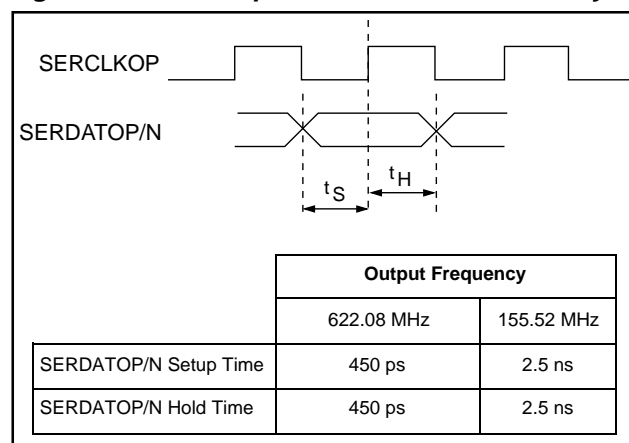


Figure 4. Input Jitter Tolerance Specification

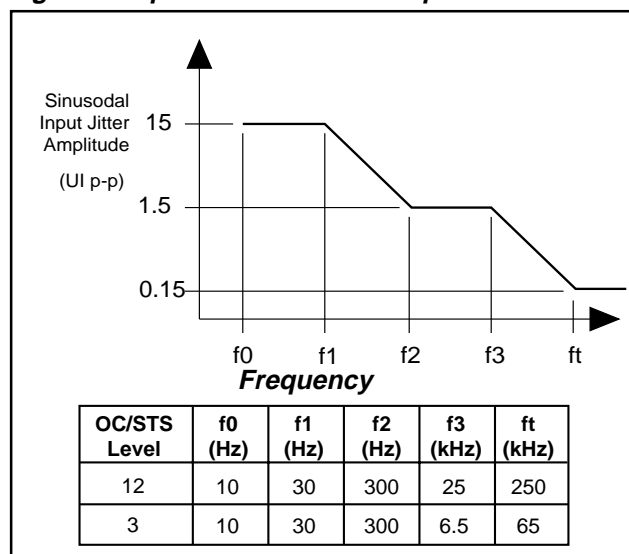
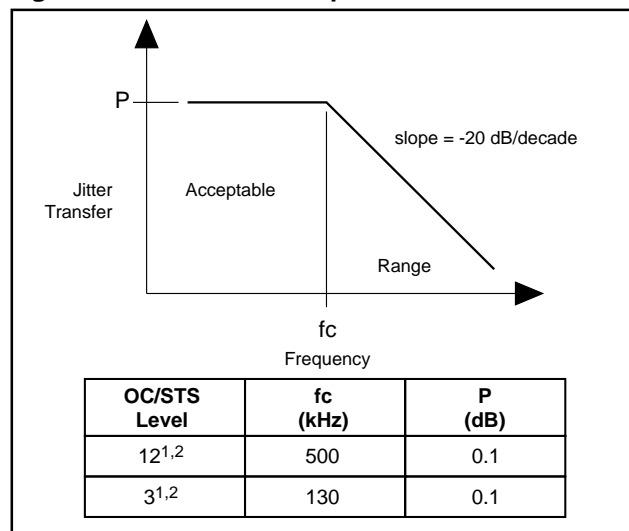


Figure 5. Jitter Transfer Specification



1. Bellcore Specifications: TR-NWT-000253, Issue 2, December 1991.
2. CCITT Recommendations: G.958.

Table 1. S3023 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
SERDATIP SERDATIN	Diff. LVPECL	I	2 3	Serial Data In. A clock is recovered from transitions on these inputs.
BYPASS	LVTTTL	I	16	Bypass enable. Active High. Used during production test to bypass the VCO in the PLL. Tie to ground for normal operation.
SDN	LVPECL	I	15	Signal Detect. Active Low. A single-ended LVPECL input to be driven by the external optical receiver module to indicate presence of received optical power. When SD is inactive, the PLL will be forced to lock to the TTLREF input and the SERDATOP/N output will be held in the logic low state. When SD is active, data on the SERDATIP/N pins will be processed normally.
TTLREF	LVTTTL	I	7	Reference clock input used to establish the initial operating frequency of the clock recovery PLL and also used as a standby clock in the absence of data or when LOCKDET is inactive.
CAP1 CAP2		I	18 17	Loop Filter Pins. The loop filter capacitor and resistors are connected to these pins. See Figure 8.
LCKREFN	LVTTTL	I	8	Lock to Reference. Active Low. When active, the serial clock output will be forced to lock to the TTLREF local reference input, and the SERDATOP/N output will be held at the logic low state. See Table 2.
MODE	LVTTTL	I	6	Rate select used to select the bit rate of the device. Set High to select 622.08 Mbit/s. Set Low to select 155.52 Mbit/s.
SERDATOP SERDATON	Diff. LVPECL	O	14 13	Serial Data Out signal that is the delayed version of the incoming data stream (SERDATI) updated on the falling edge of Serial Clock Out (SERCLKOP).
SERCLKOP SERCLKON	Diff. LVPECL	O	12 11	Serial Clock Out signal that is phase aligned with Serial Data Out (SERDATOP/N). (See Figure 3.)
LOCKDET	LVPECL	O	5	Lock Detect. Active High. When active, this output indicates that the PLL is locked to the serial data inputs and valid clock and data are present at the serial outputs. When inactive, it indicates that the PLL is locked to the local reference clock. The lock detect will go inactive under the following conditions: 1. If SDN is inactive. 2. If the VCO drifts away from the local reference clock by more than 1000 ppm. 3. If LCKREFN is active.
DGND	GND	—	9	Digital Ground (0V)
DVCC	+3.3V	—	10	Digital Power Supply (+3.3V)
AGND	GND	—	4, 19	Analog Ground (0V)
AVCC	+3.3V	—	1, 20	Analog Power Supply (+3.3V)

Figure 6. S3023 Pinout

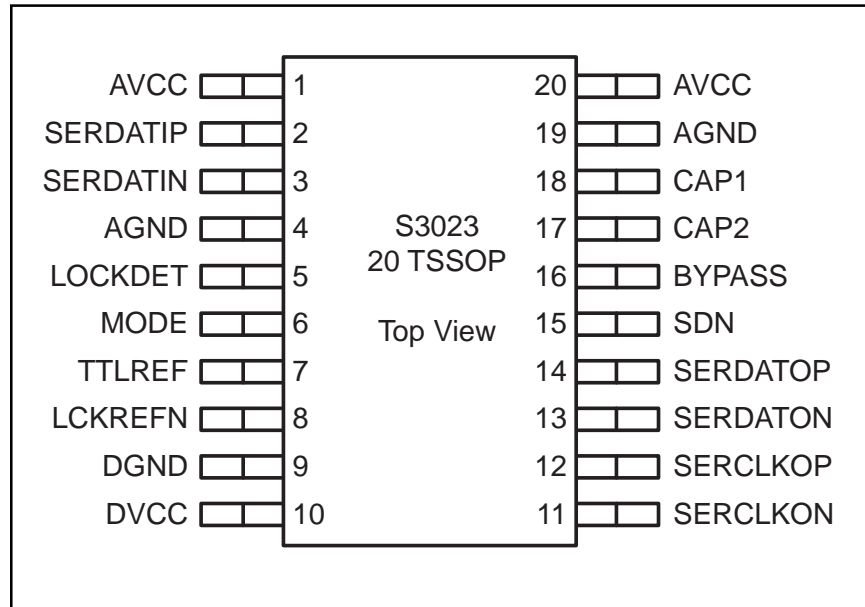


Figure 7. S3023 TSSOP Package

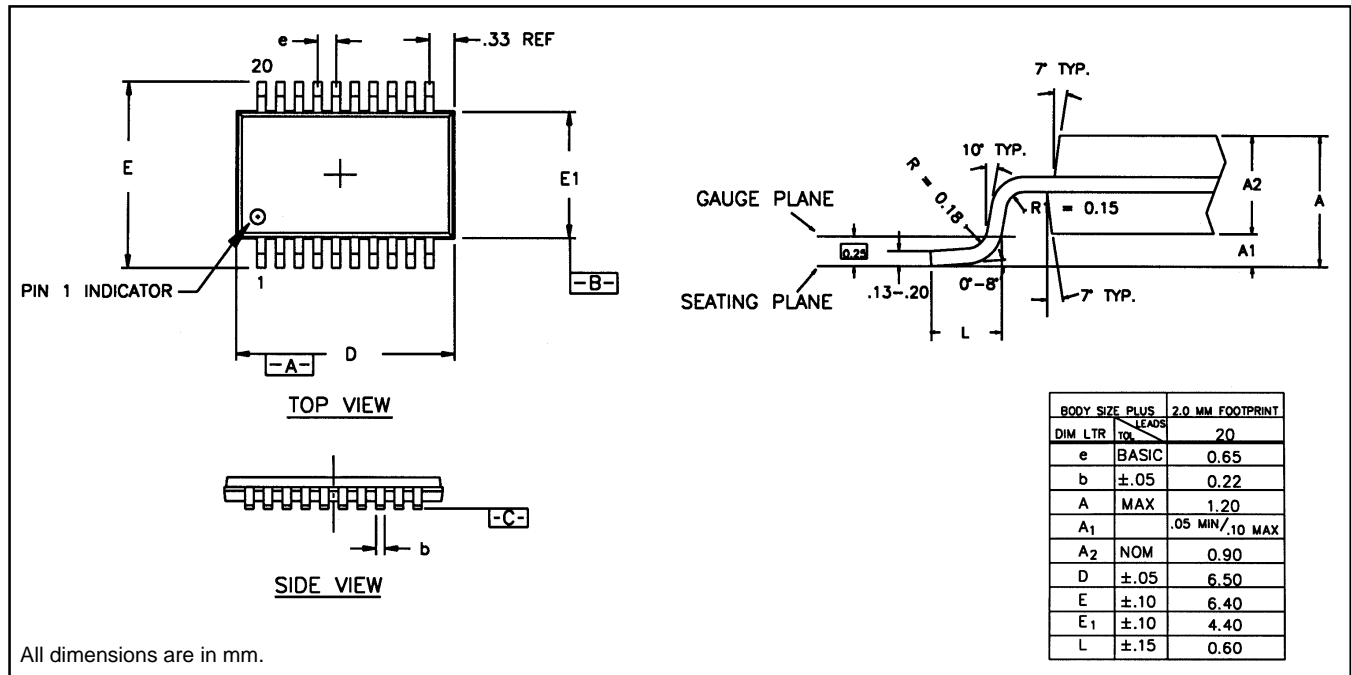


Table 2. Clock and Data Output Control

SDN	LCKREFN	LOCK DETECT	SERCLKOP/N	SERDATP/N
X	0	0	Active	0
1	X	0	Active	0
0	1	1	Active	Active

Table 3. Thermal Management

Device	Power	Θja Still Air
S3023	347 mW	77°C/W

Table 4. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
Storage Temperature	-65		+150	° C
Voltage on V_{CC} with Respect to GND	-0.5		+7.0	V
Voltage on any LVTTTL Input Pin	-0.5		V_{CC}	V
Voltage on any LVPECL Input Pin	V_{CC} -2.0		V_{CC}	V
LVTTTL Output Sink Current			20	mA
LVTTTL Output Source Current			10	mA
High Speed LVPECL Output Source Current			50	mA
ESD Sensitivity ¹	Under 500			V

1. Human Body Model.

Table 5. Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Ambient Temperature under Bias	-40		+85	° C
Voltage on V_{CC} with Respect to GND	3.13	3.3	3.46	V
Voltage on any LVTTTL Input Pin	0.0		V_{CC}	V
Voltage on any LVPECL Input Pin	V_{CC} -2		V_{CC}	V
PECL Output Source Current (50Ω to V_{CC} -2V)		14	25	mA
ICC Supply Current		80	100	mA

Table 6. Performance Specifications

Parameters	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		622.08		MHz	
Reference Clock Frequency Tolerance Clock Recovery ¹	-250		+250	ppm	
STS-3/STS-12 Capture Range		±500		ppm	With respect to fixed reference frequency
Clock Output Duty Cycle	45		55	% of UI	Minimum transition density of 20%.
Acquisition Lock Time ¹ STS-3/STS-12			16	μsec	With device already powered up and valid REFCLK.
PECL Output Rise & Fall Times			600	ps	10% to 90%, 50Ω to -2V equivalent load, 5 pF cap.
SERCLKOP/N Jitter Generation		0.005	0.01	UI	With less than 14ps rms jitter on SERDATIP/N data inputs.
STS-3/STS-12 Jitter Tolerance ¹	0.5			UI	Sinusoidal input jitter. Amplitude or SERDATIP/N data inputs from 250 kHz to 5 MHz for STS-12, 65 kHz to 1.3 MHz for STS-3.

1. Guaranteed but not tested.

Table 7. LVTTTL Input/Output DC Characteristics¹

(T_A = -40°C to +85°C, V_{CC} = 3.3 V ±5%)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V _{IL} ¹	Input LOW Voltage		0.8	V	Guaranteed Input LOW Voltage for all inputs
V _{IH} ¹	Input HIGH Voltage	2.0		V	Guaranteed Input HIGH Voltage for all inputs
I _{IL}	Input LOW Current	-400.0		μA	V _{CC} = MAX, V _{IN} = 0.5V
I _{IH}	Input HIGH Current		50.0	μA	V _{CC} = MAX, V _{IN} = 2.7V
I _I	Input HIGH Current at Max V _{IN}		1.0	mA	V _{CC} = MAX, V _{IN} = V _{CC}
V _{IK}	Input Clamp Diode Voltage	-1.2		V	V _{CC} = MIN, I _{IN} = -18.0mA

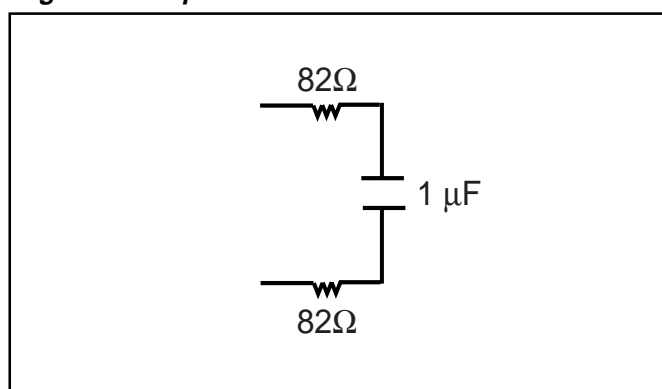
1. These input levels provide a zero-noise immunity and should only be tested in a static, noise-free environment.

Table 8. LVPECL Input/Output Characteristics

(T_A = -40°C to +85°C, V_{CC} = 3.3 V)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Input Low Voltage	V _{CC} -2.000		V _{CC} -1.441	V	Guaranteed Input Low Voltage for single-ended inputs
V _{IH}	Input High Voltage	V _{CC} -1.225		V _{CC} -0.570	V	Guaranteed Input High Voltage for single-ended inputs
V _{IL}	Input Low Voltage	V _{CC} -2.000		V _{CC} -0.700	V	Guaranteed Input Low Voltage for differential inputs
V _{IH}	Input High Voltage	V _{CC} -1.750		V _{CC} -0.450	V	Guaranteed Input High Voltage for differential inputs
V _{ID}	Input Differential Voltage	0.250	0.500	1.400	V	Differential Input Voltage
I _{IH}	Input High Current	-0.500		100	uA	V _{ID} = 500 mV
I _{IL}	Input Low Current	-0.60		20.000	uA	V _{ID} = 500 mV
V _{OL}	Output Low Voltage	V _{CC} -2.000		V _{CC} -1.57	V	50 Ω termination to V _{CC} -2V
V _{OH}	Output High Voltage	V _{CC} -1.35		V _{CC} -0.670	V	50 Ω termination to V _{CC} -2V
V _{OD}	Output Differential Voltage	0.390		1.330	V	Differential Output Voltage

Figure 8. Loop Filter Connections



Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	3023	A – 20 TSSOP

X
Prefix

XXXX
Device

X
Package



Applied Micro Circuits Corporation • 6290 Sequence Dr., San Diego, CA 92121

Phone: (858) 450-9333 • (800)755-2622 • Fax: (858) 450-9885

<http://www.amcc.com>

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