



A276308A

64K X 8 OTP CMOS EPROM

Document Title

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Revision History

| <u>Rev. No.</u> | <u>History</u> | <u>Issue Date</u> | <u>Remark</u> |
|------------------------|------------------------------------|--------------------------|----------------------|
| 0.0 | Initial issue | March 24, 2000 | Preliminary |
| 0.1 | Change Program Verify VCC to 6.25V | March 14, 2001 | |
| 1.0 | Final spec release | December 17, 2001 | |



A276308A

64K X 8 OTP CMOS EPROM

Features

- 65,536 X 8 bit organization
- Programming voltage: 12.75V
- Access time: 55/70/90 ns (max.)
- Current: Operating: 30mA (max.) at 5MHz
Standby: 100µA (max.)
- All inputs and outputs are directly TTL-compatible
- Available in 28-pin DIP and 32-PLCC packages

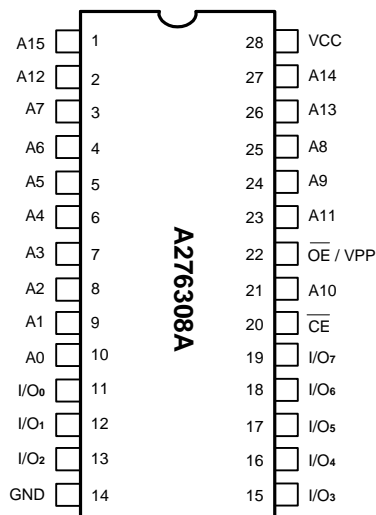
General Description

The A276308A chip is a high-performance 524,288 bit one-time programmable read only memory (OTP EPROM) organized as 64K by 8 bits. The A276308A requires only 5V power supply in normal read mode

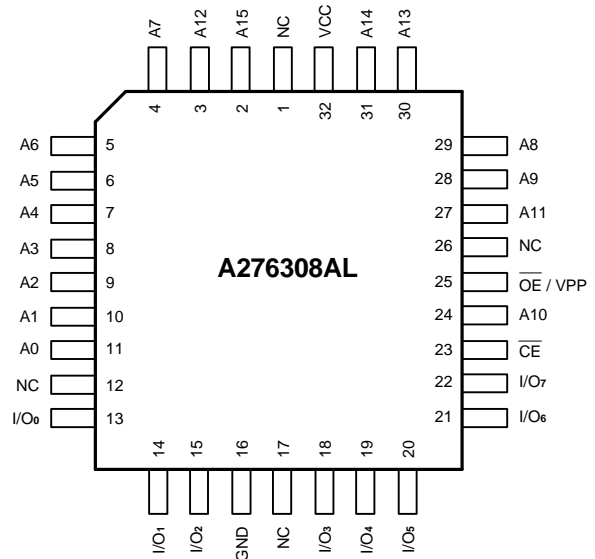
operation and any input signals are TTL levels. The A276308A is available in industry standard 28 pin dual-in-line and 32 lead PLCC packages.

Pin Configurations

■ DIP



■ PLCC



Pin Configurations

| Pin Name | Function |
|------------------------------|--------------------------------------|
| A0-A15 | Address Inputs |
| I/O7-I/O0 | Data Inputs / Outputs |
| $\overline{\text{CE}}$ | Chip Enable |
| $\overline{\text{OE}}$ / VPP | Output Enable / Program Power Supply |
| VCC | Power Supply |
| GND | Ground |
| NC | No Internal Connection |

Operating Modes and Truth Table

| Mode | $\overline{\text{CE}}$ | $\overline{\text{OE}}$ / VPP | A0 | A1 | A9 | VCC | I/O7-I/O0 |
|----------------------------------|------------------------|------------------------------|-----------------|-----------------|-----------------|-------|-----------|
| Read | V _{IL} | V _{IL} | X | X | X | VCC | Data Out |
| Output Disable | V _{IL} | V _{IH} | X | X | X | VCC | Hi-Z |
| Standby | V _{IH} | X | X | X | X | VCC | Hi-Z |
| Program | V _{IL} | 12.75V | X | X | X | 6.25V | Data In |
| Program Verify | V _{IL} | V _{IL} | X | X | X | 6.25V | Data Out |
| Program Inhibit | V _{IH} | 12.75V | X | X | X | 6.25V | Hi-Z |
| Manufacturer Code ⁽³⁾ | V _{IL} | V _{IL} | V _{IL} | V _{IL} | V _{ID} | VCC | 37H |
| Device Code ⁽³⁾ | V _{IL} | V _{IL} | V _{IH} | V _{IL} | V _{ID} | VCC | 2CH |
| Continuation Code ⁽³⁾ | V _{IL} | V _{IL} | V _{IL} | V _{IH} | V _{ID} | VCC | 7FH |

Notes:

1. X = Either V_{IH} or V_{IL}.
2. V_{ID} = 12V ± 0.5V.
3. A2 ~ A8 = A10 ~ A15 = V_{IL} (For auto identification)

Functional Description

Read Mode

The A276308A has two control functions, both of which must be logically active in order to obtain data at the outputs. \overline{CE} is the power control and should be used for device selection. \overline{OE} is the output control and should be used to data to the output pins, which is independent of device selection. Assuming that addresses are stable, address access time (t_{AA}) is equal to the delay from \overline{CE} to output (t_{CE}). Data is available at the output after a delay (t_{OE}) from the falling edge of \overline{OE} , as long as \overline{CE} has been low and the addresses have been stable for at least $t_{AA} - t_{OE}$.

Standby Mode

The A276308A has a standby mode which reduces the active current from 30mA to 100 μ A. The A276308A is placed in the standby mode by applying a CMOS high signal to \overline{CE} . When in the standby mode, the output are in a high impedance state, independent of the \overline{OE} .

Absolute Maximum Ratings*

Ambient Operating Temperature (T_A) -10°C to +85°C
 Storage Temperature Plastic Package (T_{STG})
 -55°C to 125°C
 Applied Input Voltage (V_i):
 All Pins Except A9, VPP and VCC
 -0.6V to VCC + 0.6V
 A9, VPP -0.6V to 13.5V
 VCC -0.6V to 7.0V
 Output Voltage (V_o) -0.6V to 7.0V (Note 1)

Notes:

1. During voltage transitions, the input may undershoot GND to -2.0V for periods less than 20 ns. Maximum DC voltage on input and I/O may overshoot to VCC + 2.0V for periods less than 20 ns.
2. When transitions, A9 and VPP may undershoot GND to -2.0V for periods less than 20 ns. Maximum DC input voltage on A9 and VPP is +13.5V which may overshoot to 14.0V for period less than 20 ns.

Auto Identify Mode

The auto identify mode allows the reading out of a binary code from a EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

To activate the mode, the programming equipment must apply 12.0V \pm 0.5V on address line A9 of the A276308A. Three identification code can be read from data output pin by toggling A0 and A1. The other addresses must be held at V_{IL} during this mode. Byte 0 (with A0 at V_{IL} , A1 at V_{IL}) represents the manufacturer code which is 37H. Byte 1 and Byte 2 represent the device code and continuation code, which is 2CH and 7FH respectively. All identifiers for these codes will possess odd parity, with MSB (IO7) defined the parity bit.

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Read Mode DC Electrical Characteristics ($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 10\%$, $V_{PP} = V_{CC}$)

| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|-----------|---------------------------------|------|----------------|---------------|---|
| V_{OH} | Output High Voltage | 2.4 | | V | $I_{OH} = -400\mu\text{A}$ |
| V_{OL} | Output Low Voltage | | 0.4 | V | $I_{OL} = 2.1\text{mA}$ |
| V_{IH} | Input High Voltage | 2.0 | $V_{CC} + 0.5$ | V | |
| V_{IL} | Input Low Voltage | -0.5 | 0.8 | V | |
| I_{LI} | Input Leakage Current | -1 | +1 | μA | $V_{CC} = \text{max.}$ $V_{in} = 0V$ to V_{CC} |
| I_{LO} | Output Leakage Current | -1 | +1 | μA | $V_{CC} = \text{max.}$ $V_{out} = 0V$ to V_{CC} |
| I_{CC} | V_{CC} Read Operating Current | | 30 | mA | $V_{CC} = \text{max.}$ $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$ $I_{out} = 0\text{mA}$, at 5MHz |
| I_{SB} | V_{CC} Standby Current (TTL) | | 1 | mA | $V_{CC} = \text{max.}$ $\overline{CE} = V_{IH}$ |
| I_{SB1} | V_{CC} Standby Current (CMOS) | | 100 | μA | $V_{CC} = \text{max.}$ $\overline{CE} = V_{CC} - 0.2V$ |
| I_{PP} | V_{PP} Current During Read | | 10 | μA | $\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$ |
| I_{ID} | A9 Auto Select Current | | 100 | μA | $A9 = V_{ID}$, $V_{CC} = \text{max.}$ |

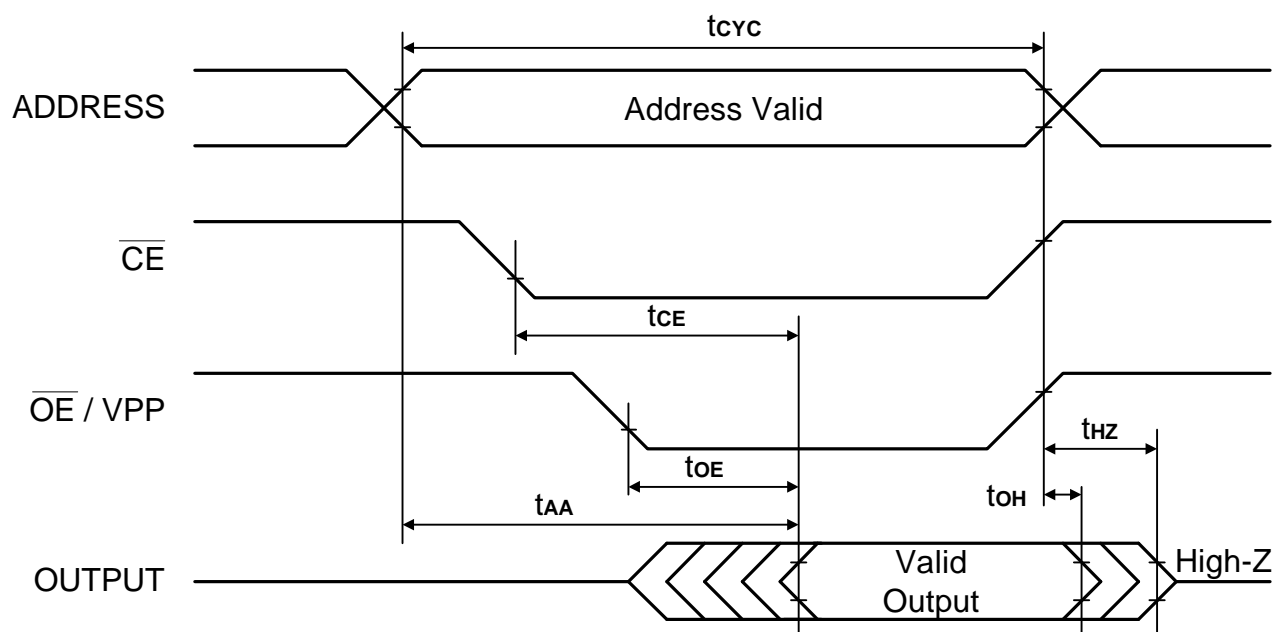
Capacitance ($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|-----------|--------------------|------|------|------|----------------|
| C_{IN} | Input Capacitance | | 8 | pF | $V_{IN} = 0V$ |
| C_{out} | Output Capacitance | | 8 | pF | $V_{out} = 0V$ |

* These parameters are sampled and not 100% tested.

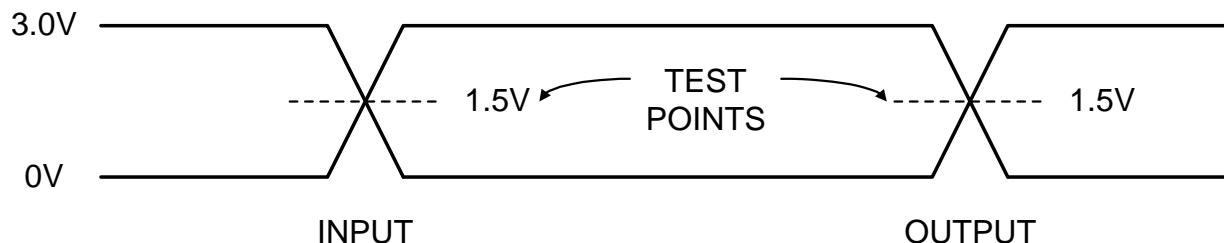
Read Mode AC Characteristics ($T_a = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 10\%$, $V_{PP} = V_{CC}$)

| Symbol | Parameter | 55ns | | 70ns | | 90ns | | Unit |
|-----------|--|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{cyc} | Cycle Time | 55 | | 70 | | 90 | | ns |
| t_{AA} | Address Access Time | | 55 | | 70 | | 90 | ns |
| t_{CE} | Chip Enable Access Time | | 55 | | 70 | | 90 | ns |
| t_{OE} | Output Enable Access Time | | 30 | | 35 | | 40 | ns |
| t_{OH} | Output Hold after Address, \overline{CE} or \overline{OE} , whichever Occurred First | 0 | | 0 | | 0 | | ns |
| t_{HZ} | Output High Z Delay | | 20 | | 20 | | 25 | ns |

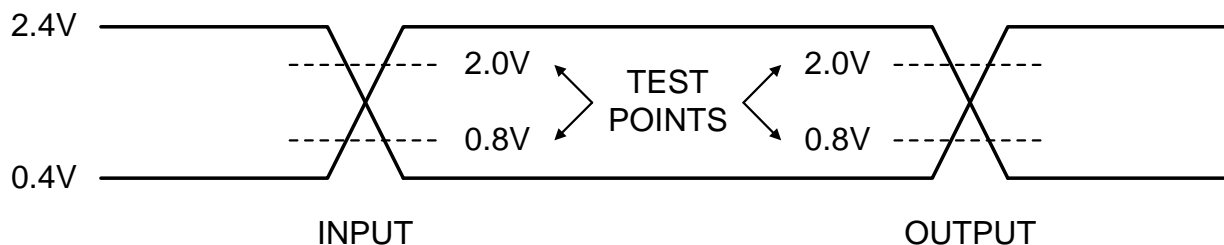
Read Mode Switching Waveforms


AC Measurement Conditions

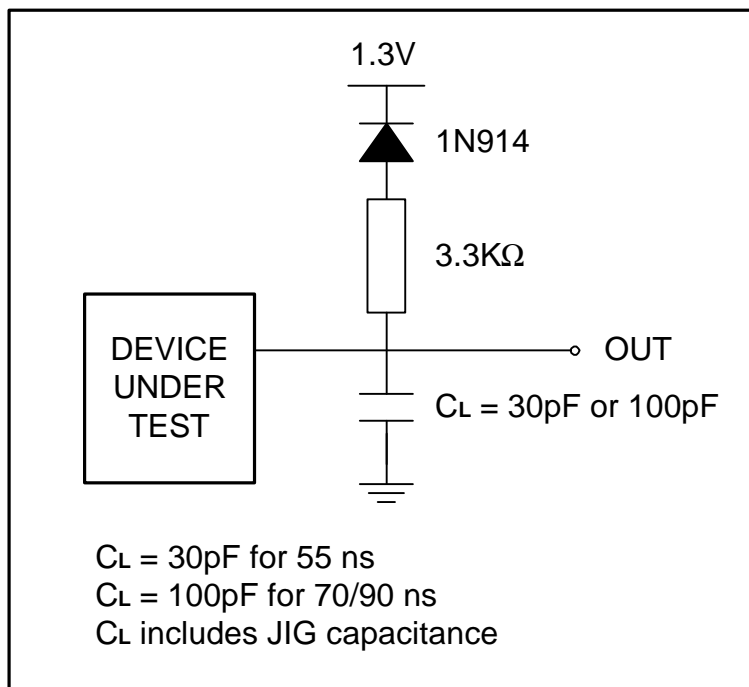
- for 55 ns
- ① Input Rise and Fall Times ≤ 10 ns
 - ② Input Pulse Voltage: 0V to 3V
 - ③ Input and Output Timing Ref. Voltage: 1.5V



- for 70/90 ns
- ① Input Rise and Fall Times ≤ 10 ns
 - ② Input Pulse Voltage: 0.4V to 2.4V
 - ③ Input and Output Timing Ref. Voltage: 0.8V to 2.0V



AC Testing Load Circuit



Programming and Program Verify

The programming flowchart is shown in Page 10.

The A276308A is shipped with all bits being set to "1". Programming causes relevant bits to be changed to "0". The programming mode is started by setting VCC to 6.25V, \overline{OE}/VPP to +12.75V and \overline{CE} is at V_{IL} . Data to be programmed can be directly input in the 8 bit format through the data bus.

The write programming algorithm reduces programming time by using 100 μ s pulse followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not pass the verification,

an additional pulse programming is applied for a maximum of 25 pulses. On completion of 1 byte programming and, The verified address is incremented. After the final address is completed, all bytes are verified again with VCC = 5.0 Volt.

Program Inhibit

This mode is used to program one of multiple A276308A whose VCC, address bus and data bus are connected in parallel. When programming is performed, other A276308A can be inhibited from being programmed by setting their \overline{CE} pins to V_{IH} and \overline{OE}/VPP pins to +12.75V.

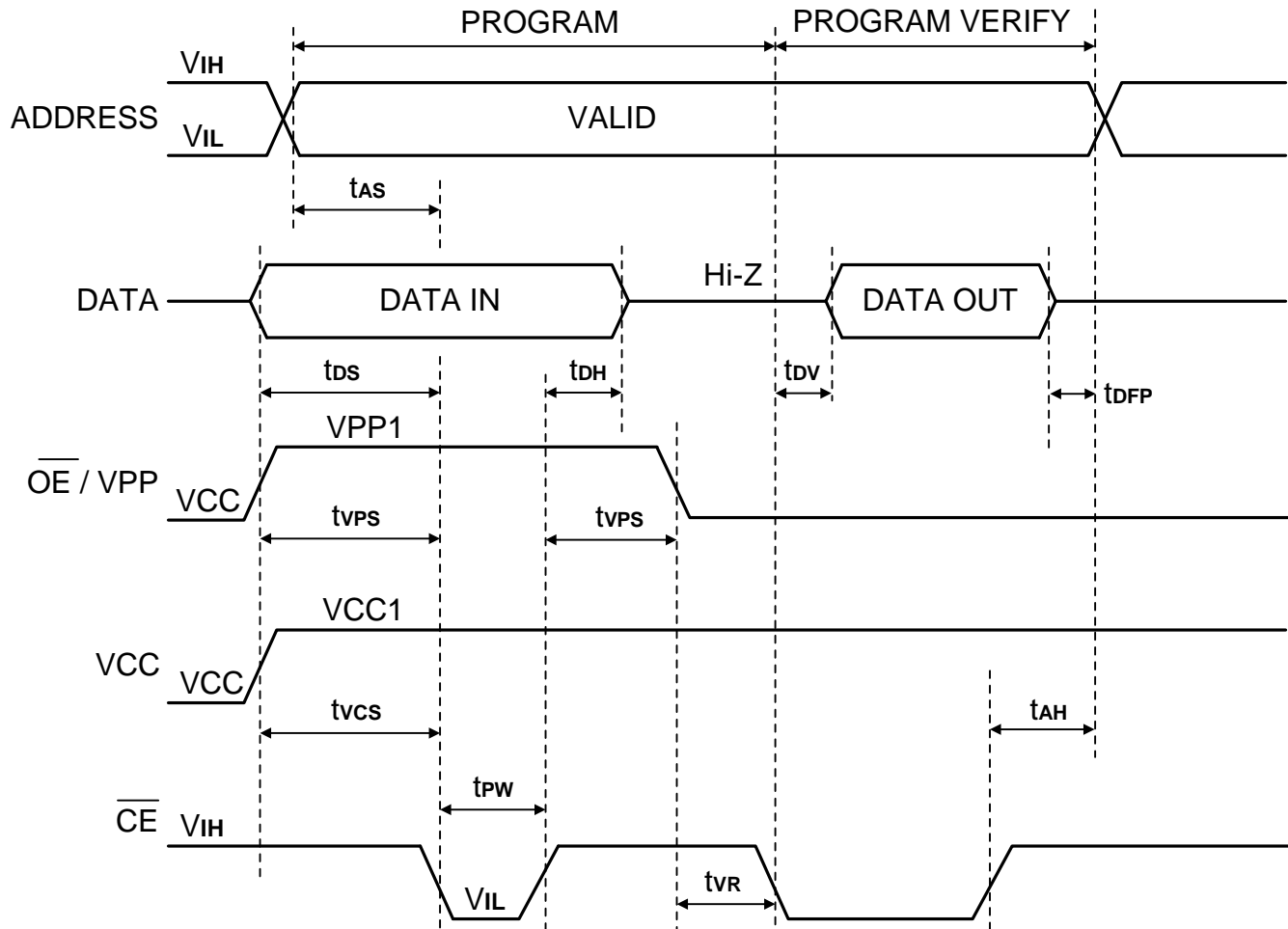
Programming Mode DC Characteristics (Ta = 0°C to 70°C, VCC = 6.25V \pm 0.25V, VPP = 12.75V \pm 0.25V)

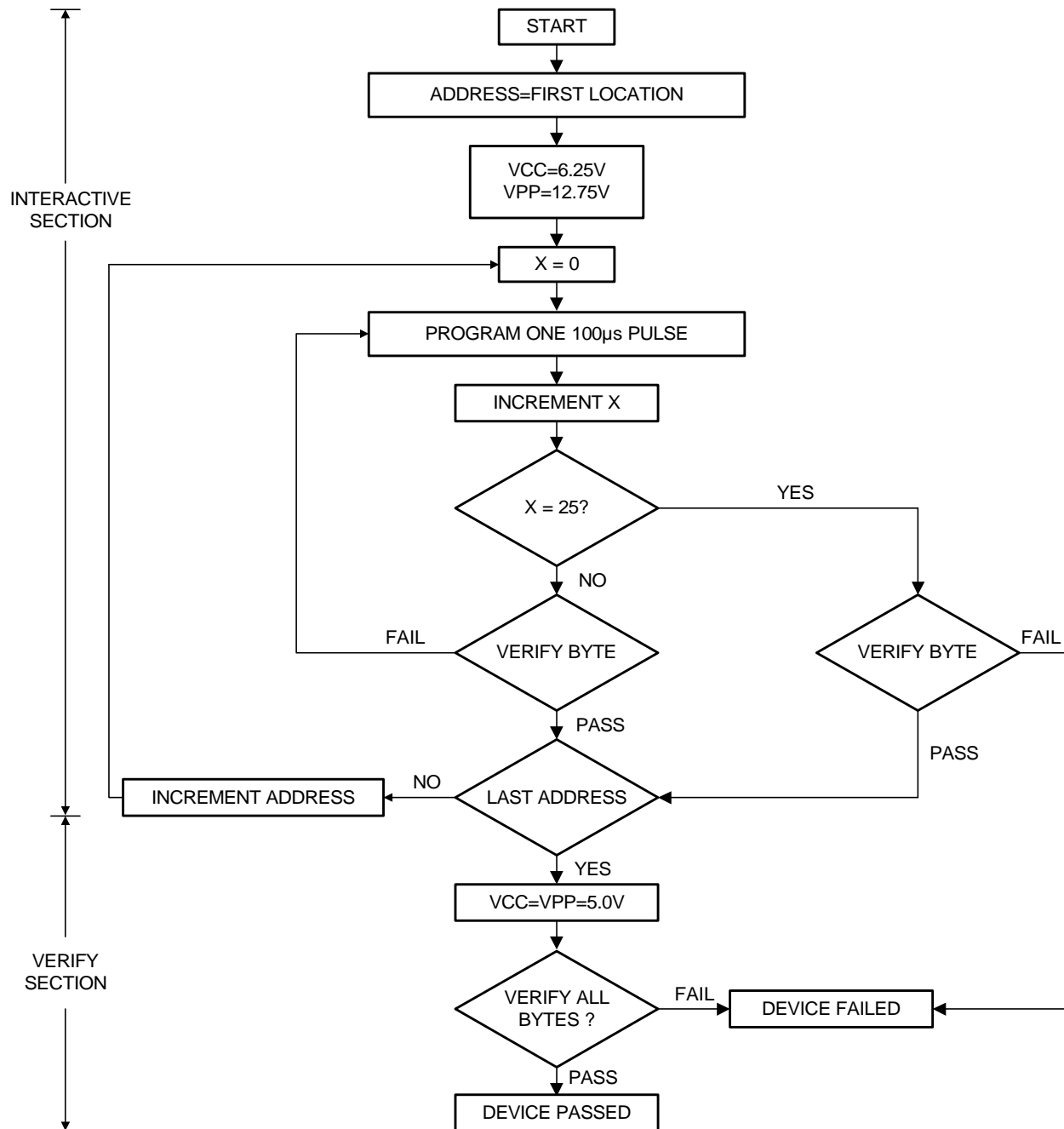
| Symbol | Parameter | Min. | Max. | Unit | Test Conditions |
|----------|----------------------------|------|-----------|---------|----------------------------|
| V_{OH} | Output High Voltage | 2.4 | | V | $I_{OH} = -400\mu A$ |
| V_{OL} | Output Low Voltage | | 0.4 | V | $I_{OL} = 2.1mA$ |
| V_{IH} | Input High Voltage | 2.0 | VCC + 0.5 | V | |
| V_{IL} | Input Low Voltage | -0.5 | 0.8 | V | |
| I_{LI} | Input Leakage Current | -1 | +1 | μA | VCC = max. Vin = 0V to VCC |
| I_{CC} | VCC Current During Program | | 50 | mA | |
| I_{PP} | VPP Current During Program | | 50 | mA | $\overline{CE} = V_{IL}$ |
| V_{ID} | A9 Auto Select Voltage | 11.5 | 12.5 | V | A9 = V_{ID} |
| VCC1 | Programming Supply Voltage | 6.0 | 6.5 | V | |
| VPP1 | Programming Voltage | 12.5 | 13 | V | |

Note: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.

Programming Mode AC Characteristics ($T_a = 0^{\circ}\text{C}$ to 70°C , $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$)

| Symbol | Parameter | Min. | Max. | Unit |
|-----------|-------------------------------------|------|------|---------------|
| t_{AS} | Address Valid to Program Low | 2 | | μs |
| t_{DS} | Input Valid to Program Low | 2 | | μs |
| t_{VPS} | VPP Set up Time | 2 | | μs |
| t_{VCS} | VCC Set up Time | 2 | | μs |
| t_{PW} | Program Pulse Width | 95 | 105 | μs |
| t_{DH} | Data Hold Time | 2 | | μs |
| t_{VR} | \overline{OE} / VPP Recovery Time | 2 | | μs |
| t_{DV} | Data Valid from \overline{CE} | | 100 | ns |
| t_{DFP} | Chip Enable to Output Float Delay | | 130 | ns |
| t_{AH} | Address Hold Time | 0 | | ns |

Programming and Verify Mode AC Waveforms


Programming Flowchart


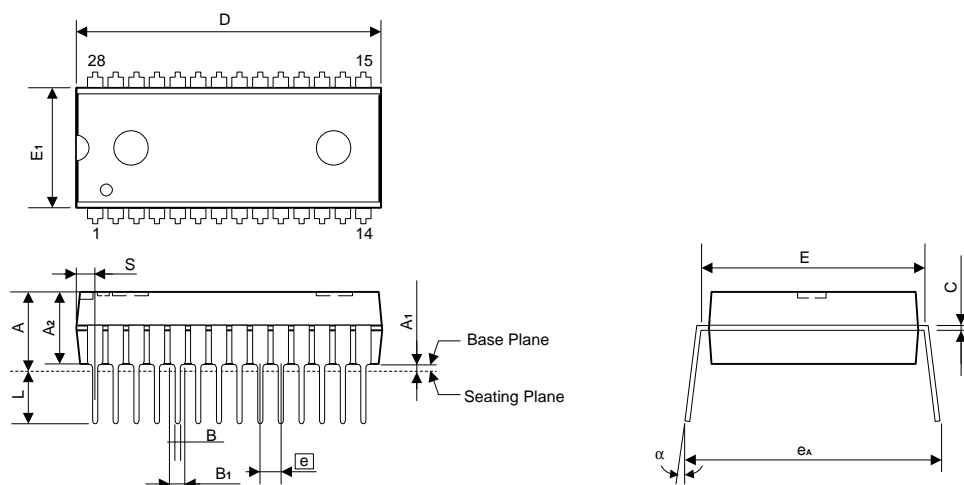
Ordering Information

| Part No. | Access Time (ns) | Operating Current Max. (mA) at 5MHz | Standby Current Max. (μA) | Package |
|-----------------|-------------------------|--|--------------------------------------|----------------|
| A276308A-55 | 55 | 30 | 100 | 28Pin DIP |
| A276308AL-55 | 55 | 30 | 100 | 32Pin PLCC |
| A276308A-70 | 70 | 30 | 100 | 28Pin DIP |
| A276308AL-70 | 70 | 30 | 100 | 32Pin PLCC |
| A276308A-90 | 90 | 30 | 100 | 28Pin DIP |
| A276308AL-90 | 90 | 30 | 100 | 32Pin PLCC |

Package Information

P-DIP 28L Outline Dimensions

unit: inches/mm



| Symbol | Dimensions in inches | | | Dimensions in mm | | |
|--------|----------------------|-------|-------|------------------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | - | - | 0.210 | - | - | 5.33 |
| A1 | 0.010 | - | - | 0.25 | - | - |
| A2 | 0.150 | 0.155 | 0.160 | 3.81 | 3.94 | 4.06 |
| B | 0.016 | 0.018 | 0.022 | 0.41 | 0.46 | 0.56 |
| B1 | 0.058 | 0.060 | 0.064 | 1.47 | 1.52 | 1.63 |
| C | 0.008 | 0.010 | 0.014 | 0.20 | 0.25 | 0.36 |
| D | - | 1.460 | 1.470 | - | 37.08 | 37.34 |
| E | 0.590 | 0.600 | 0.610 | 14.99 | 15.24 | 15.49 |
| E1 | 0.540 | 0.545 | 0.550 | 13.72 | 13.84 | 13.97 |
| e | 0.090 | 0.100 | 0.110 | 2.29 | 2.54 | 2.79 |
| L | 0.120 | 0.130 | 0.140 | 3.05 | 3.30 | 3.56 |
| α | 0° | - | 15° | 0° | - | 15° |
| eA | 0.630 | 0.650 | 0.670 | 16.00 | 16.51 | 17.02 |
| S | - | - | 0.090 | - | - | 2.29 |

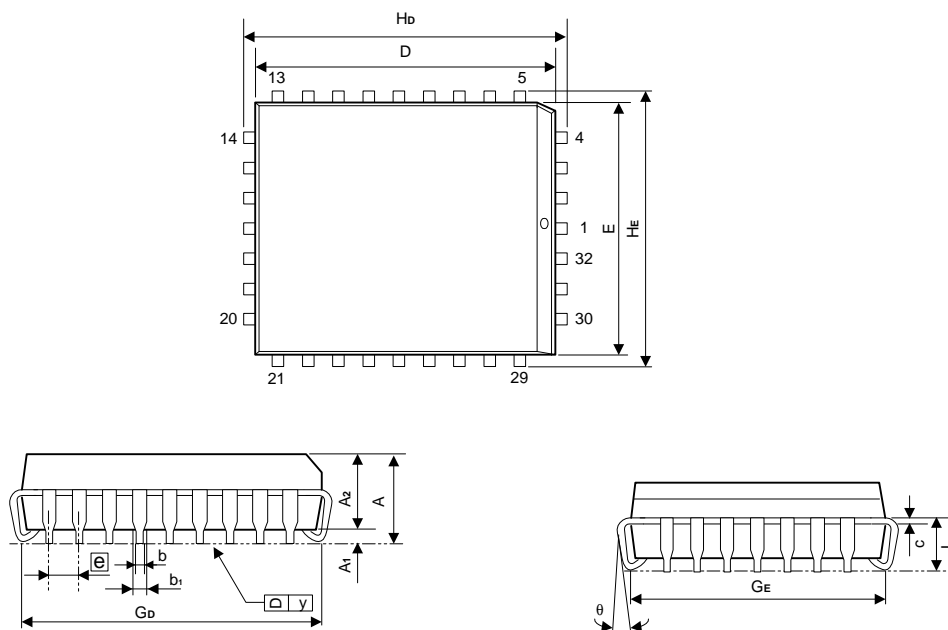
Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E1 does not include resin fins.
3. Dimension S includes end flash.

Package Information

PLCC 32L Outline Dimension

unit: inches/mm



| Symbol | Dimensions in inches | | | Dimensions in mm | | |
|----------------|----------------------|-------|-------|------------------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | - | - | 0.134 | - | - | 3.40 |
| A ₁ | 0.0185 | - | - | 0.47 | - | - |
| A ₂ | 0.105 | 0.110 | 0.115 | 2.67 | 2.80 | 2.93 |
| b ₁ | 0.026 | 0.028 | 0.032 | 0.66 | 0.71 | 0.81 |
| b | 0.016 | 0.018 | 0.021 | 0.41 | 0.46 | 0.54 |
| C | 0.008 | 0.010 | 0.014 | 0.20 | 0.254 | 0.35 |
| D | 0.547 | 0.550 | 0.553 | 13.89 | 13.97 | 14.05 |
| E | 0.447 | 0.450 | 0.453 | 11.35 | 11.43 | 11.51 |
| e | 0.044 | 0.050 | 0.056 | 1.12 | 1.27 | 1.42 |
| G _D | 0.490 | 0.510 | 0.530 | 12.45 | 12.95 | 13.46 |
| G _E | 0.390 | 0.410 | 0.430 | 9.91 | 10.41 | 10.92 |
| H _D | 0.585 | 0.590 | 0.595 | 14.86 | 14.99 | 15.11 |
| H _E | 0.485 | 0.490 | 0.495 | 12.32 | 12.45 | 12.57 |
| L | 0.075 | 0.090 | 0.095 | 1.91 | 2.29 | 2.41 |
| y | - | - | 0.003 | - | - | 0.075 |
| θ | 0° | - | 10° | 0° | - | 10° |

Notes:

- Dimensions D and E do not include resin fins.
- Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.