



## **A42U0616 Series**

***Preliminary***

***1M X 16 CMOS DYNAMIC RAM WITH EDO PAGE MODE***

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### **Document Title**

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### **Revision History**

<b><u>Rev. No.</u></b>	<b><u>History</u></b>	<b><u>Issue Date</u></b>	<b><u>Remark</u></b>
0.0	Initial issue	June 13, 2001	Preliminary



# A42U0616 Series

**Preliminary**

## 1M X 16 CMOS DYNAMIC RAM WITH EDO PAGE MODE

### Features

- Organization: 1,048,576 words X 16 bits
- Part Identification
  - A42U0616 (1K Ref.)
- Single 2.5V power supply/built-in VBB generator
- Low power consumption
  - Operating: 120mA (-50 max)
  - Standby: 1mA (TTL), 0.2mA (CMOS), 250μA (Self-refresh current)
- High speed
  - 50/60/80 ns  $\overline{\text{RAS}}$  access time
  - 25/30/40 ns column address access time

- 13/15/20 ns  $\overline{\text{CAS}}$  access time
- 20/25/35 ns EDO Page Mode Cycle Time
- Separate  $\overline{\text{CAS}}$  ( $\overline{\text{UCAS}}$ ,  $\overline{\text{LCAS}}$ ) for byte selection
- Fast Page Mode with Extended Data Out
- Read-modify-write,  $\overline{\text{RAS}}$  -only,  $\overline{\text{CAS}}$  -before-  $\overline{\text{RAS}}$ , Hidden refresh capability
- TTL-compatible, three-state I/O
- JEDEC standard packages
  - 400mil, 42-pin SOJ
  - 400mil, 50/44 TSOP type II package

### General Description

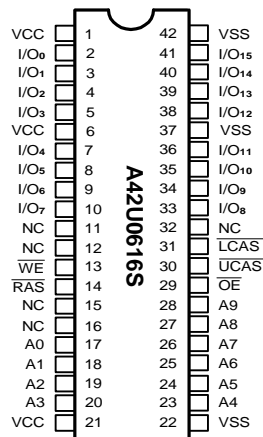
The A42U0616 is a new generation randomly accessed memory for graphics, organized in a 1,048,576 -word by 16-bit configuration. This product can execute Write and Read operation via  $\overline{\text{CAS}}$  pin.

The A42U0616 offers an accelerated Fast Page Mode cycle with a feature called Extended Data Out (EDO).

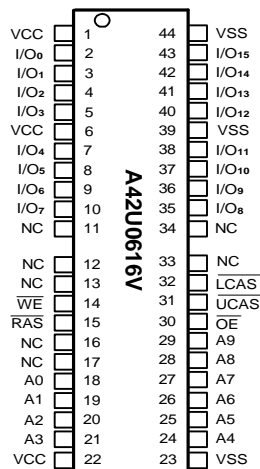
This allow random access of up to 1024(1K Ref.) words within a row at a 50/40/28 MHz EDO cycle, making the A42U0616 ideally suited for graphics, digital signal processing and high performance computing systems.

### Pin Configuration

#### ■ SOJ



#### ■ TSOP



### Pin Descriptions

Symbol	Description
A0 - A9	Address Inputs (1K product)
I/O <sub>0</sub> - I/O <sub>15</sub>	Data Input/Output
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{LCAS}}$	Column Address Strobe for Lower Byte (I/O <sub>0</sub> – I/O <sub>7</sub> )
$\overline{\text{UCAS}}$	Column Address Strobe for Upper Byte (I/O <sub>8</sub> – I/O <sub>15</sub> )
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
VCC	2.5V Power Supply
VSS	Ground
NC	No Connection

## Selection Guide

Symbol	Description	-50	-60	-80	Unit
t <sub>RAC</sub>	Maximum $\overline{\text{RAS}}$ Access Time	50	60	80	ns
t <sub>AA</sub>	Maximum Column Address Access Time	25	30	40	ns
t <sub>CAC</sub>	Maximum $\overline{\text{CAS}}$ Access Time	13	15	20	ns
t <sub>OE</sub>	Maximum Output Enable ( $\overline{\text{OE}}$ ) Access Time	13	15	20	ns
t <sub>RC</sub>	Minimum Read or Write Cycle Time	84	104	134	ns
t <sub>PC</sub>	Minimum EDO Cycle Time	20	25	35	ns

## Functional Description

The A42U0616 reads and writes data by multiplexing an 20-bit address into a 10-bit row and 10-bit column address.  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are used to strobe the row address and the column address, respectively.

The A42U0616 has two  $\overline{\text{CAS}}$  inputs:  $\overline{\text{LCAS}}$  controls I/O<sub>0</sub>-I/O<sub>7</sub>, and  $\overline{\text{UCAS}}$  controls I/O<sub>8</sub> - I/O<sub>15</sub>.  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  function in an identical manner to  $\overline{\text{CAS}}$  in that either will generate an internal  $\overline{\text{CAS}}$  signal. The  $\overline{\text{CAS}}$  function and timing are determined by the first  $\overline{\text{CAS}}$  ( $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ ) to transition low and by the last to transition high. Byte Read and Byte Write are controlled by using  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  separately.

A Read cycle is performed by holding the  $\overline{\text{WE}}$  signal high during  $\overline{\text{RAS}}/\overline{\text{CAS}}$  operation. A Write cycle is executed by holding the  $\overline{\text{WE}}$  signal low during  $\overline{\text{RAS}}/\overline{\text{CAS}}$  operation; the input data is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs later. The data inputs and outputs are routed through 16 common I/O pins, with  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$  and  $\overline{\text{OE}}$  controlling the in direction.

EDO Page Mode operation all 1024(1K) columns within a selected row to be randomly accessed at a high data rate. A EDO Page Mode cycle is initiated with a row address latched by  $\overline{\text{RAS}}$  followed by a column address latched by  $\overline{\text{CAS}}$ . While holding  $\overline{\text{RAS}}$  low,  $\overline{\text{CAS}}$  can be toggled to strobe changing column addresses, thus achieving shorter cycle times.

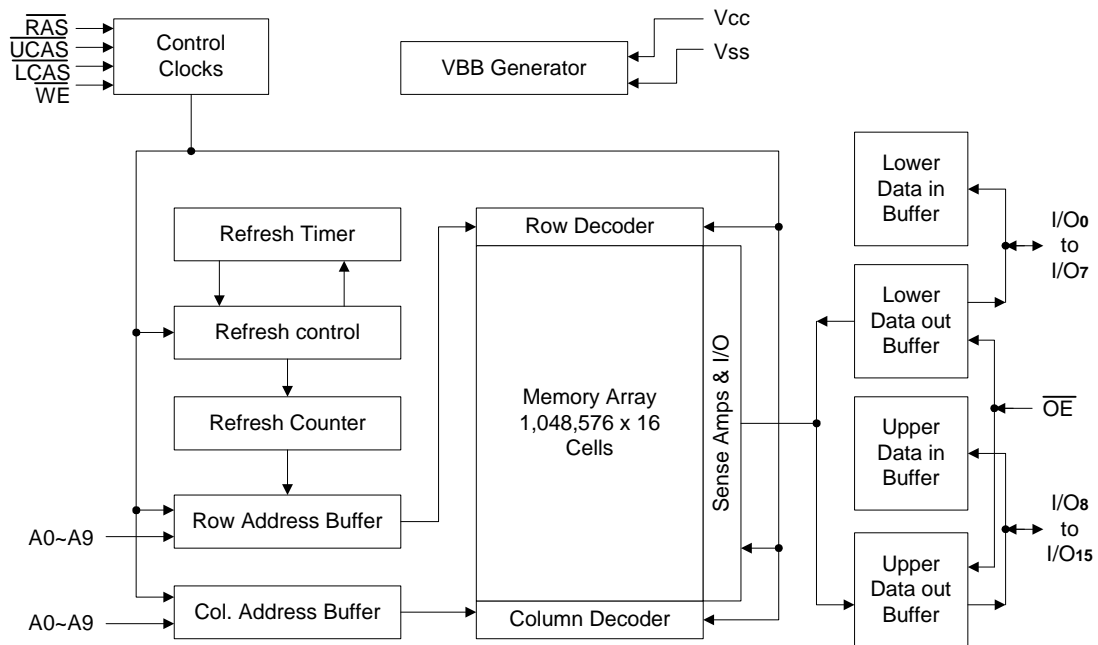
The A42U0616 offers an accelerated Fast Page Mode cycle through a feature called Extended Data Out, which

keeps the output drivers on during the  $\overline{\text{CAS}}$  precharge time (t<sub>cp</sub>). Since data can be output after  $\overline{\text{CAS}}$  goes high, the user is not required to wait for valid data to appear before starting the next access cycle. Data-out will remain valid as long as  $\overline{\text{RAS}}$  and  $\overline{\text{OE}}$  are low, and  $\overline{\text{WE}}$  is high; this is the only characteristic which differentiates Extended Data Out operation from a standard Read or Fast Page Read.

A memory cycle is terminated by returning both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  high. Memory cell data will retain its correct state by maintaining power and accessing all 1024(1K) combinations of the 10-bit row addresses, regardless of sequence, at least once every 16ms through any  $\overline{\text{RAS}}$  cycle (Read, Write) or  $\overline{\text{RAS}}$  Refresh cycle ( $\overline{\text{RAS}}$ -only, CBR, or Hidden). The CBR Refresh cycle automatically controls the row addresses by invoking the refresh counter and controller.

## Power-On

The initial application of the VCC supply requires a 200  $\mu\text{s}$  wait followed by a minimum of any eight initialization cycles containing a  $\overline{\text{RAS}}$  clock. During Power-On, the VCC current is dependent on the input levels of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ . It is recommended that  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  track with VCC or be held at a valid V<sub>ih</sub> during Power-On to avoid current surges.

**Block Diagram**

**Recommended Operating Conditions** (Ta = 0°C to +70°C)

Symbol	Description	Min.	Typ.	Max.	Unit
VCC	Power Supply	2.25	2.5	2.75	V
VSS	Input High Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage	1.8	-	VCC + 0.2	V
V <sub>IL</sub>	Input Low Voltage	-1.0	-	0.8	V

**Truth Table**

Function	RAS	UCAS	LCAS	WE	OE	Address	I/Os	Notes
Standby	H	X	X	X	X	X	High-Z	
Read: Word	L	L	L	H	L	Row/Col.	Data Out	
Read: Lower Byte	L	H	L	H	L	Row/Col.	I/O <sub>0-7</sub> = Data Out I/O <sub>8-15</sub> = High-Z	
Read: Upper Byte	L	L	H	H	L	Row/Col.	I/O <sub>0-7</sub> = High-Z I/O <sub>8-15</sub> = Data Out	
Write: Word	L	L	L	L	H	Row/Col.	Data In	
Write: Lower Byte	L	H	L	L	H	Row/Col.	I/O <sub>0-7</sub> = Data In I/O <sub>8-15</sub> = X	
Write: Upper Byte	L	L	H	L	H	Row/Col.	I/O <sub>0-7</sub> = X I/O <sub>8-15</sub> = Data In	
Read-Write	L	L	L	H→L	L→H	Row/Col.	Data Out → Data In	1,2
EDO-Page-Mode Read: Hi-Z								
-First cycle	L	H→L	H→L	H	H→L	Row/Col.	Data Out	2
-Subsequent Cycles	L	H→L	H→L	H	H→L	Col.	Data Out	2
EDO-Page-Mode Write								
-First cycle	L	H→L	H→L	L	H	Row/Col.	Data In	1
-Subsequent Cycles	L	H→L	H→L	L	H	Col.	Data In	1
EDO-Page-Mode Read-Write								
-First cycle	L	H→L	H→L	H→L	L→H	Row/Col.	Data Out → Data In	1, 2
-Subsequent Cycles	L	H→L	H→L	H→L	L→H	Col.	Data Out → Data In	1, 2
Hidden Refresh Read	L→H→L	L	L	H	L	Row/Col.	Data Out	2
Hidden Refresh Write	L→H→L	L	L	L	X	Row/Col.	Data In → High-Z	1
RAS-Only Refresh	L	H	H	X	X	Row	High-Z	
CBR Refresh	H→L	L	L	X	X	X	High-Z	3
Self Refresh	H→L	L	L	H	X	X	High-Z	

Note: 1. Byte Write may be executed with either UCAS or LCAS active.  
2. Byte Read may be executed with either UCAS or LCAS active.  
3. Only one CAS signal (UCAS or LCAS) must be active.

**Absolute Maximum Ratings\***

Input Voltage (Vin) . . . . . -0.5V to VCC+0.5V  
 Output Voltage (Vout) . . . . . -0.5V to VCC+0.5V  
 Power Supply Voltage (VCC) . . . . . -0.5V to VCC+0.5V  
 Operating Temperature (TOPR) . . . . . 0°C to +70°C  
 Storage Temperature (TSTG) . . . . . -55°C to +150°C  
 Soldering Temperature X Time (TSOLDER) . . . . .  
 . . . . . 260°C X 10sec  
 Power Dissipation (PD) . . . . . 1W  
 Short Circuit Output Current (Iout) . . . . . 50mA  
 Latch-up Current . . . . . 200mA

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of these specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics** (VCC = 2.5V ± 10%, VSS = 0V, Ta = 0°C to +70°C)

Symbol	Parameter	-50		-60		-80		Unit	Test Conditions	Notes
		Min.	Max.	Min.	Max.	Min.	Max.			
IIL	Input Leakage Current	-5	+5	-5	+5	-5	+5	μA	0V ≤ Vin ≤ Vin + 0.2V Pins not under Test = 0V	
IoL	Output Leakage Current	-5	+5	-5	+5	-5	+5	μA	DOUt disabled, 0V ≤ Vout ≤ + VCC	
Icc1	Operating Power Supply Current	-	120	-	110	-	100	mA	$\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}}$ Address cycling; tRC = min.	1, 2
Icc2	TTL Standby Power Supply Current	-	1	-	1	-	1	mA	$\overline{\text{RAS}} = \overline{\text{UCAS}} = \overline{\text{LCAS}} = V_{IH}$	
Icc3	Average Power Supply Current, RAS Refresh Mode	-	120	-	110	-	100	mA	$\overline{\text{RAS}}$ cycling, $\overline{\text{UCAS}} = \overline{\text{LCAS}} = V_{IH}$ , tRC = min.	1
Icc4	EDO Page Mode Average Power Supply Current	-	100	-	90	-	80	mA	$\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{UCAS}}, \overline{\text{LCAS}}$ Address cycling; tPC = min.	1, 2
Icc5	$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Power Supply Current	-	110	-	100	-	90	mA	$\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}}$ cycling; tRC = min.	1
Icc6	CMOS Standby Power Supply Current	-	0.2	-	0.2	-	0.2	mA	$\overline{\text{RAS}} = \overline{\text{UCAS}} = \overline{\text{LCAS}} = V_{CC} - 0.2V$	
Icc7	Self Refresh Mode Current	-	250	-	250	-	250	μA	$\overline{\text{RAS}} = \overline{\text{CAS}} \leq V_{SS} + 0.2V$ All other input high levels are VCC-0.2V or input low levels are VSS +0.2V	
VoH	Output Voltage	2.0	-	2.0	-	2.0	-	V	Iout = -2mA	
VoL		-	0.4	-	0.4	-	0.4	V	Iout = 2mA	

**AC Characteristics** ( $V_{CC} = 2.5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0^\circ C$  to  $+70^\circ C$ )

Test Conditions:

Input timing reference level:  $V_{IH}/V_{IL}=1.8V/0.8V$ 

Output reference level:  $V_{OH}/V_{OL}=1.6V/0.8V$ 

Output Load: 1TTL gate + CL (100pF)

Assumed  $t_r=2ns$ 

#	Std Symbol	Parameter	-50		-60		-80		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
	$t_r$	Transition Time (Rise and Fall)	1	50	1	50	1	50	ns	4, 5
	$t_{REF}$	Refresh Period	-	16	-	16	-	16	ms	3
1	$t_{RC}$	Random Read or Write Cycle Time	84	-	104	-	134	-	ns	
2	$t_{RP}$	$\overline{RAS}$ Precharge Time	30	-	40	-	50	-	ns	
3	$t_{RAS}$	$\overline{RAS}$ Pulse Width	50	10K	60	10K	80	10K	ns	
4	$t_{CAS}$	$\overline{CAS}$ Pulse Width	7	10K	10	10K	15	10K	ns	
5	$t_{RCD}$	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11	37	14	45	20	60	ns	6
6	$t_{RAD}$	$\overline{RAS}$ to Column Address Delay Time	9	25	12	30	15	40	ns	7
7	$t_{RSH}$	$\overline{CAS}$ to $\overline{RAS}$ Hold Time	7	-	10	-	10	-	ns	
8	$t_{CSH}$	$\overline{CAS}$ Hold Time	37	-	40	-	50	-	ns	
9	$t_{CRP}$	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
10	$t_{ASR}$	Row Address Setup Time	0	-	0	-	0	-	ns	
11	$t_{RAH}$	Row Address Hold Time	7	-	10	-	10	-	ns	
12	$t_{CLZ}$	$\overline{CAS}$ to Output in Low Z	0	-	0	-	0	-	ns	8
13	$t_{RAC}$	Access Time from $\overline{RAS}$	-	50	-	60	-	80	ns	6,7
14	$t_{CAC}$	Access Time from $\overline{CAS}$	-	13	-	15	-	20	ns	6, 12
15	$t_{AA}$	Access Time from Column Address	-	25	-	30	-	40	ns	7, 12
16	$t_{AR}$	Column Address Hold Time from $\overline{RAS}$	44	-	55	-	70	-	ns	
17	$t_{RCS}$	Read Command Setup Time	0	-	0	-	0	-	ns	
18	$t_{RCH}$	Read Command Hold Time	0	-	0	-	0	-	ns	9
19	$t_{RRH}$	Read Command Hold Time Reference to $\overline{RAS}$	0	-	0	-	0	-	ns	9

**AC Characteristics (continued)** ( $V_{CC} = 2.5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0^\circ C$  to  $+70^\circ C$ )

Test Conditions:

Input timing reference level:  $V_{IH}/V_{IL}=1.8V/0.8V$ 

Output reference level:  $V_{OH}/V_{OL}=1.6V/0.8V$ 

Output Load: 1TTL gate +  $C_L$  (100pF)

Assumed  $t_r=2ns$ 

#	Std Symbol	Parameter	-50		-60		-80		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
20	$t_{RAL}$	Column Address to $\overline{RAS}$ Lead Time	25	-	30	-	40	-	ns	
21	$t_{COH}$	Output Hold After $\overline{CAS}$ Low	5	-	5	-	3	-	ns	
22	$t_{ODS}$	Output Disable Setup Time	0	-	0	-	0	-	ns	
23	$t_{OFF}$	Output Buffer Turn-Off Delay Time	0	13	0	15	0	20	ns	8, 10
24	$t_{ASC}$	Column Address Setup Time	0	-	0	-	0	-	ns	
25	$t_{CAH}$	Column Address Hold Time	7	-	10	-	10	-	ns	
26	$t_{OES}$	$\overline{OE}$ Low to $\overline{CAS}$ High Set Up	5	-	5	-	10	-	ns	
27	$t_{WCS}$	Write Command Setup Time	0	-	0	-	0	-	ns	11
28	$t_{WCH}$	Write Command Hold Time	7	-	10	-	10	-	ns	11
29	$t_{WCR}$	Write Command Hold Time to $\overline{RAS}$	44	-	55	-	70	-	ns	
30	$t_{WP}$	Write Command Pulse Width	7	-	10	-	10	-	ns	
31	$t_{RWL}$	Write Command to $\overline{RAS}$ Lead Time	13	-	15	-	20	-	ns	
32	$t_{CWL}$	Write Command to $\overline{CAS}$ Lead Time	7	-	10	-	10	-	ns	
33	$t_{DS}$	Data-in setup Time	0	-	0	-	0	-	ns	
34	$t_{DH}$	Data-in Hold Time	7	-	10	-	15	-	ns	
35	$t_{DHR}$	Data-in Hold Time to $\overline{RAS}$	44	-	55	-	70	-	ns	
36	$t_{RWC}$	Read-Modify-Write Cycle Time	110	-	135	-	180	-	ns	
37	$t_{RWD}$	$\overline{RAS}$ to $\overline{WE}$ Delay Time (Read-Modify-Write)	67	-	79	-	107	-	ns	11
38	$t_{CWD}$	$\overline{CAS}$ to $\overline{WE}$ Delay Time (Read-Modify-Write)	30	-	34	-	47	-	ns	11
39	$t_{AWD}$	Column Address to $\overline{WE}$ Delay Time (Read-Modify-Write)	42	-	49	-	67	-	ns	11



**AC Characteristics (continued)** ( $V_{CC} = 2.5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0^{\circ}C$  to  $+70^{\circ}C$ )

Test Conditions:

Input timing reference level:  $V_{IH}/V_{IL}=1.8V/0.8V$ 

Output reference level:  $V_{OH}/V_{OL}=1.6V/0.8V$ 

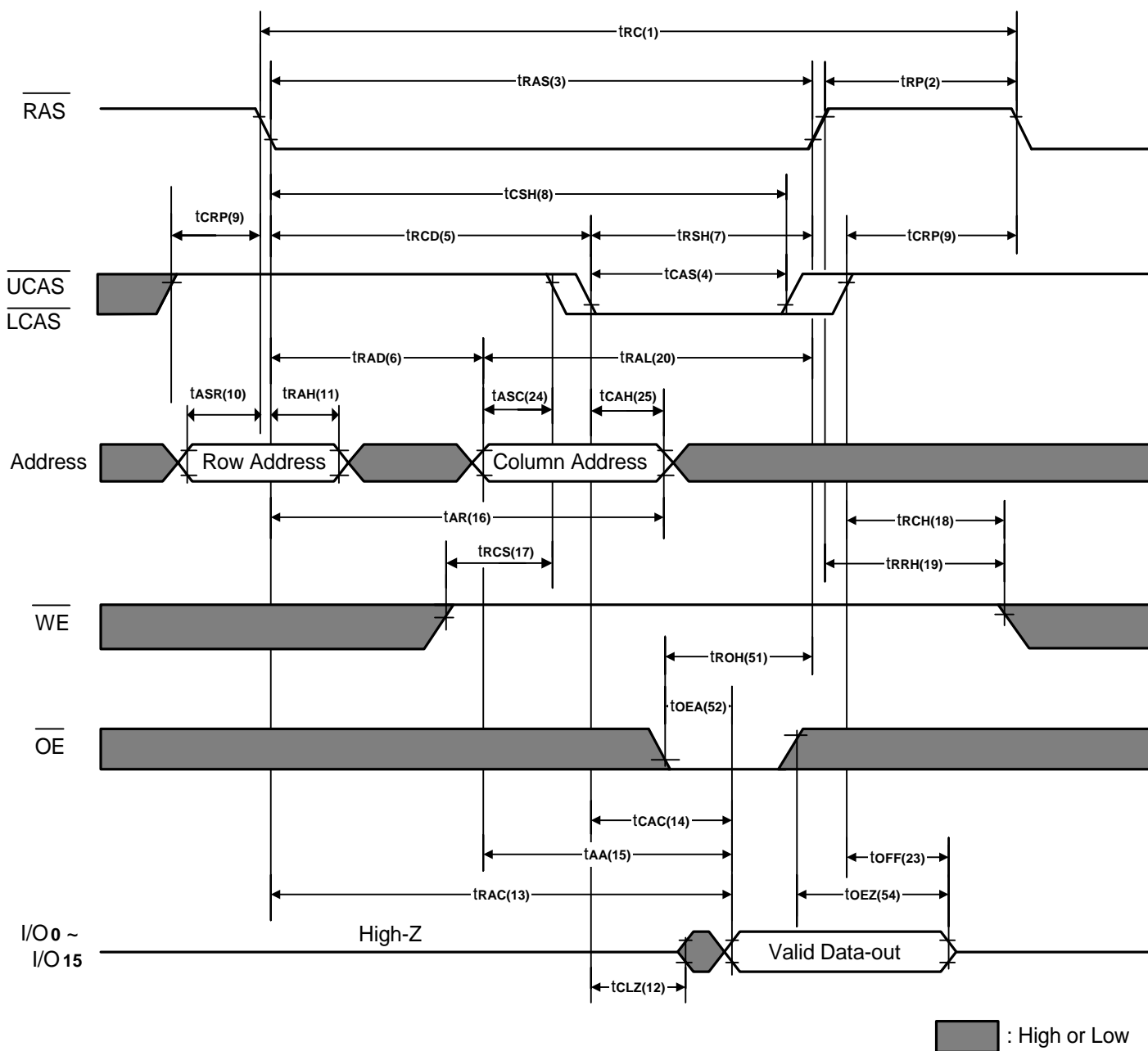
Output Load: 1TTL gate +  $C_L$  (100pF)

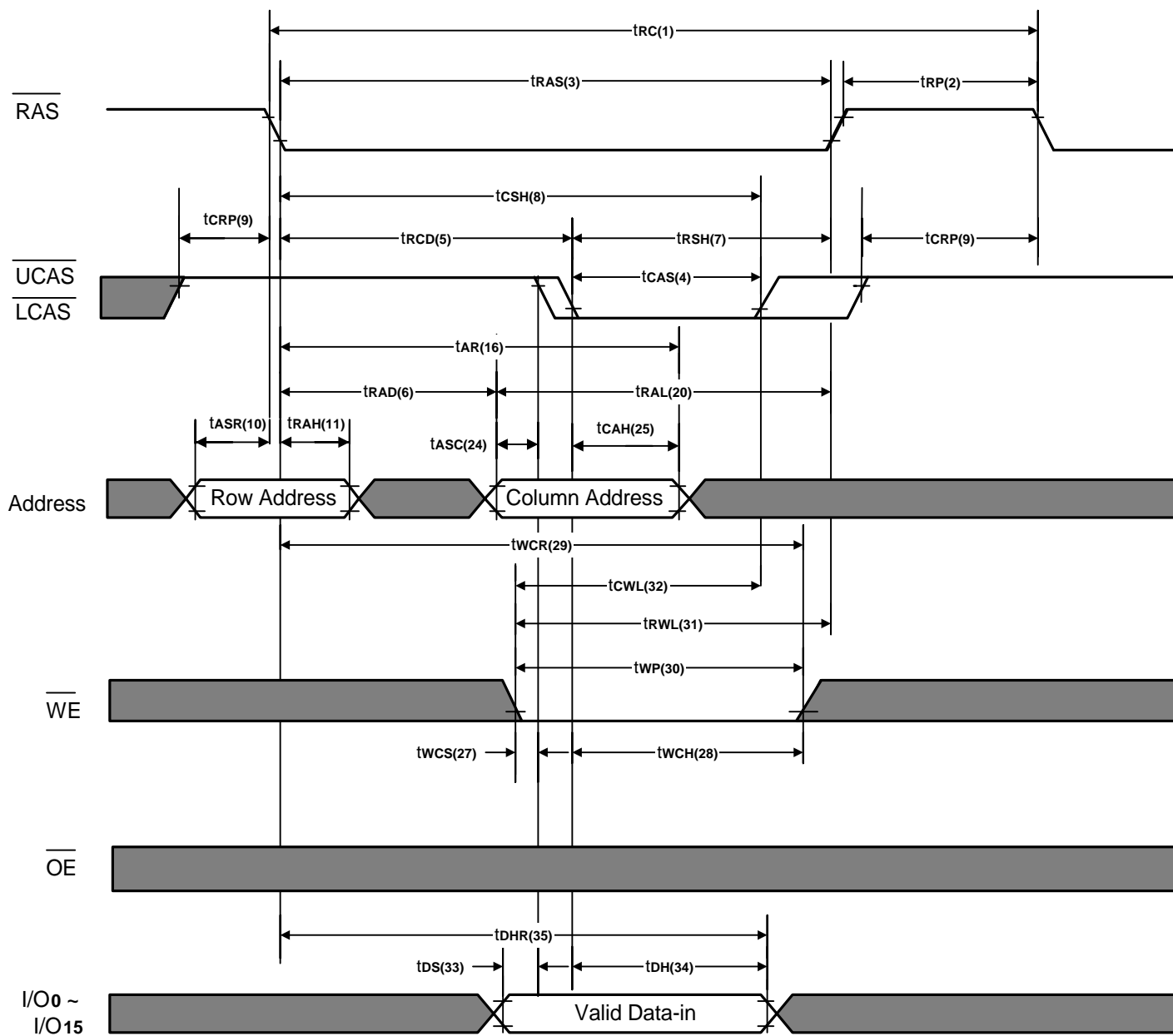
Assumed  $t_r=2ns$ 

#	Std Symbol	Parameter	-50		-60		-80		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
40	toEH	$\overline{OE}$ Hold Time from $\overline{WE}$	7	-	10	-	20	-	ns	
41	toEP	$\overline{OE}$ High Pulse Width	2	-	2	-	5	-	ns	
42	tpc	Read or Write Cycle Time (EDO Page)	20	-	25	-	35	-	ns	13
43	tCPA	Access Time from $\overline{CAS}$ Precharge (EDO Page)	-	28	-	33	-	45	ns	12
44	tCP	$\overline{CAS}$ Precharge Time (EDO Page)	7	-	10	-	10	-	ns	
45	tpCM	EDO Page Mode RMW Cycle Time	58	-	68	-	80	-	ns	
46	tCRW	EDO Page Mode $\overline{CAS}$ Pulse Width (RMW)	34	-	38	-	42	-	ns	
47	trASP	$\overline{RAS}$ Pulse Width (EDO Page)	50	100K	60	100K	80	100K	ns	
48	tCSR	$\overline{CAS}$ Setup Time ( $\overline{CAS}$ -before- $\overline{RAS}$ )	5	-	5	-	5	-	ns	3
49	tCHR	$\overline{CAS}$ Hold Time ( $\overline{CAS}$ -before- $\overline{RAS}$ )	10	-	10	-	15	-	ns	3
50	trPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time ( $\overline{CAS}$ -before- $\overline{RAS}$ )	5	-	5	-	5	-	ns	
51	tROH	$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	5	-	5	-	5	-	ns	
52	toEA	$\overline{OE}$ Access Time	-	13	-	15	-	20	ns	
53	toED	$\overline{OE}$ to Data Delay	13	-	15	-	20	-	ns	
54	toEZ	Output Buffer Turn-off Delay from $\overline{OE}$	0	13	0	15	0	20	ns	8
55	trASS	$\overline{RAS}$ pulse width ( $\overline{C}$ -B- $\overline{R}$ self-refresh)	100	-	100	-	100	-	$\mu s$	
56	trPS	$\overline{RAS}$ precharge time ( $\overline{C}$ -B- $\overline{R}$ self-refresh)	84	-	104	-	134	-	ns	
57	tCHS	$\overline{CAS}$ hold time ( $\overline{C}$ -B- $\overline{R}$ self-refresh)	-	50	-	50	-	50	ns	

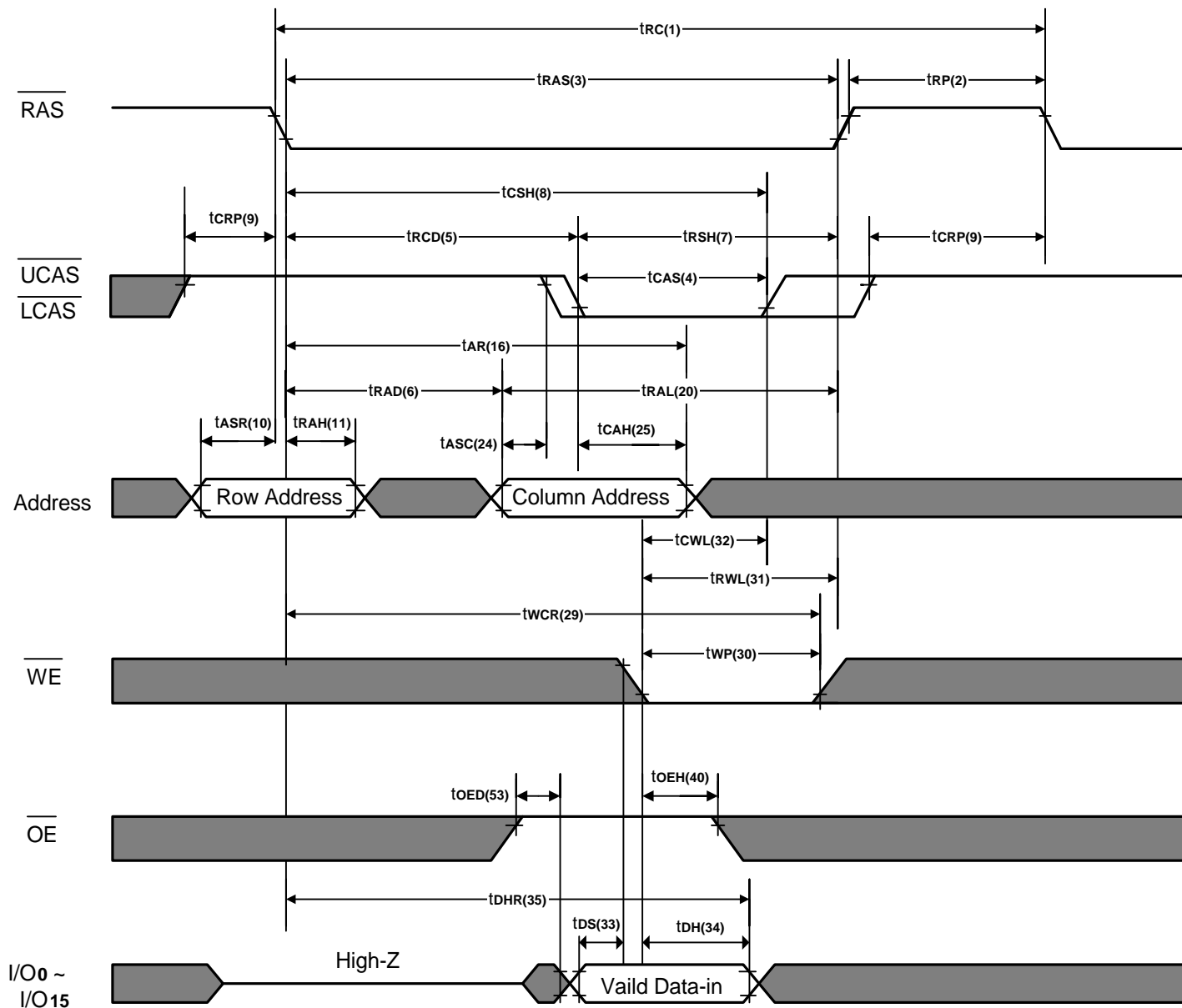
**Notes:**

1.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ , and  $I_{CC5}$  depend on cycle rate.
2.  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the outputs open.
3. An initial pause of 200 $\mu$ s is required after power-up followed by any 8  $\overline{\text{RAS}}$  cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  initialization cycles instead of 8  $\overline{\text{RAS}}$  cycles are required. 8 initialization cycles are required after extended periods of bias without clocks.
4. AC Characteristics assume  $t_r = 2\text{ns}$ . All AC parameters are measured with a load equivalent to one TTL load and 100pF,  $V_{IL}(\text{min.}) \geq \text{GND}$  and  $V_{IH}(\text{max.}) \leq V_{CC}$ .
5.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
6. Operation within the  $t_{RCO}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCO}(\text{max.})$  is specified as a reference point only. If  $t_{RCO}$  is greater than the specified  $t_{RCO}(\text{max.})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
7. Operation within the  $t_{RAD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
8. Assumes three state test load (5pF and a 500 $\Omega$  Thevenin equivalent).
9. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
10.  $t_{OFF}(\text{max.})$  defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels.
11.  $t_{WCS}$ ,  $t_{WCH}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$  and  $t_{WCH} \geq t_{WCH}(\text{min.})$ , the cycle is an early write cycle and data-out pins will remain open circuit, high impedance, throughout the entire cycle. If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{AWD} \geq t_{AWD}(\text{min.})$ , the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
12. Access time is determined by the longer of  $t_{AA}$  or  $t_{CAC}$  or  $t_{CPA}$ .
13.  $t_{ASC} \geq t_{CP}$  to achieve  $t_{PC}(\text{min.})$  and  $t_{CPA}(\text{max.})$  values.

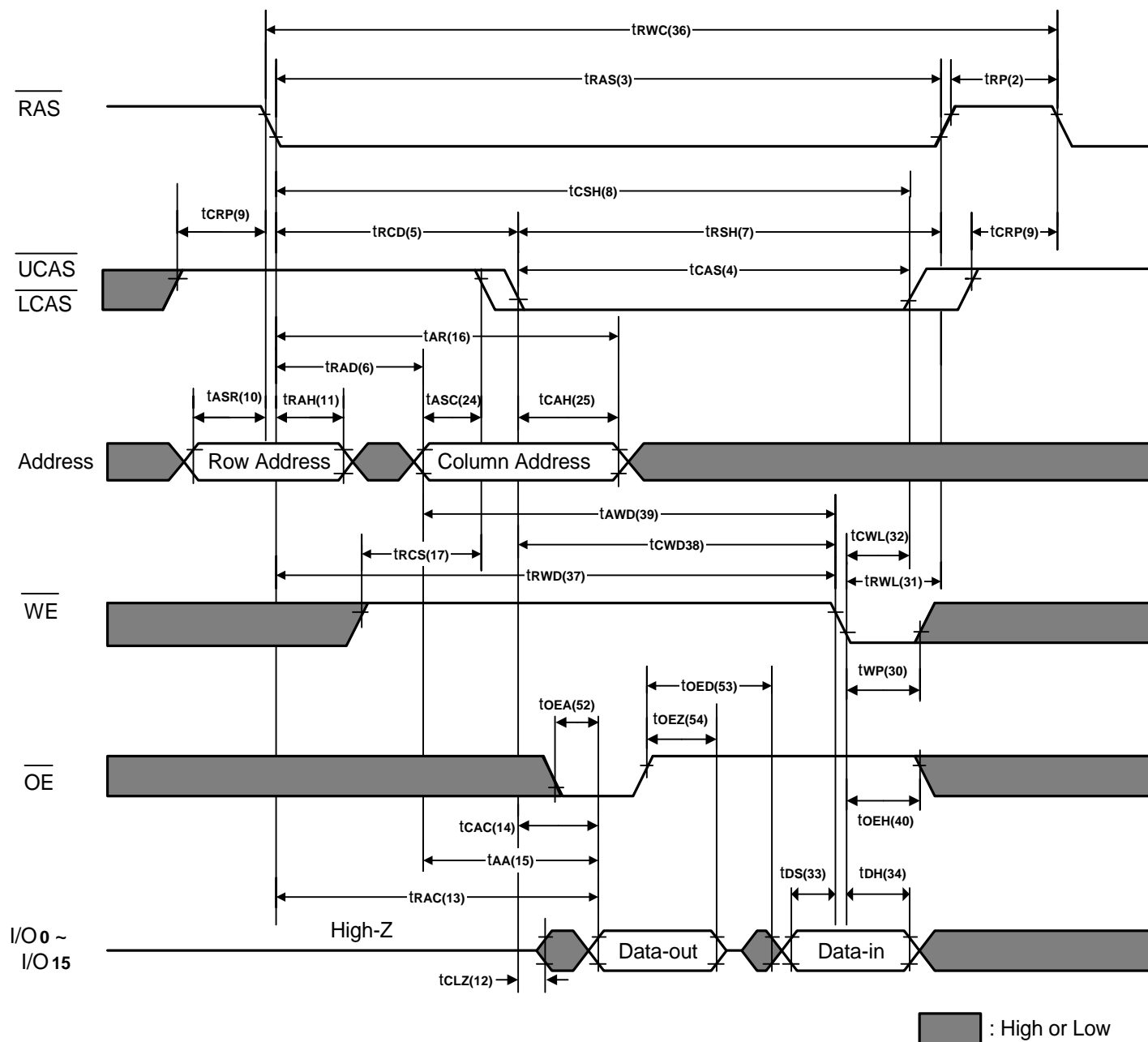
**Word Read Cycle**


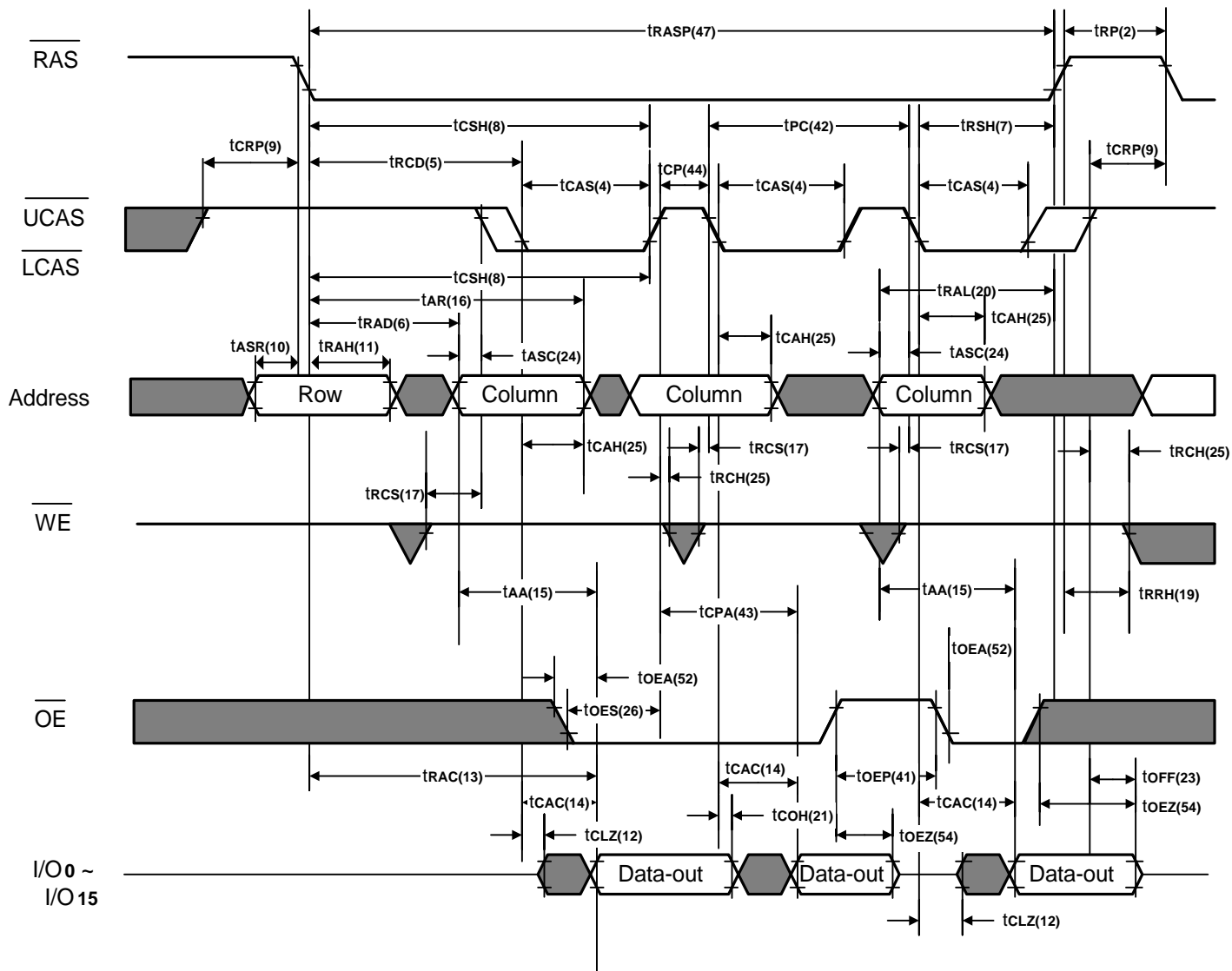
**Word Write Cycle (Early Write)**


 : High or Low

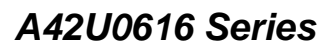
**Word Write Cycle (Late Write)**


 : High or Low

**Word Read-Modify-Write Cycle**


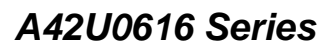
**EDO Page Mode Word Read Cycle**



■ : High or Low

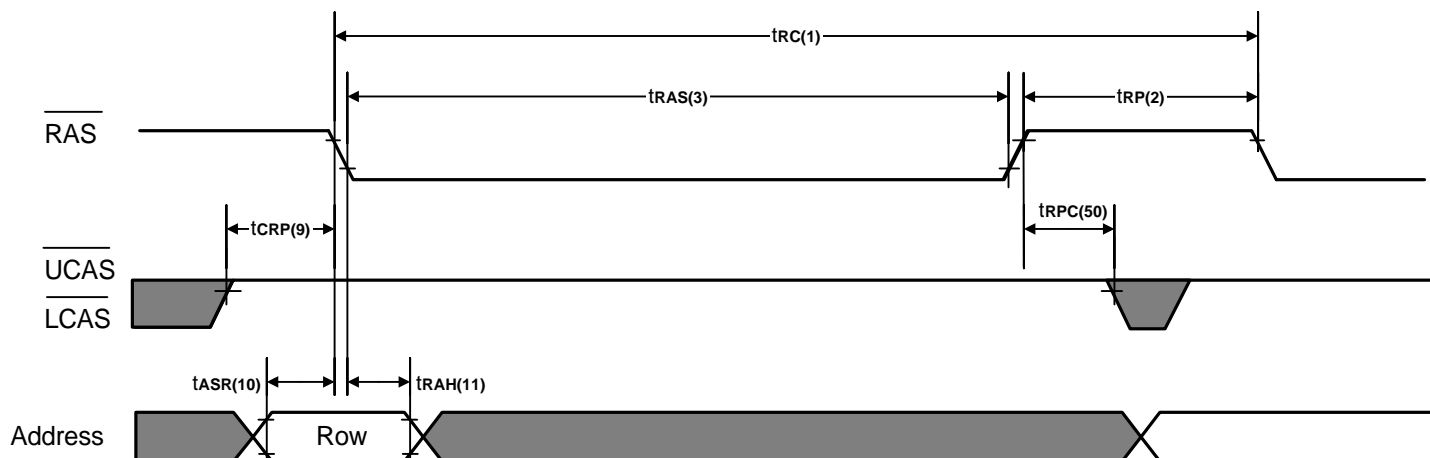


The timing diagram illustrates the sequence of signals for the 64K1602 device. The signals shown are RAS, UCAS, LCAS, Address, WE, OE, and I/O 0 ~ I/O 15. The diagram includes various timing parameters such as  $t_{RASP}(47)$ ,  $t_{CRP}(9)$ ,  $t_{CSH}(8)$ ,  $t_{PC}(42)$ ,  $t_{RSH}(7)$ ,  $t_{RCD}(5)$ ,  $t_{CAS}(4)$ ,  $t_{CP}(44)$ ,  $t_{RAD}(6)$ ,  $t_{ASR}(10)$ ,  $t_{RAH}(11)$ ,  $t_{ASC}(24)$ ,  $t_{CAH}(25)$ ,  $t_{CWL}(32)$ ,  $t_{WCS}(27)$ ,  $t_{WCH}(28)$ ,  $t_{WP}(30)$ ,  $t_{TRP}(2)$ ,  $t_{RAL}(20)$ ,  $t_{TRWL}(31)$ ,  $t_{DS}(33)$ , and  $t_{DH}(34)$ . The Address signal shows a sequence of Row and Column addresses. The WE signal shows a sequence of write pulses. The OE signal is active low and remains high. The I/O 0 ~ I/O 15 signal shows a sequence of Data-in operations. A legend indicates that shaded areas represent High or Low states.




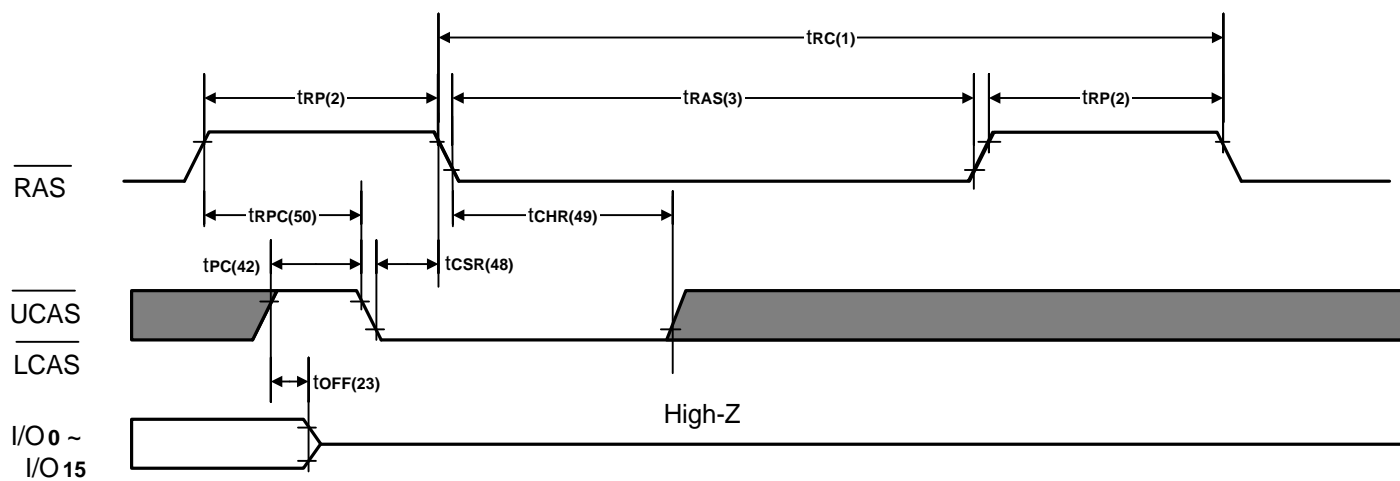
[illegible]

 : High or Low


**RAS Only Refresh Cycle**


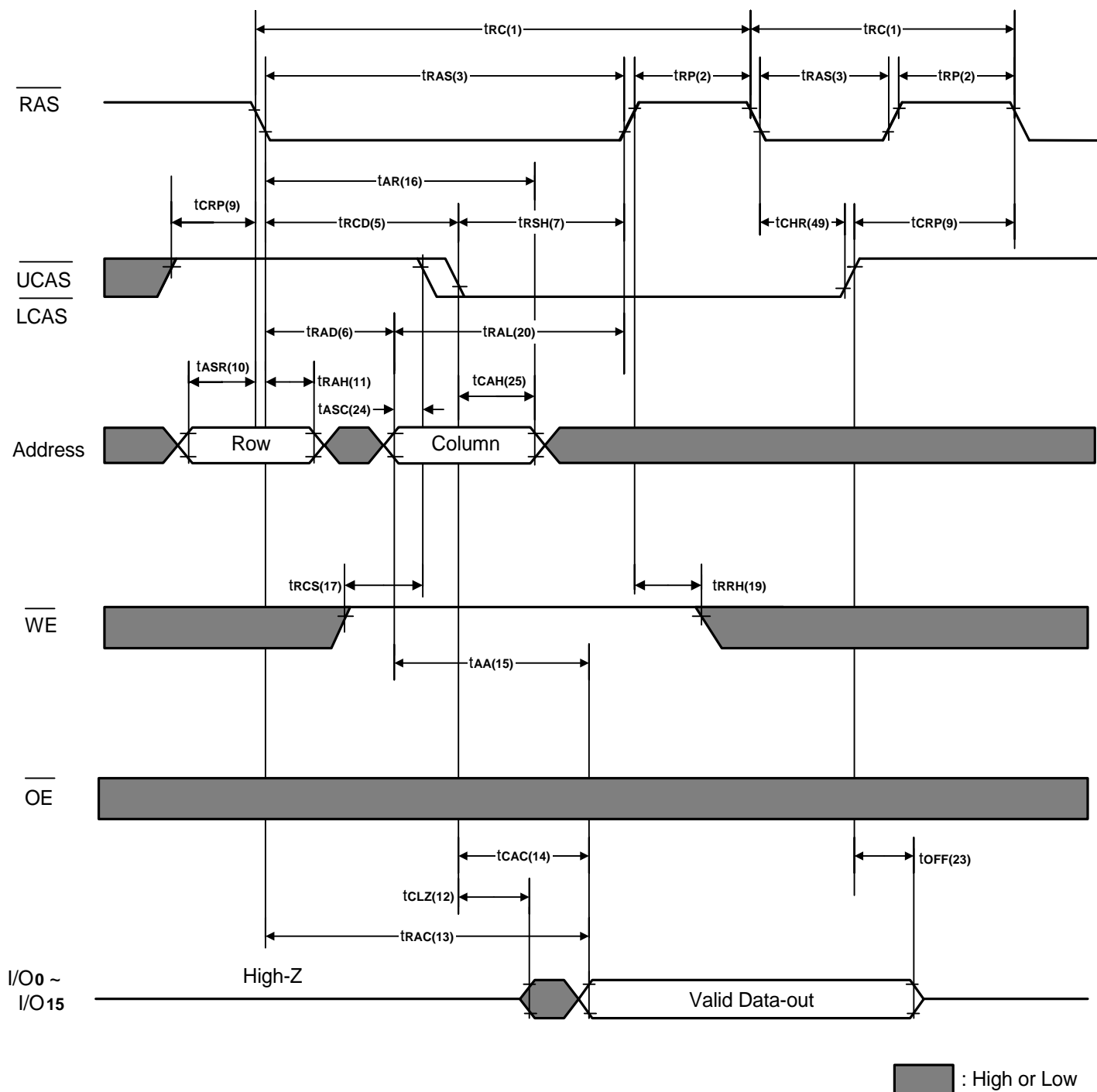
Note:  $\overline{WE}$ ,  $\overline{OE}$  = Don't care.

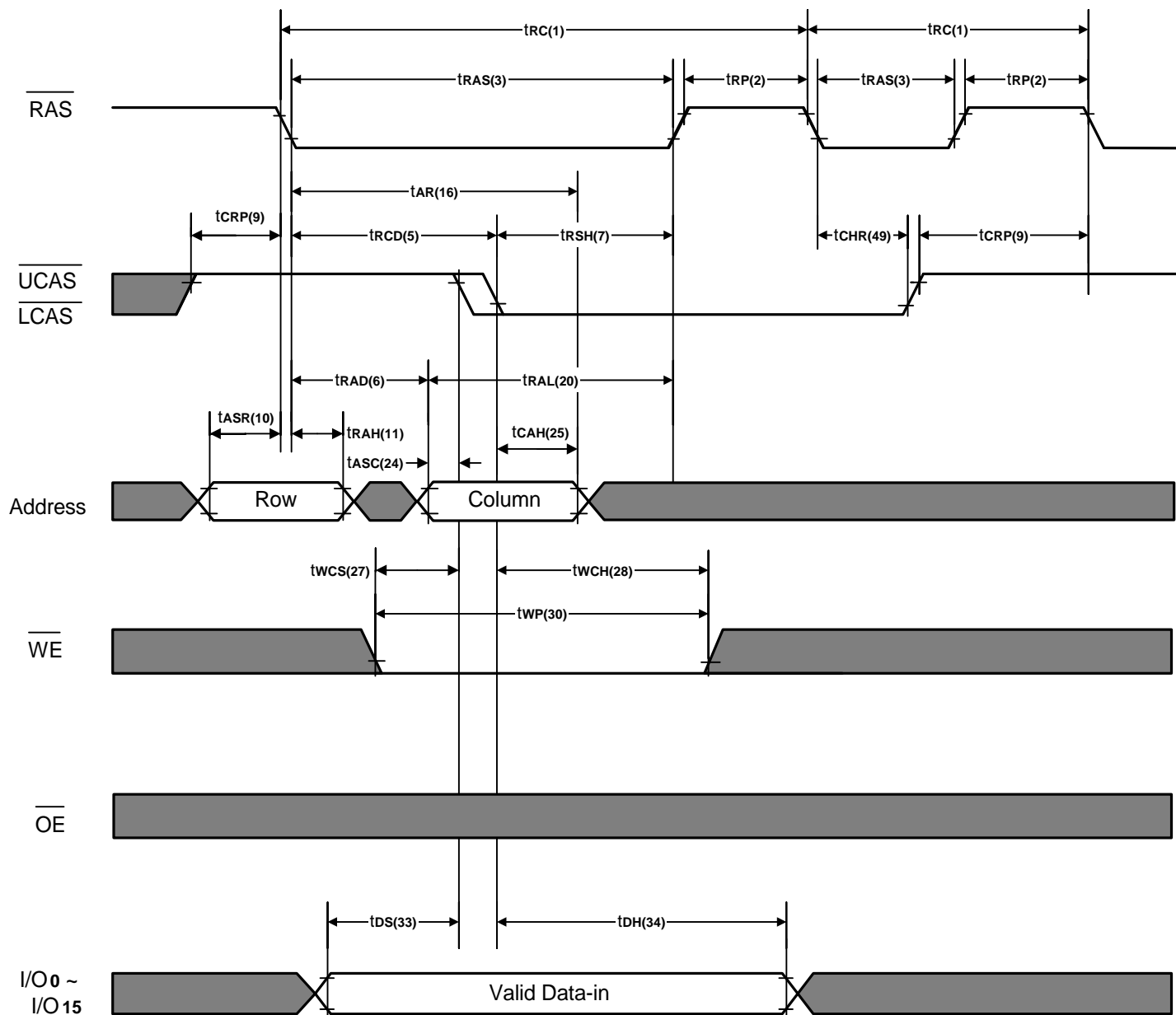
 : High or Low


**CAS Before RAS Refresh Cycle**


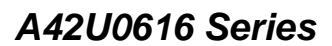
Note:  $\overline{WE}$ ,  $\overline{OE}$ , Address = Don't care.

 : High or Low

**Hidden Refresh Cycle (Word Read)**


**Hidden Refresh Cycle (Early Word Write)**


 : High or Low



The timing diagram illustrates the relationship between various control signals and data flow during memory operations. The signals shown are:

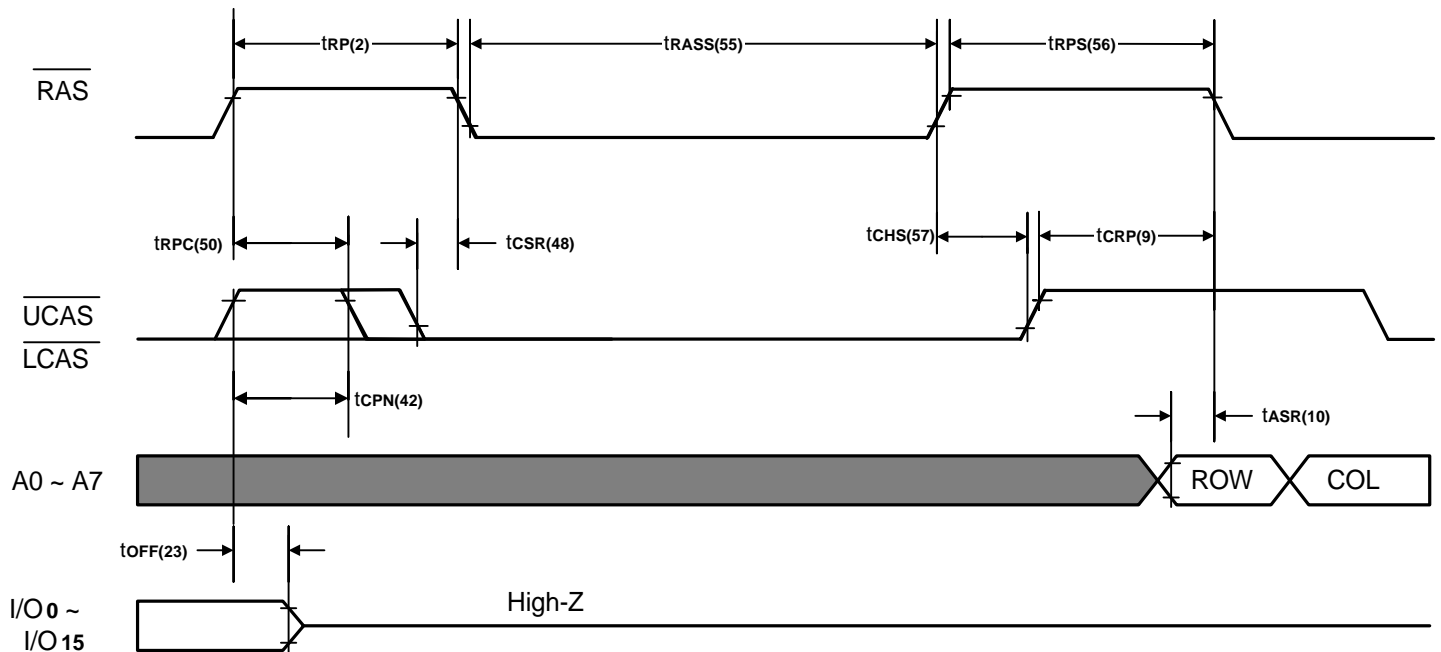
- RAS**: Row Address Strobe.
- UCAS/LCAS**: Universal Column Address Strobe / Local Column Address Strobe.
- Address**: Memory address bus, showing Row and Column addresses.
- WE**: Write Enable signal.
- OE**: Output Enable signal.
- I/O<sub>0</sub> ~ I/O<sub>15</sub>**: Data bus.

Key timing parameters labeled include:

- $t_{RAS}(47)$ ,  $t_{CRP}(9)$ ,  $t_{RCD}(5)$ ,  $t_{CSH}(8)$ ,  $t_{PC}(42)$ ,  $t_{CAS}(4)$ ,  $t_{CP}(44)$ ,  $t_{RSH}(7)$ ,  $t_{CPR}(9)$ ,  $t_{RAD}(6)$ ,  $t_{RAH}(11)$ ,  $t_{ASC}(24)$ ,  $t_{CAH}(25)$ ,  $t_{ASC}(24)$ ,  $t_{CAH}(25)$ ,  $t_{RAL}(20)$ ,  $t_{SR}(10)$ ,  $t_{RCH}(18)$ ,  $t_{WCS}(27)$ ,  $t_{WC}(28)$ ,  $t_{AA}(15)$ ,  $t_{CAP}(43)$ ,  $t_{CAC}(14)$ ,  $t_{DQS}(33)$ ,  $t_{DH}(34)$ ,  $t_{COH}(21)$ ,  $t_{OEA}(52)$ .

The diagram shows three sequential memory accesses (Row → Column → Column) with corresponding data output and input phases. Shaded areas indicate active periods for RAS, UCAS/LCAS, WE, and OE.

 : High or Low

**Self Refresh Mode**


Note:  $\overline{WE}$ ,  $\overline{OE}$  = Don't care.

 : High or Low

**■ Self Refresh Mode.**
**a. Entering the Self Refresh Mode:**

The A42U0616 Self Refresh Mode is entered by using  $\overline{CAS}$  before  $\overline{RAS}$  cycle and holding  $\overline{RAS}$  and  $\overline{CAS}$  signal "low" longer than 100 $\mu$ s.

**b. Continuing the Self Refresh Mode:**

The Self Refresh Mode is continued by holding  $\overline{RAS}$  "low" after entering the Self Refresh Mode.

It does not depend on  $\overline{CAS}$  being "high" or "low" after entering the Self Refresh Mode continue the Self Refresh Mode.

**c. Exiting the Self Refresh Mode:**

The A42U0616 exits the Self Refresh Mode when the  $\overline{RAS}$  signal is brought "high".



**Capacitance** (Ta = Room Temperature, VCC = 2.5V ± 10%)

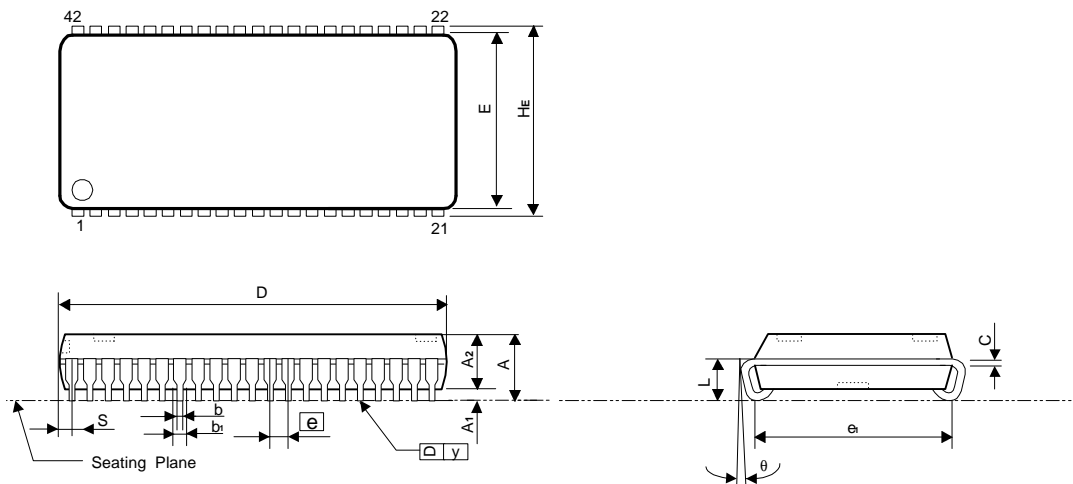
Symbol	Signals	Parameter	Max.	Unit	Test Conditions
CIN1	A0 – A9	Input Capacitance	5	pF	Vin = 0V
CIN2	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$		7	pF	Vin = 0V
C <sub>I/O</sub>	I/O <sub>0</sub> - I/O <sub>15</sub>	I/O Capacitance	10	pF	Vin = Vout = 0V

## Ordering Codes

Package\ $\overline{\text{RAS}}$ Access Time	50ns	60ns	80ns	Refresh Cycle	Self-Refresh
42L SOJ (400mil)	A42U0616S-50	A42U0616S-60	A42U0616S-80	1K	Yes
50(44)L TSOP type II (400mil)	A42U0616V-50	A42U0616V-60	A42U0616V-80	1K	Yes

**Package Information**
**SOJ 42L Outline Dimensions**

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.128	0.138	0.148	3.25	3.51	3.76
A1	0.025	-	-	0.64	-	-
A2	0.105	0.110	0.115	2.67	2.79	2.92
b1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.015	0.018	0.020	0.38	0.46	0.51
C	0.007	0.008	0.013	0.18	0.20	0.33
D	1.075	1.080	1.085	27.31	27.43	27.56
E	0.395	0.400	0.405	10.03	10.16	10.29
e	-	0.050	-	-	1.27	-
e1	-	0.370	-	-	9.4	-
HE	0.435	0.440	0.445	11.05	11.18	11.30
L	0.082	-	-	2.08	-	-
S	-	-	0.045	-	-	1.14
y	-	-	0.003	-	-	0.075
$\theta$	0°	-	10°	0°	-	10°

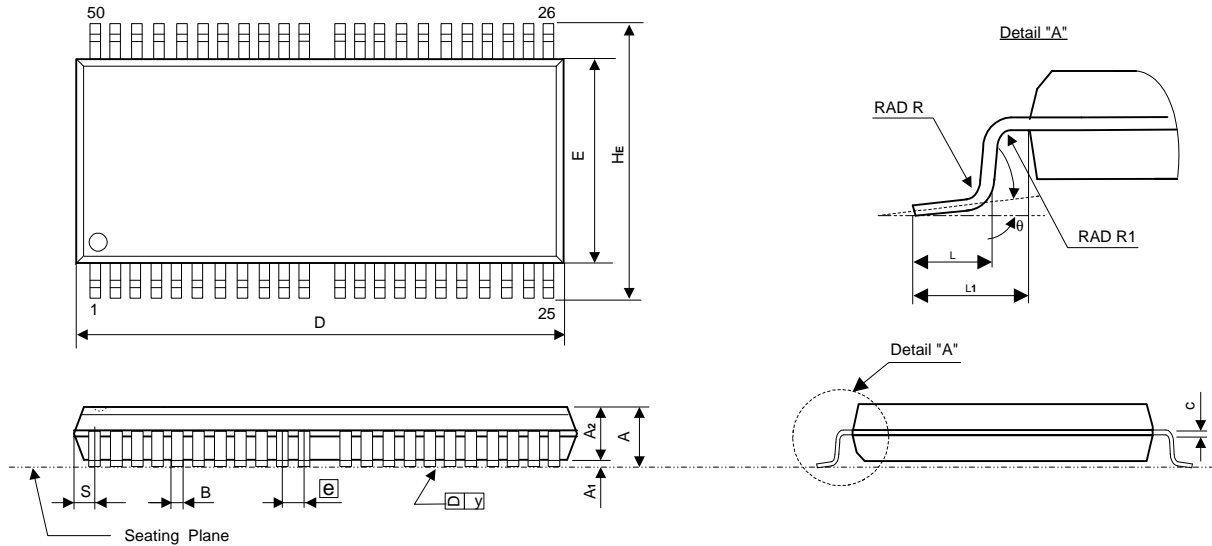
**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.



**Package Information**
**TSOP 50/44L (Type II) Outline Dimensions**

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.048	-	-	1.20
A1	0.002	-	0.006	0.05	-	0.15
A2	0.037	0.039	0.042	0.95	1.00	1.05
B	0.012	-	0.018	0.30	-	0.45
c	0.005	-	0.008	0.12	-	0.21
D	0.820	0.825	0.830	20.82	20.95	21.08
E	0.400 BSC			10.16 BSC		
HE	0.463 BSC			11.76 BSC		
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	0.031 REF			0.80 REF		
[e]	0.031 BSC			0.80 BSC		
R	0.005	-	0.010	0.12	-	0.25
R1	0.005	-	-	0.12	-	-
S	0.0435 REF			0.875 BSC		
θ	0°	-	5°	0°	-	5°

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.