



## **A625308A Series**

***Preliminary***

**32K X 8 BIT CMOS SRAM**

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### **Document Title**

**32K X 8 BIT CMOS SRAM**

### **Revision History**

<b><u>Rev. No.</u></b>	<b><u>History</u></b>	<b><u>Issue Date</u></b>	<b><u>Remark</u></b>
0.0	Initial issue	February 2, 2001	Preliminary
0.1	Add ultra temp grade and 28-pin DIP package type	November 7, 2001	
0.2	Add SI grade	July 17, 2002	



# A625308A Series

## Preliminary

## 32K X 8 BIT CMOS SRAM

### Features

- Power Supply Range: 4.5V to 5.5V
- Access times: 70 ns
  - A625308A-S series: Operating: 35mA (max.)  
Standby: 10μA (max.)
  - A625308A-SI/SU series: Operating: 35mA (max.)  
Standby: 15μA (max.)

- Extended operating temperature range: 0°C to 70°C for -S series, -25°C to 85°C for -SI series, -40°C to 85°C for -SU series.
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 2.0V (min.)
- Available in 28-pin, DIP/SOP and TSOP

### General Description

The A625308A is a low operating current 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates on a voltage from 4.5V to 5.5V.

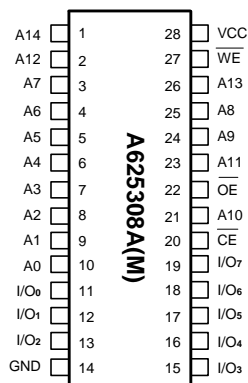
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Minimum standby power is drawn by this device when  $\overline{CE}$  is at a high level, independent of the other input levels.

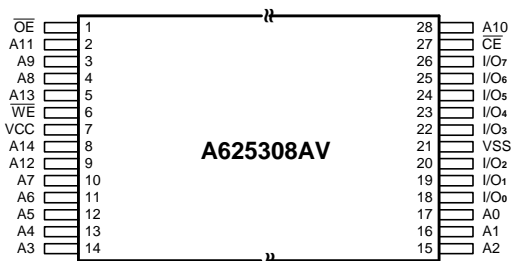
Data retention is guaranteed at a power supply voltage as low as 2.0V.

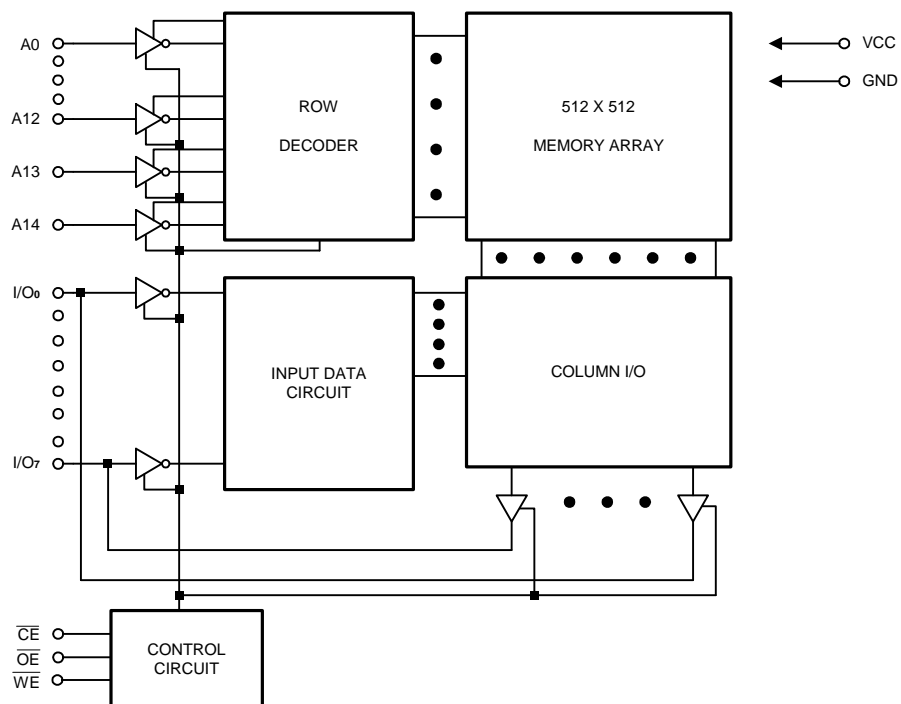
### Pin Configurations

#### ■ DIP / SOP



#### ■ TSOP



**Block Diagram**

**Pin Descriptions – DIP / SOP**

Pin No.	Symbol	Description
1-10, 21, 23-26	A0 - A14	Address Input
11-13, 15-19	I/O <sub>0</sub> - I/O <sub>7</sub>	Data Input/Output
20	$\overline{CE}$	Chip Enable
22	$\overline{OE}$	Output Enable
27	$\overline{WE}$	Write Enable
28	VCC	Power Supply
14	GND	Ground

**Pin Description-TSOP**

Pin No.	Symbol	Description
2-5, 8-17, 28	A0 - A14	Address Input
18-20, 22-26	I/O <sub>0</sub> - I/O <sub>7</sub>	Data Input/Output
27	$\overline{CE}$	Chip Enable
1	$\overline{OE}$	Output Enable
6	$\overline{WE}$	Write Enable
7	VCC	Power Supply
21	GND	Ground

**Recommended DC Operating Conditions**

( $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  or  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	-	VCC + 0.5	V
V <sub>IL</sub>	Input Low Voltage	-0.5	0	+0.8	V

**Absolute Maximum Ratings\***

VCC to GND . . . . . -0.5V to +7.0V  
 IN, IN/OUT Volt to GND . . . . . -0.5V to VCC + 0.5V  
 Operating Temperature, T<sub>opr</sub> . . . . .  
 . . . . .  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  or  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 Storage Temperature, T<sub>stg</sub> . . . . .  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
 Power Dissipation, P<sub>T</sub> . . . . . 0.7W  
 Soldering Temp. & Time . . . . .  $260^{\circ}\text{C}$ , 10 sec

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics** ( $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  or  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , VCC = 5.0V  $\pm$  10%, GND = 0V)

Symbol	Parameter	A625308A-70S/SI/SU		Unit	Conditions
		Min.	Max.		
I <sub>LI</sub>	Input Leakage Current	-	1	$\mu\text{A}$	V <sub>IN</sub> = GND to VCC
I <sub>LO</sub>	Output Leakage Current	-	1	$\mu\text{A}$	$\overline{\text{CE}} = \text{V}_{\text{IH}}$ V <sub>IO</sub> = GND to VCC
I <sub>CC</sub>	Active Power Supply Current	-	5	mA	$\overline{\text{CE}} = \text{V}_{\text{IL}}$ , I <sub>I/O</sub> = 0mA
I <sub>CC1</sub>	Dynamic Operating Current	-	35	mA	Min. Cycle, Duty = 100% $\overline{\text{CE}} = \text{V}_{\text{IL}}$ , I <sub>I/O</sub> = 0mA
I <sub>CC2</sub>	Dynamic Operating Current	-	5	mA	$\overline{\text{CE}} = \text{V}_{\text{IL}}$ , V <sub>IH</sub> = VCC V <sub>IL</sub> = 0V, f = 1 MHz I <sub>I/O</sub> = 0 mA

**DC Electrical Characteristics (continued)**

Symbol	Parameter	A625308A-70S		A625308A-70SI/SU		Unit	Conditions
		Min.	Max.	Min.	Max.		
I <sub>SB</sub>	Supply Current Standby Power	-	0.5	-	0.5	mA	$\overline{CE} = V_{IH}$
I <sub>SB1</sub>		-	10	-	15	μA	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq 0V$
V <sub>OL</sub>	Output Low Voltage	-	0.4	-	0.4	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4	-	2.4	-	V	I <sub>OH</sub> = -1.0 mA

**Truth Table**

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	High Z	I <sub>SB</sub> , I <sub>SB1</sub>
Output Disable	L	H	H	High Z	I <sub>CC</sub> , I <sub>CC1</sub> , I <sub>CC2</sub>
Read	L	L	H	DOUT	I <sub>CC</sub> , I <sub>CC1</sub> , I <sub>CC2</sub>
Write	L	X	L	DIN	I <sub>CC</sub> , I <sub>CC1</sub> , I <sub>CC2</sub>

Note: X: H or L

**Capacitance** (T<sub>A</sub> = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C <sub>IN</sub> *	Input Capacitance	-	6	pF	V <sub>IN</sub> = 0V
C <sub>I/O</sub> *	Input/Output Capacitance	-	8	pF	V <sub>I/O</sub> = 0V

\* These parameters are sampled and not 100% tested.

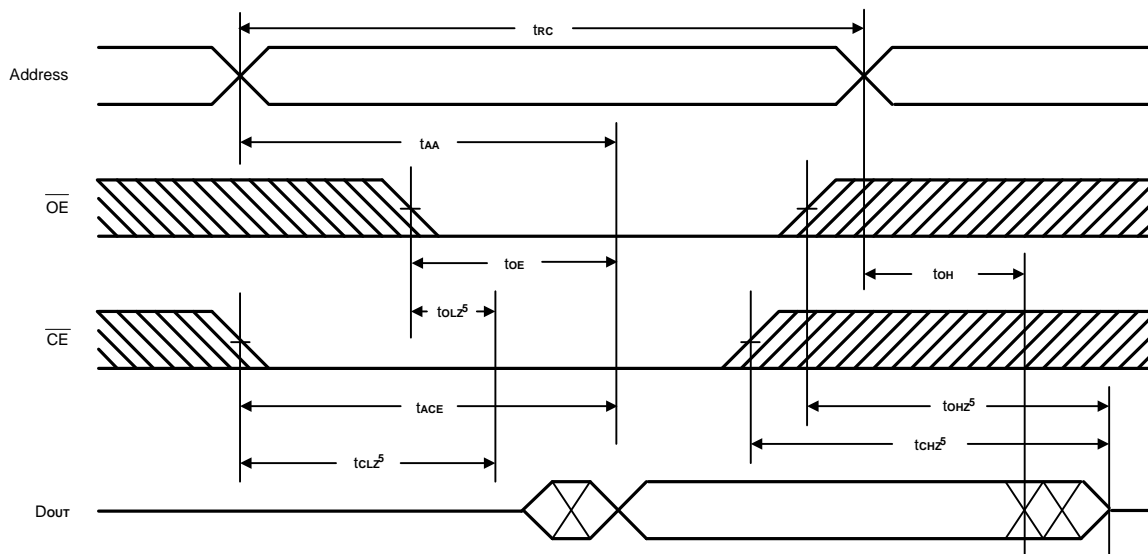
**AC Characteristics** ( $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  or  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$ )

Symbol	Parameter	A625308A-70S/SI/SU		Unit
		Min.	Max.	
Read Cycle				
t <sub>RC</sub>	Read Cycle Time	70	-	ns
t <sub>AA</sub>	Address Access Time	-	70	ns
t <sub>ACE</sub>	Chip Enable Access Time	-	70	ns
t <sub>OE</sub>	Output Enable to Output Valid	-	35	ns
t <sub>CLZ</sub>	Chip Enable to Output in Low Z	10	-	ns
t <sub>OLZ</sub>	Output Enable to Output in Low Z	5	-	ns
t <sub>CHZ</sub>	Chip Disable to Output in High Z	-	25	ns
t <sub>OHZ</sub>	Output Disable to Output in High Z	-	25	ns
t <sub>OH</sub>	Output Hold from Address Change	10	-	ns
Write Cycle				
t <sub>WC</sub>	Write Cycle Time	70	-	ns
t <sub>CW</sub>	Chip Enable to End of Write	60	-	ns
t <sub>AS</sub>	Address Set up Time	0	-	ns
t <sub>AW</sub>	Address Valid to End of Write	60	-	ns
t <sub>WP</sub>	Write Pulse Width	50	-	ns
t <sub>WR</sub>	Write Recovery Time	0	-	ns
t <sub>WHZ</sub>	Write to Output in High Z	-	25	ns
t <sub>DW</sub>	Data to Write Time Overlap	30	-	ns
t <sub>DH</sub>	Data Hold from Write Time	0	-	ns
t <sub>OW</sub>	Output Active from End of Write	5	-	ns

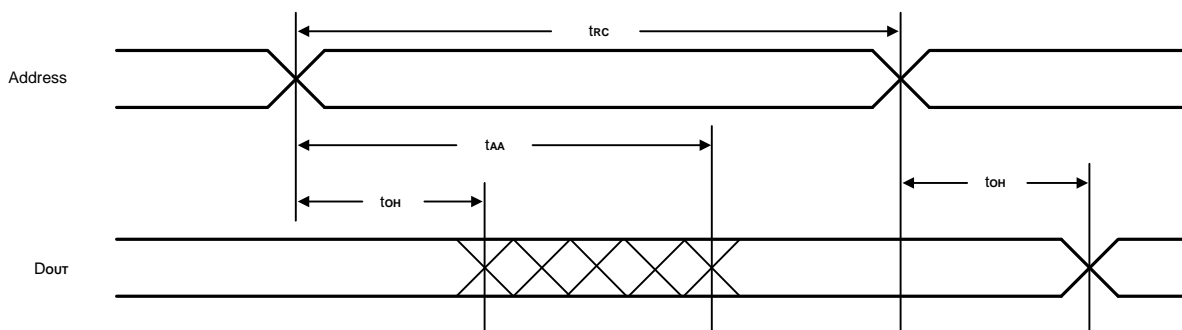
Notes:  $t_{CHZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

## Timing Waveforms

### Read Cycle 1 <sup>(1)</sup>

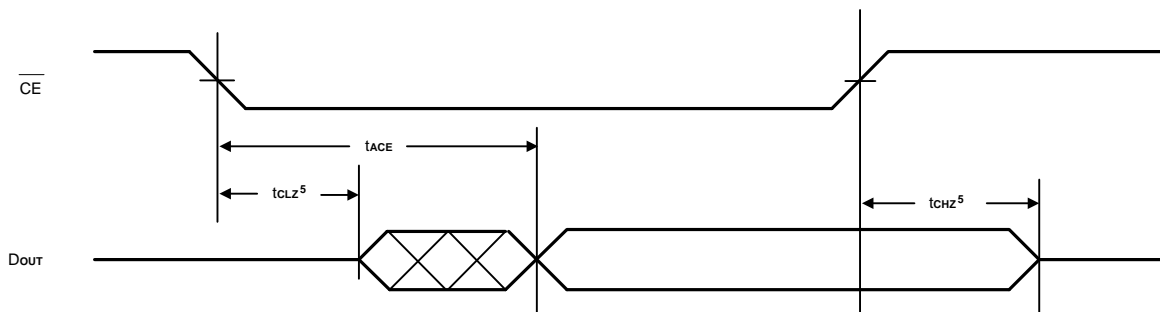


### Read Cycle 2 <sup>(1, 2, 4)</sup>



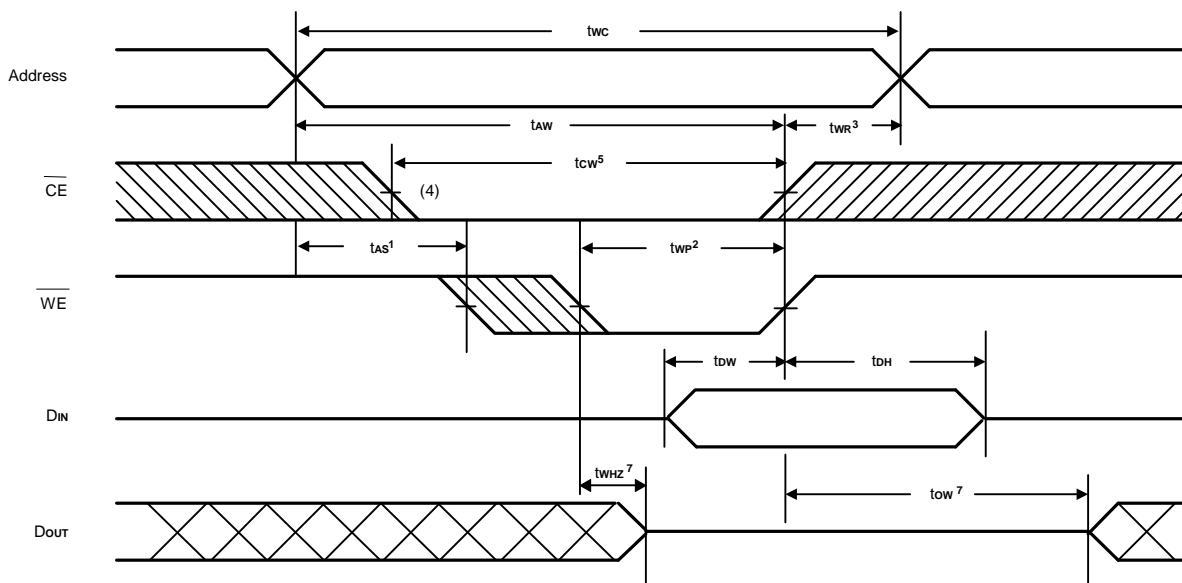
## Timing Waveforms (continued)

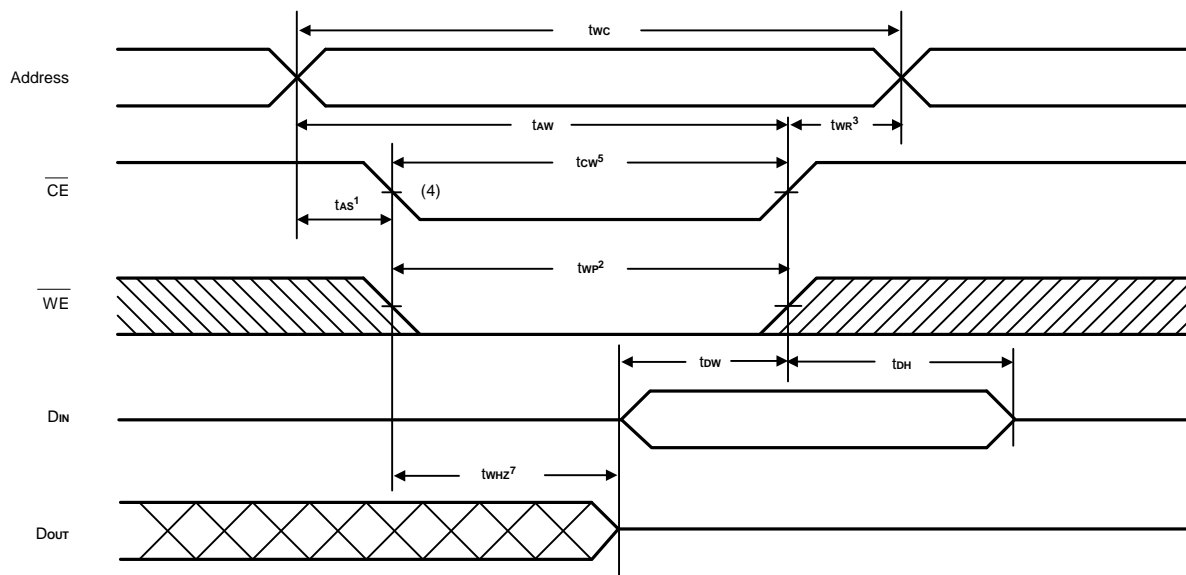
### Read Cycle 3 <sup>(1, 3, 4)</sup>



- Notes:
1.  $\overline{WE}$  is high for Read Cycle.
  2. Device is continuously enabled,  $\overline{CE} = V_{IL}$ .
  3. Address valid prior to or coincident with  $\overline{CE}$  transition low.
  4.  $\overline{OE} = V_{IL}$ .
  5. Transition is measured  $\pm 500\text{mV}$  from steady state. This parameter is sampled and not 100% tested.

### Write Cycle 1 <sup>(6)</sup> (Write Enable Controlled)

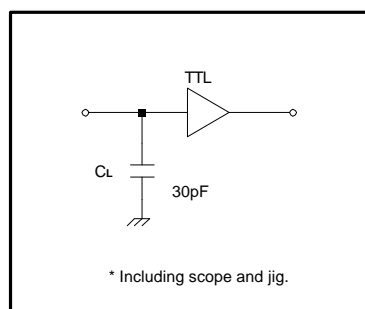
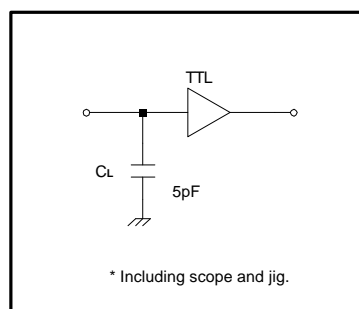


**Timing Waveforms (continued)**
**Write Cycle 2 <sup>(6)</sup>**  
**(Chip Enable Controlled)**


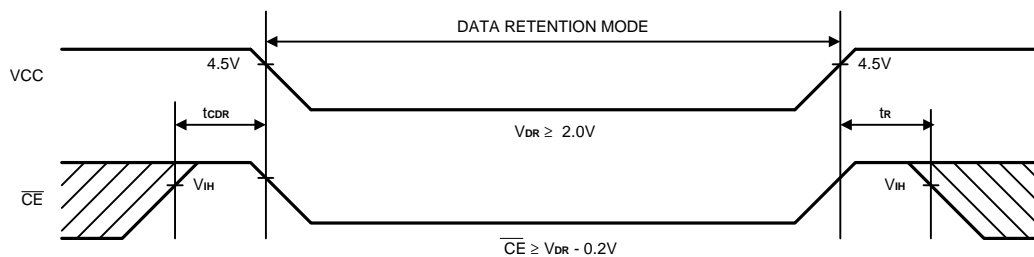
- Notes:
1.  $t_{AS}^1$  is measured from the address valid to the beginning of Write.
  2. A Write occurs during the overlap ( $t_{WP}^2$ ) of a low  $\overline{CE}$  and a low  $\overline{WE}$ .
  3.  $t_{WR}^3$  is measured from the earliest of  $\overline{CE}$  or  $\overline{WE}$  going high to the end of the Write cycle.
  4. If the  $\overline{CE}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, outputs remain in a high impedance state.
  5.  $t_{CW}^5$  is measured from the later of  $\overline{CE}$  going low to the end of Write.
  6.  $\overline{OE}$  level is high or low.
  7. Transition is measured  $\pm 500\text{mV}$  from steady. This parameter is sampled and not 100% tested.

**AC Test Conditions**

Input Pulse Levels	0V, 3V
Input Rise And Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 1 and 2


**Figure 1. Output Load**

**Figure 2. Output Load for  $t_{CLZ1}$ ,  $t_{CLZ2}$ ,  $t_{OHZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ1}$ ,  $t_{CHZ2}$ ,  $t_{WHZ}$ , and  $t_{OW}$** 
**Data Retention Characteristics** ( $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  or  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )

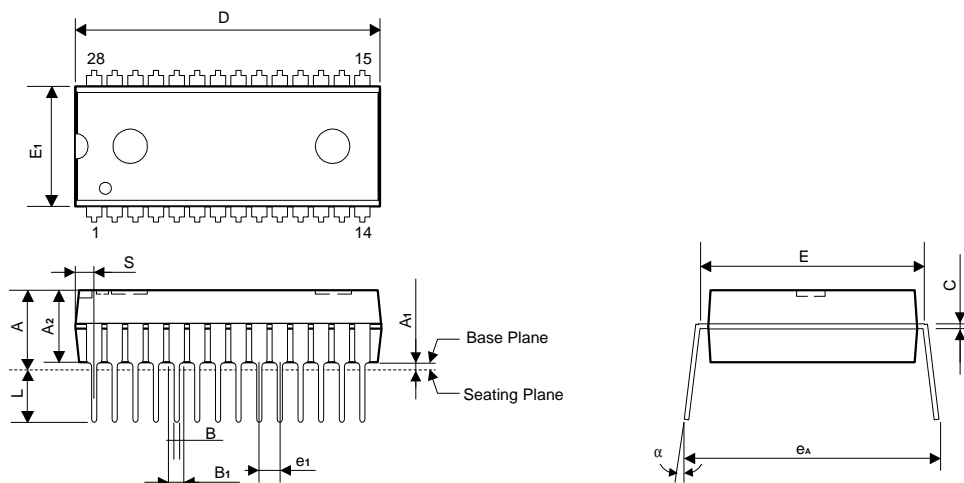
Symbol	Parameter	Min.	Max.	Unit	Conditions
$V_{DR}$	VCC for Data Retention	2.0	5.5	V	$\overline{CE} \geq V_{CC} - 0.2V$
$I_{CCDR}$	Data Retention Current	-	3	$\mu A$	$V_{CC} = 2.0V$ , $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq 0V$
$t_{CDR}$	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
$t_R$	Operation Recovery Time	$t_{RC}$	-	ns	

**Low VCC Data Retention Waveform**

**Ordering Information**

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. ( $\mu A$ )	Package
A625308A-70S	70	35	10	28L DIP
A625308AM-70S		35	10	28L SOP
A625308AV-70S		35	10	28L TSOP (Forward)
A625308A-70SI		35	15	28L DIP
A625308AM-70SI		35	15	28L SOP
A625308AV-70SI		35	15	28L TSOP (Forward)
A625308A-70SU		35	15	28L DIP
A625308AM-70SU		35	15	28L SOP
A625308AV-70SU		35	15	28L TSOP (Forward)

**Package Information**
**P-DIP 28L Outline Dimensions**

unit: inches/mm



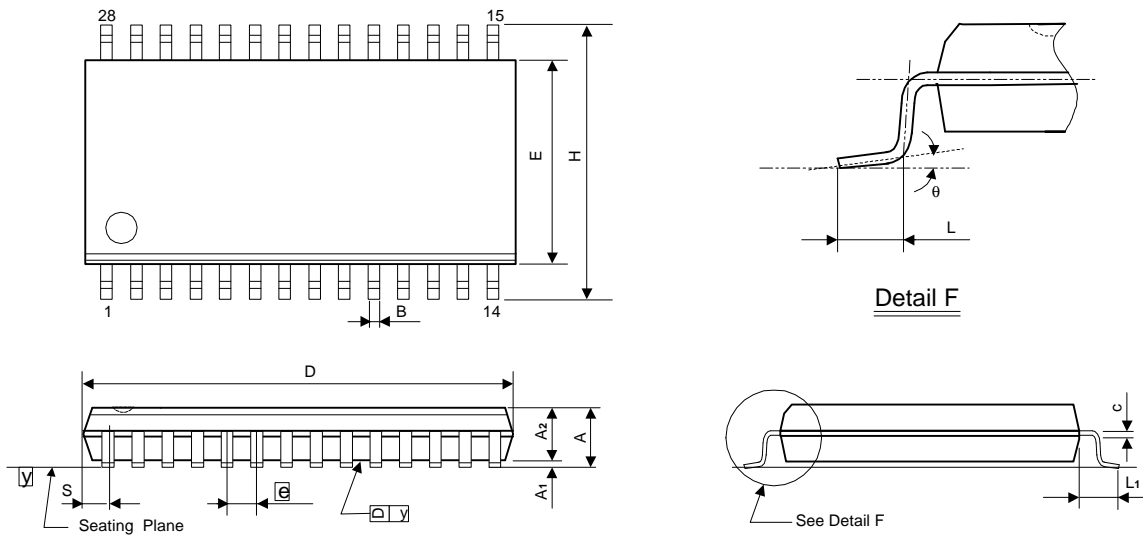
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.210	-	-	5.33
A1	0.010	-	-	0.25	-	-
A2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B1	0.058	0.060	0.064	1.47	1.52	1.63
C	0.008	0.010	0.014	0.20	0.25	0.36
D	-	1.460	1.470	-	37.08	37.34
E	0.590	0.600	0.610	14.99	15.24	15.49
E1	0.540	0.545	0.550	13.72	13.84	13.97
e1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
$\alpha$	0°	-	15°	0°	-	15°
eA	0.630	0.650	0.670	16.00	16.51	17.02
S	-	-	0.090	-	-	2.29

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E1 does not include resin fins.
3. Dimension S includes end flash.

**Package Information**
**SOP (W.B.) 28L Outline Dimensions**

unit: inches/mm



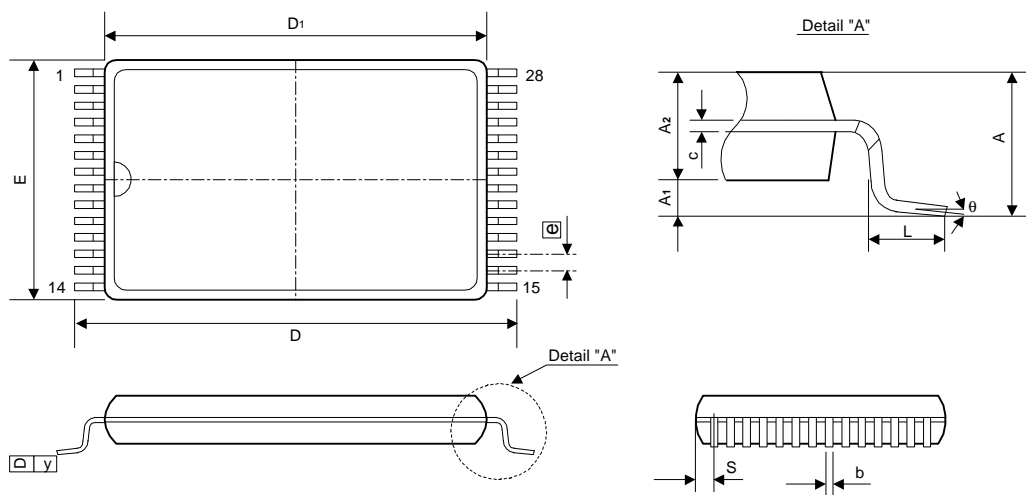
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.112	-	-	2.85
A1	0.004	-	-	0.10	-	-
A2	0.093	0.098	0.103	2.36	2.49	2.62
B	0.014	0.016	0.020	0.36	0.41	0.51
C	0.008	0.010	0.012	0.20	0.25	0.30
D	-	0.713	0.728	-	18.11	18.49
E	0.326	0.331	0.336	8.28	8.41	8.53
$\bar{e}$	0.044	0.050	0.056	1.12	1.27	1.42
H	0.453	0.465	0.477	11.51	11.81	12.12
L	0.028	0.036	0.044	0.71	0.91	1.12
L1	0.059	0.067	0.075	1.50	1.70	1.91
S	-	-	0.047	-	-	1.19
y	-	-	0.004	-	-	0.10
$\theta$	0°	-	8°	0°	-	8°

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

**Package Information**
**TSOP 28L TYPE I (8 X 13.4mm) Outline Dimensions**

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.049	-	-	1.25
A1	0.002	-	-	0.05	-	-
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.005	-	0.008	0.12	-	0.21
E	0.311	0.315	0.319	7.90	8.00	8.10
L	0.012	0.020	0.028	0.30	0.50	0.70
D	0.520	0.528	0.536	13.20	13.40	13.60
D1	0.461	0.465	0.469	11.70	11.80	11.90
[e]	0.022 BSC			0.55 BSC		
S	0.017 TYP			0.425 TYP		
y	-	-	0.004	-	-	0.10
θ	0°	-	5°	0°	-	5°

**Notes:**

1. The maximum value of dimension D<sub>1</sub> includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.