



Preliminary

A627308 Series

128K X 8 BIT CMOS SRAM

Document Title

128K X 8 BIT CMOS SRAM

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
0.0	Initial issue	August 15, 2000	Preliminary
0.1	Omit 100ns grade items Change I _{CC1} from 70mA to 45mA Change I _{SB1} from 25μA to 15μA	October 25, 2000	
0.2	Change I _{SB1} from 15μA to 25μA	February 6, 2001	



A627308 Series

128K X 8 BIT CMOS SRAM

Preliminary

Features

- Power supply range: 4.5V to 5.5V
- Access times: 70 ns (max.)
- Current:
 - Operating: 45mA (max.)
 - Standby: 25μA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL compatible

- Common I/O using three-state output
- Output enable and two chip enable inputs for easy application
- Data retention voltage: 2V (min.)
- Available in 32-pin SOP, TSOP, sTSOP (8X 13.4mm) forward type packages

General Description

The A627308 is a low operating current 1048,576-bit static random access memory organized as 131,072 words by 8 bits and operates on a power supply voltage from 4.5V to 5.5V.

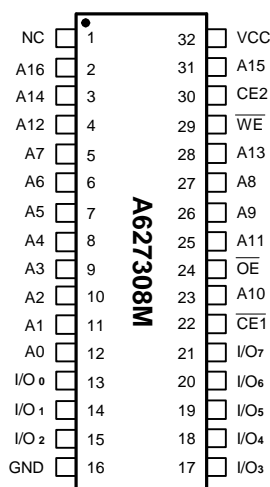
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Two chip enable inputs are provided for power down and a write enable and an output enable input are included for easy interfacing.

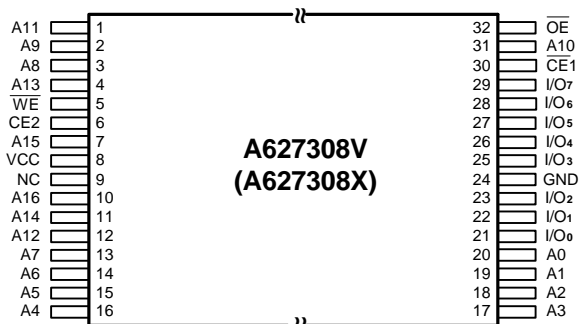
Data retention is guaranteed at a power supply voltage as low as 2V.

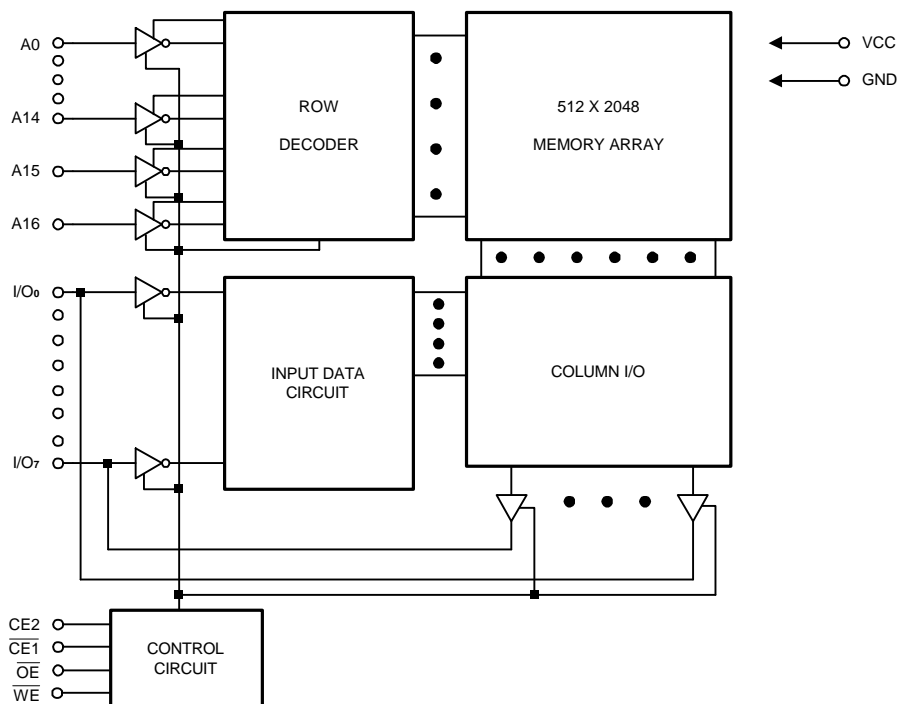
Pin Configurations

■ SOP



■ TSOP/(sTSOP) (forward type)



Block Diagram

Pin Descriptions - SOP

Pin No.	Symbol	Description
2 - 12, 23, 25 - 28, 31	A0 - A16	Address Inputs
13 - 15, 17 - 21	I/O ₀ - I/O ₇	Data Inputs/Outputs
22	$\overline{\text{CE1}}$	Chip Enable 1
30	CE2	Chip Enable 2
24	$\overline{\text{OE}}$	Output Enable
29	$\overline{\text{WE}}$	Write Enable
32	VCC	Power Supply
16	GND	Ground
1	NC	No Connection

Pin Description - TSOP/sTSOP

Pin No.	Symbol	Description
1 - 4, 7, 10 - 20, 31	A0 - A16	Address Inputs
21 - 23, 25 - 29	I/O ₀ - I/O ₇	Data Inputs/Outputs
30	$\overline{\text{CE1}}$	Chip Enable 1
6	CE2	Chip Enable 2
32	$\overline{\text{OE}}$	Output Enable
5	$\overline{\text{WE}}$	Write Enable
8	VCC	Power Supply
24	GND	Ground
9	NC	No Connection

Recommended DC Operating Conditions
 $(T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C})$

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	-	VCC + 0.5	V
V _{IL}	Input Low Voltage	-0.5	-	+0.8	V
C _L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

Absolute Maximum Ratings*

VCC to GND -0.5V to +7.0V
 IN, IN/OUT Volt to GND -0.5V to VCC + 0.5V
 Operating Temperature, Topr -25°C to +85°C
 Storage Temperature, Tstg -55°C to +125°C
 Power Dissipation, Pr 0.7W
 Soldering Temp. & Time 260°C, 10 sec

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics $(T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}, \text{VCC} = 5.0\text{V} \pm 10\%, \text{GND} = 0\text{V})$

Symbol	Parameter	A627308-70S		Unit	Conditions
		Min.	Max.		
I _{LI}	Input Leakage Current	-	1	μA	V _{IN} = GND to VCC
I _{LO}	Output Leakage Current	-	1	μA	$\overline{\text{CE1}} = V_{IH}$ or $\text{CE2} = V_{IL}$ or $\text{OE} = V_{IH}$ or $\overline{\text{WE}} = V_{IL}$ V _{IO} = GND to VCC
I _{CC}	Active Power Supply Current	-	7	mA	$\overline{\text{CE1}} = V_{IL}$, CE2 = V _{IH} I _{IO} = 0mA
I _{CC1}	Dynamic Operating Current	-	45	mA	Min. Cycle, Duty = 100% $\overline{\text{CE1}} = V_{IL}$, CE2 = V _{IH} I _{IO} = 0mA
I _{CC2}	Dynamic Operating Current	-	7	mA	$\overline{\text{CE1}} = V_{IL}$, CE2 = V _{IH} V _{IH} = VCC, V _{IL} = 0V F = 1MHz, I _{IO} = 0mA

DC Electrical Characteristics (continued)

Symbol	Parameter	A627308-70S		Unit	Conditions
		Min.	Max.		
I _{SB}	Standby Power Supply Current	-	0.5	mA	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$
I _{SB1}		-	25	μA	$CE2 \leq 0.2V$, or $\overline{CE1} \geq V_{CC} - 0.2V$
V _{OL}	Output Low Voltage	-	0.4	V	I _{OL} = 2.1mA
V _{OH}	Output High Voltage	2.4	-	V	I _{OH} = -1.0mA

Truth Table

Mode	$\overline{CE1}$	CE2	\overline{OE}	\overline{WE}	I/O Operation	Supply Current
Standby	H	X	X	X	High Z	I _{SB} , I _{SB1}
	X	L	X	X	High Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	H	High Z	I _{CC} , I _{CC1} , I _{CC2}
Read	L	H	L	H	D _{OUT}	I _{CC} , I _{CC1} , I _{CC2}
Write	L	H	X	L	D _{IN}	I _{CC} , I _{CC1} , I _{CC2}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C _{IN} *	Input Capacitance	-	6	pF	V _{IN} = 0V
C _{I/O} *	Input/Output Capacitance	-	8	pF	V _{I/O} = 0V

* These parameters are sampled and not 100% tested.

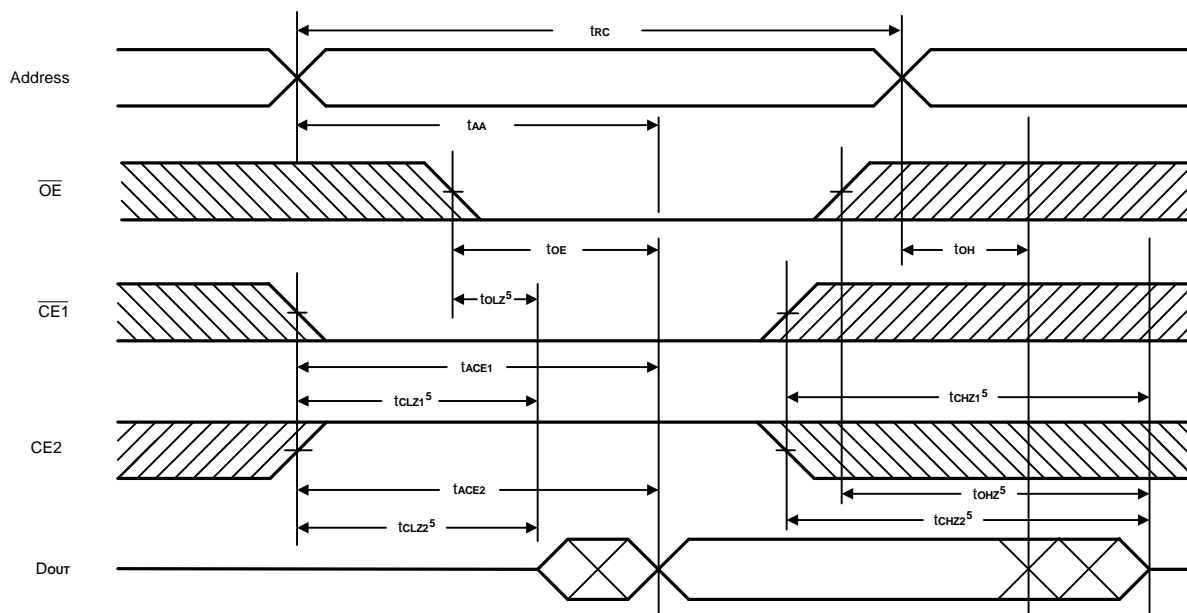
AC Characteristics ($T_A = 0^\circ\text{C}$ to $+70^\circ$, $V_{CC} = 5.0\text{V} \pm 10\%$)

Symbol	Parameter		A627308-70S		Unit
			Min.	Max.	
Read Cycle					
t _{RC}	Read Cycle Time		70	-	ns
t _{AA}	Address Access Time		-	70	ns
t _{ACE1}	Chip Enable Access Time	$\overline{CE1}$	-	70	ns
t _{ACE2}		CE2	-	70	ns
t _{OE}	Output Enable to Output Valid		-	35	ns
t _{CLZ1}	Chip Enable to Output in Low Z	$\overline{CE1}$	10	-	ns
t _{CLZ2}		CE2	10	-	ns
t _{OLZ}	Output Enable to Output in Low Z		5	-	ns
t _{CHZ1}	Chip Disable to Output in High Z	$\overline{CE1}$	0	25	ns
t _{CHZ2}		CE2	0	25	ns
t _{OHZ}	Output Disable to Output in High Z		0	25	ns
t _{OH}	Output Hold from Address Change		10	-	ns
Write Cycle					
t _{WC}	Write Cycle Time		70	-	ns
t _{CW}	Chip Enable to End of Write		60	-	ns
t _{AS}	Address Setup Time		0	-	ns
t _{AW}	Address Valid to End of Write		60	-	ns
t _{WP}	Write Pulse Width		50	-	ns
t _{WR}	Write Recovery Time		0	-	ns
t _{WHZ}	Write to Output in High Z		0	30	ns
t _{DW}	Data to Write Time Overlap		30	-	ns
t _{DH}	Data Hold from Write Time		0	-	ns
t _{OW}	Output Active from End of Write		5	-	ns

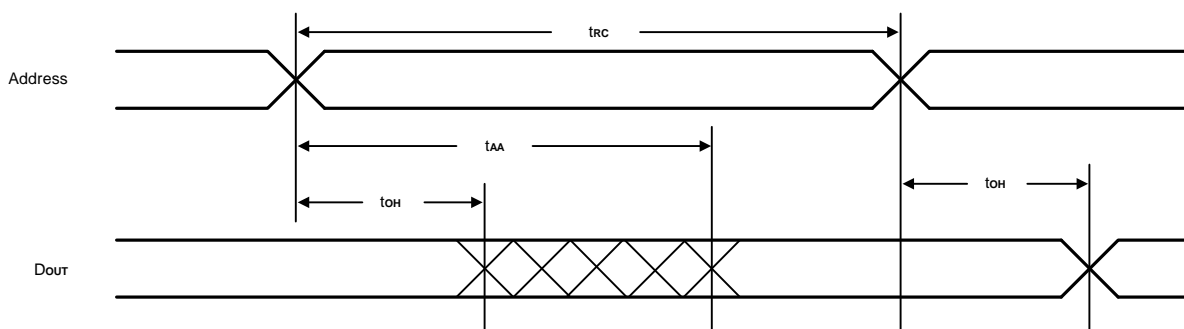
Notes: t_{CHZ1} , t_{CHZ2} , t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

Read Cycle 1⁽¹⁾

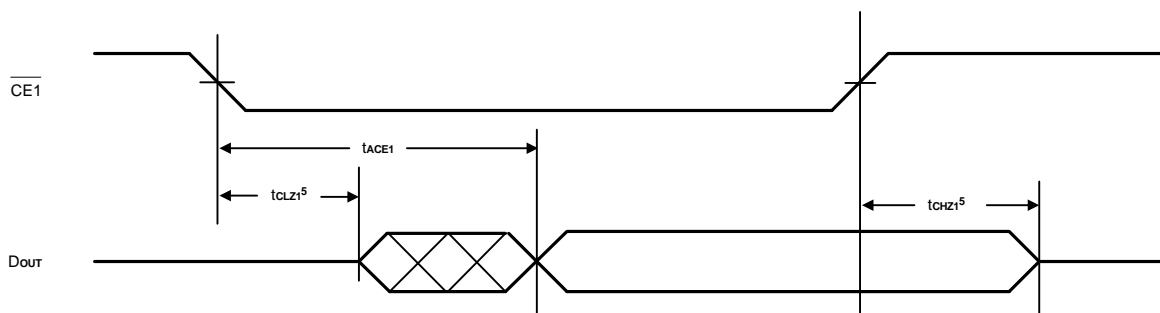


Read Cycle 2^(1, 2, 4)

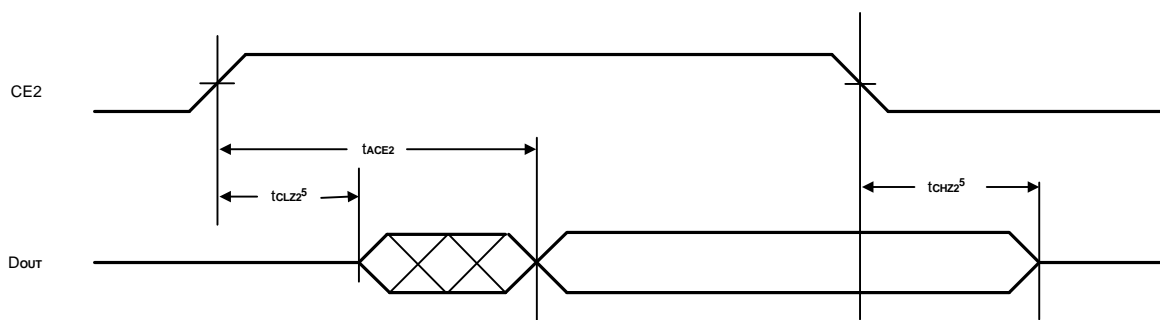


Timing Waveforms (continued)

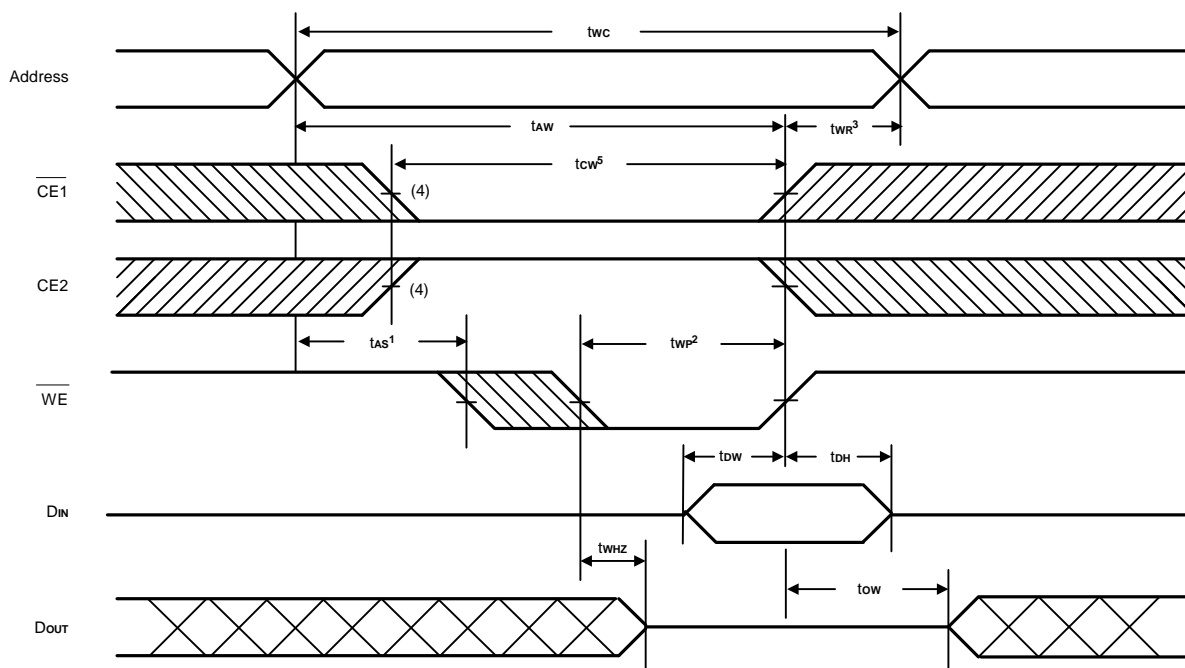
Read Cycle 3 (1, 3, 4, 6)



Read Cycle 4 (1, 4, 7, 8)

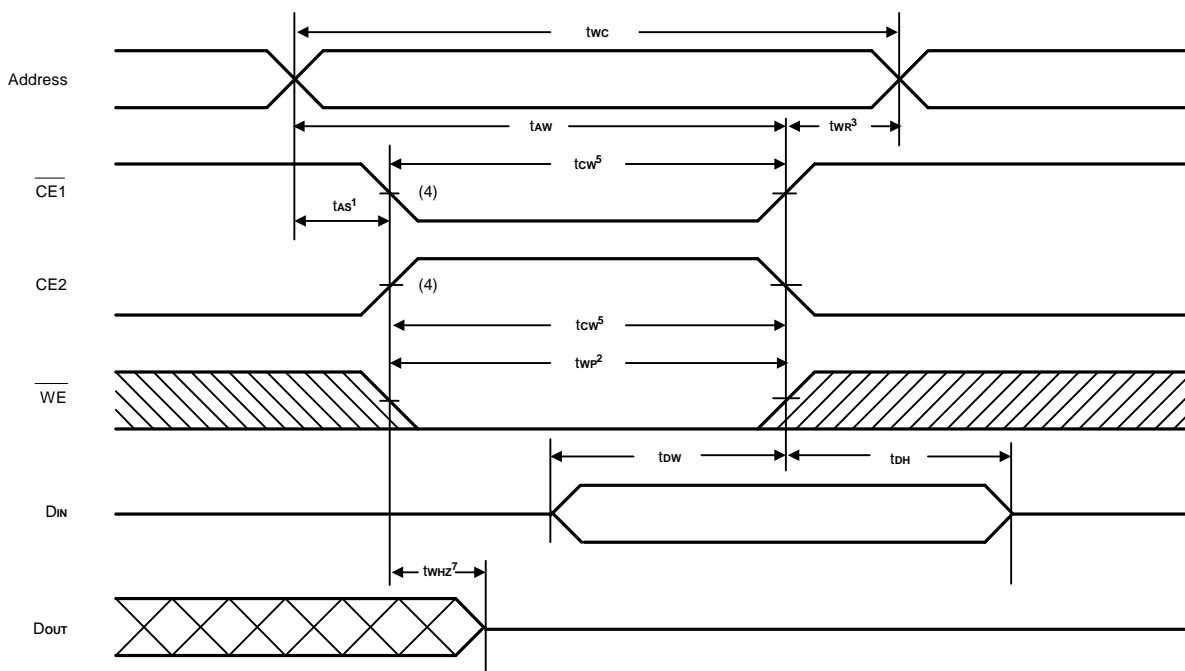


- Notes:
1. \overline{WE} is high for Read Cycle.
 2. Device is continuously enabled $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$.
 3. Address valid prior to or coincident with $\overline{CE1}$ transition low.
 4. $\overline{OE} = V_{IL}$.
 5. Transition is measured $\pm 500\text{mV}$ from steady state. This parameter is sampled and not 100% tested.
 6. $CE2$ is high.
 7. $\overline{CE1}$ is low.
 8. Address valid prior to or coincident with $CE2$ transition high.

Timing Waveforms (continued)
Write Cycle 1⁽⁶⁾
(Write Enable Controlled)


Timing Waveforms (continued)

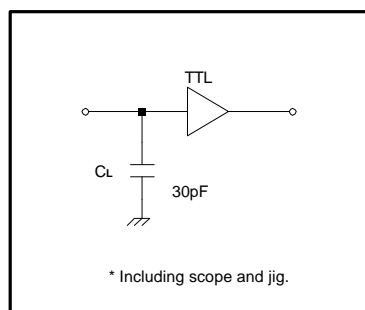
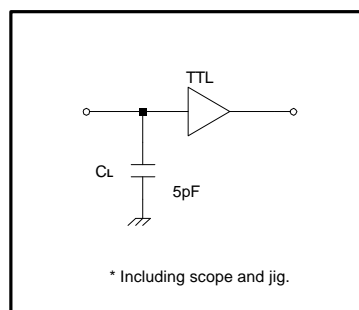
Write Cycle 2⁽⁶⁾ (Chip Enable Controlled)



- Notes:
1. t_{as} is measured from the address valid to the beginning of Write.
 2. A Write occurs during the overlap (t_{wp}) of a low $\overline{CE1}$, a high $CE2$ and a low \overline{WE} .
 3. t_{wr} is measured from the earliest of $\overline{CE1}$ or \overline{WE} going high or $CE2$ going low to the end of the Write cycle.
 4. If the $\overline{CE1}$ low transition or the $CE2$ high transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, outputs remain in a high impedance state.
 5. t_{cw} is measured from the later of $\overline{CE1}$ going low or $CE2$ going high to the end of Write.
 6. \overline{OE} is continuously low. ($\overline{OE} = V_{IL}$)
 7. Transition is measured $\pm 500\text{mV}$ from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

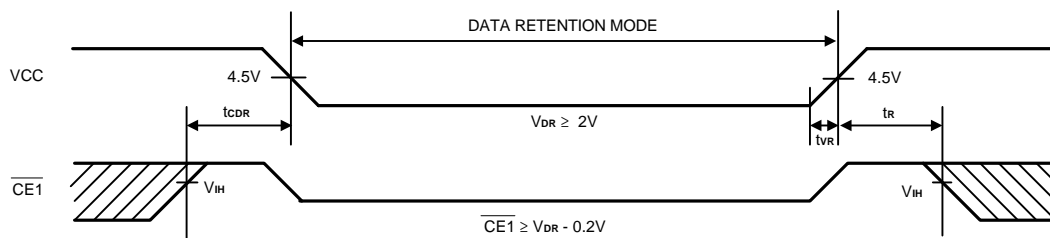
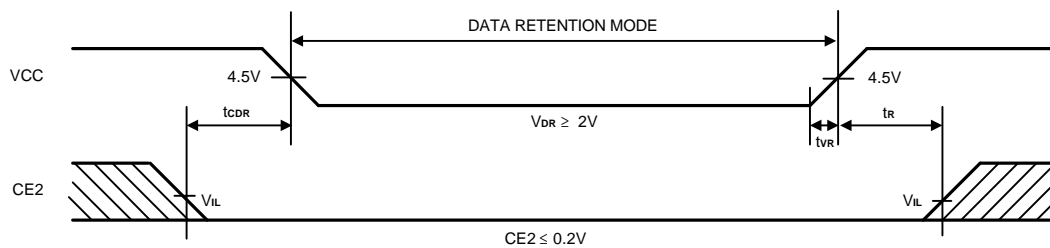
Input Pulse Levels	0V to 3V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2


Figure 1. Output Load

Figure 2. Output Load for tCLZ1, tCLZ2, tOHZ, tOLZ, tCHZ1, tCHZ2, tWHZ, and tOW
Data Retention Characteristics ($T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention	2.0	5.5	V	$CE2 \leq 0.2V$, or $\overline{CE1} \geq VCC - 0.2V$
I_{CCDR}	Data Retention Current	-	10*	μA	$VCC = 2.0V$, $CE2 \leq 0.2V$, or $\overline{CE1} \geq VCC - 0.2V$
t_{CDR}	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
t_R	Operation Recovery Time	t_{RC}	-	ns	
t_{VR}	VCC Rise Time from Data Retention Voltage to Operating Voltage	5	-	ms	

* A627308-70S

I_{CCDR} : Max. $3\mu A$ at $T_A = 0^{\circ}\text{C}$ to $+40^{\circ}\text{C}$

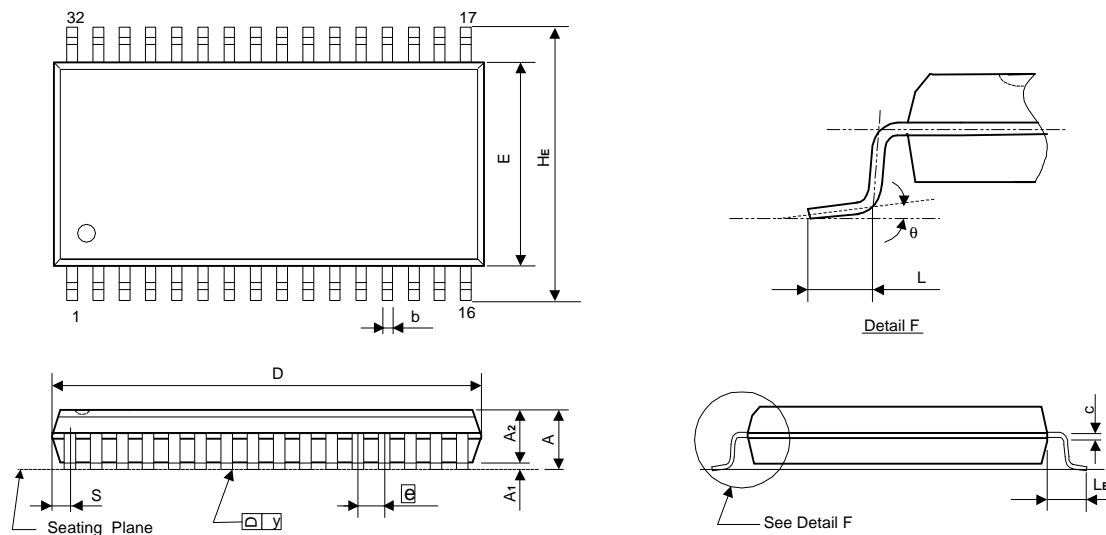
Low VCC Data Retention Waveform (1) ($\overline{\text{CE1}}$ Controlled)

Low VCC Data Retention Waveform (2) (CE2 Controlled)


**Ordering Information**

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (μA)	Package
A627308M-70S	70	45	25	32L SOP
A627308V-70S				32L TSOP
A627308X-70S				32L sTSOP

Package Information
SOP (W.B.) 32L Outline Dimensions

unit: inches/mm



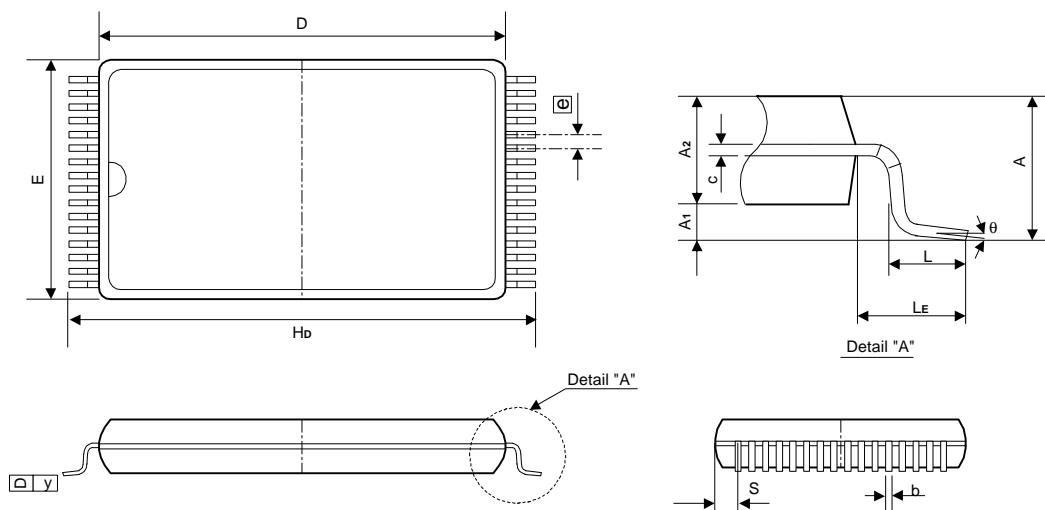
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.118	-	-	3.00
A1	0.004	-	-	0.10	-	-
A2	0.101	0.106	0.111	2.57	2.69	2.82
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.006	0.008	0.012	0.15	0.20	0.31
D	-	0.805	0.817	-	20.45	20.75
E	0.440	0.445	0.450	11.18	11.30	11.43
\bar{e}	0.044	0.050	0.056	1.12	1.27	1.42
HE	0.546	0.556	0.566	13.87	14.12	14.38
L	0.023	0.031	0.039	0.58	0.79	0.99
LE	0.047	0.055	0.063	1.19	1.40	1.60
S	-	-	0.036	-	-	0.91
y	-	-	0.004	-	-	0.10
θ	0°	-	10°	0°	-	10°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information
TSOP 32L TYPE I (8 X 20mm) Outline Dimensions

unit: inches/mm



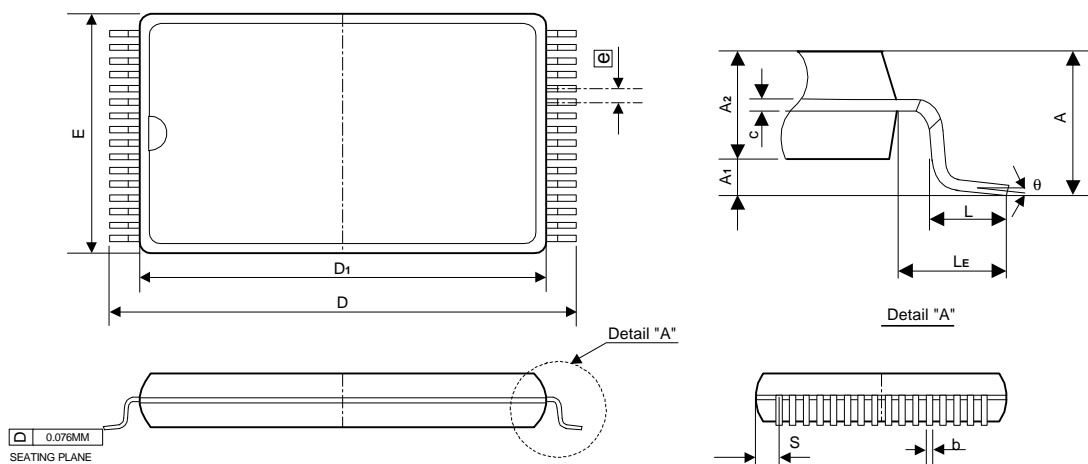
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A ₁	0.002	-	0.006	0.05	-	0.15
A ₂	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.18	0.22	0.27
c	0.004	-	0.008	0.11	-	0.20
D	0.720	0.724	0.728	18.30	18.40	18.50
E	-	0.315	0.319	-	8.00	8.10
\square e	0.020 BSC			0.50 BSC		
Hb	0.779	0.787	0.795	19.80	20.00	20.20
L	0.016	0.020	0.024	0.40	0.50	0.60
LE	-	0.032	-	-	0.80	-
S	-	-	0.020	-	-	0.50
y	-	-	0.003	-	-	0.08
θ	0°	-	5°	0°	-	5°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information
sTSOP 32L TYPE I (8 X 13.4mm) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.049	-	-	1.25
A1	0.002	-	-	0.05	-	-
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.0056	0.0059	0.0062	0.142	0.150	0.158
E	0.311	0.315	0.319	7.90	8.00	8.10
[e]	0.020 TYP			0.50 TYP		
D	0.520	0.528	0.535	13.20	13.40	13.60
D1	0.461	0.465	0.469	11.70	11.80	11.90
L	0.012	0.020	0.028	0.30	0.50	0.70
LE	0.0275	0.0315	0.0355	0.700	0.800	0.900
S	0.0109 TYP			0.278 TYP		
θ	0°	3°	5°	0°	3°	5°

Notes:

1. The maximum value of dimension D₁ includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.