



**A63L7336**

***Preliminary***      ***128K X 36 Bit Synchronous High Speed SRAM with  
Burst Counter and Pipelined Data Output***

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**Document Title**

**128K X 36 Bit Synchronous High Speed SRAM with Burst Counter and Pipelined  
Data Output**

**Revision History**

<b><u>Rev. No.</u></b>	<b><u>History</u></b>	<b><u>Issue Date</u></b>	<b><u>Remark</u></b>
0.0	Initial issue	July 11, 2005	Preliminary



# A63L7336

## ***128K X 36 Bit Synchronous High Speed SRAM with Preliminary Burst Counter and Pipelined Data Output***

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### **Features**

- Fast access times: 2.6/2.8/3.2/3.5/3.8/4.2 ns (250/227/200/166/150/133 MHz)
- Single +3.3V+10% or +3.3V-5% power supply
- Synchronous burst function
- Individual Byte Write control and Global Write
- Registered output for pipelined applications
- Three separate chip enables allow wide range of options for CE control, address pipelining
- Selectable BURST mode
- SLEEP mode (ZZ pin) provided
- Available in 100-pin LQFP package

### **General Description**

The A63L7336 is a high-speed SRAM containing 4.5M bits of bit synchronous memory, organized as 128K words by 36 bits.

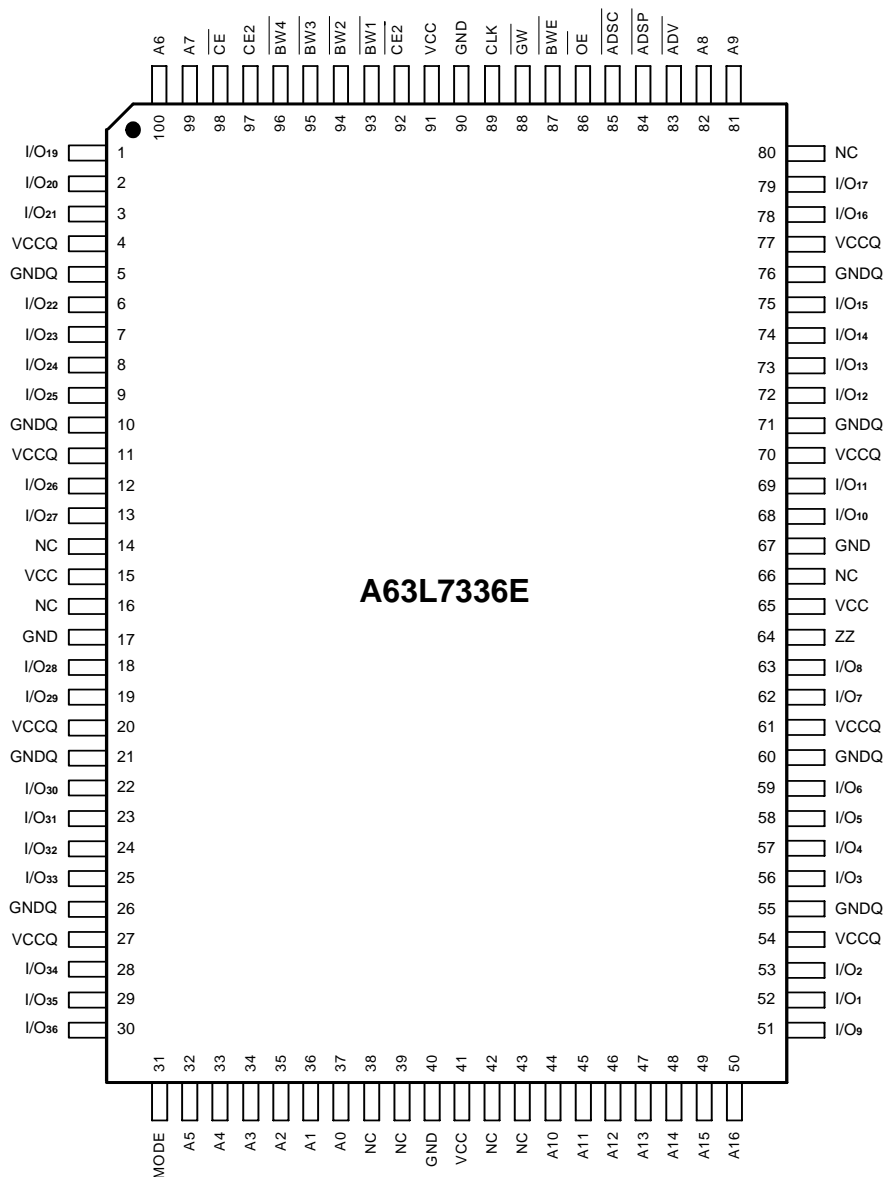
The A63L7336 combines advanced synchronous peripheral circuitry, 2-bit burst control, input registers, output registers and a 128KX36 SRAM core to provide a wide range of data RAM applications.

The positive edge triggered single clock input (CLK) controls all synchronous inputs passing through the registers. Synchronous inputs include all addresses (A0 - A16), all data inputs (I/O<sub>1</sub> - I/O<sub>36</sub>), active LOW chip enable ( $\overline{CE}$ ), two additional chip enables (CE2,  $\overline{CE2}$ ), burst control inputs ( $\overline{ADSC}$ ,  $\overline{ADSP}$ ,  $\overline{ADV}$ ), byte write enables ( $\overline{BWE}$ ,  $\overline{BW1}$ ,  $\overline{BW2}$ ,  $\overline{BW3}$ ,  $\overline{BW4}$ ) and Global Write ( $\overline{GW}$ ). Asynchronous inputs include output enable ( $\overline{OE}$ ), clock (CLK), BURST mode (MODE) and SLEEP mode (ZZ).

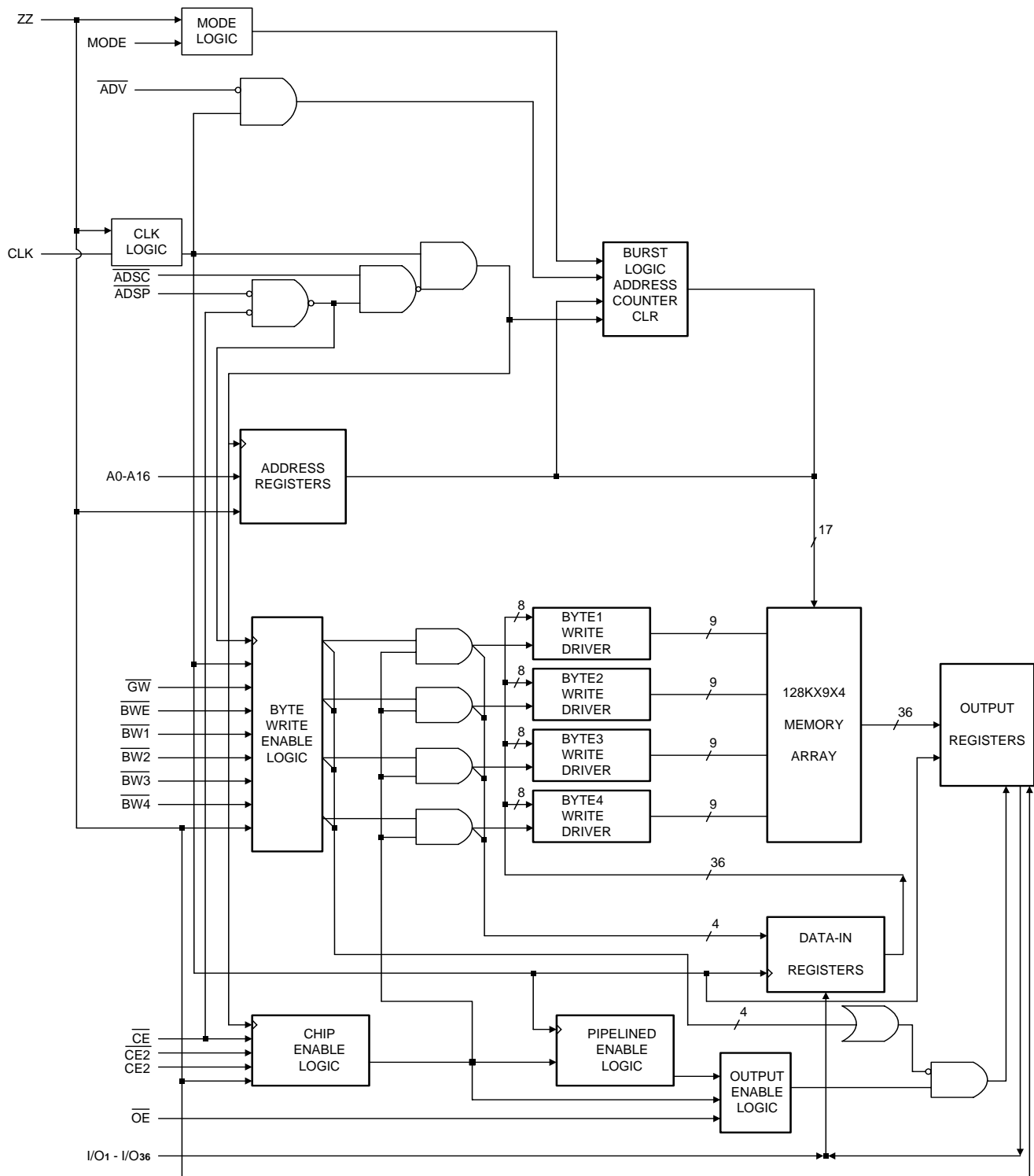
Burst operations can be initiated with either the address status processor ( $\overline{ADSP}$ ) or address status controller ( $\overline{ADSC}$ ) input pin. Subsequent burst sequence burst addresses can be internally generated by the A63L7336 and controlled by the burst advance ( $\overline{ADV}$ ) pin. Write cycles are internally self-timed and synchronous with the rising edge of the clock (CLK).

This feature simplifies the write interface. Individual Byte enables allow individual bytes to be written.  $\overline{BW1}$  controls I/O<sub>1</sub> - I/O<sub>9</sub>,  $\overline{BW2}$  controls I/O<sub>10</sub> - I/O<sub>18</sub>,  $\overline{BW3}$  controls I/O<sub>19</sub> - I/O<sub>27</sub>, and  $\overline{BW4}$  controls I/O<sub>28</sub> - I/O<sub>36</sub>, all on the condition that  $\overline{BWE}$  is LOW.  $\overline{GW}$  LOW causes all bytes to be written.

## Pin Configuration



## Block Diagram



**Pin Description**

Pin No.	Symbol	Description
32 – 37, 44 - 50, 81, 82, 99, 100	A0 - A17	Address Inputs
89	CLK	Clock
87, 93 - 96	$\overline{\text{BWE}}$ , $\overline{\text{BW1}}$ - $\overline{\text{BW4}}$	Byte Write Enables
88	$\overline{\text{GW}}$	Global Write
86	$\overline{\text{OE}}$	Output Enable
92, 97, 98	$\overline{\text{CE2}}$ , $\overline{\text{CE2}}$ , $\overline{\text{CE}}$	Chip Enables
83	$\overline{\text{ADV}}$	Burst Address Advance
84	$\overline{\text{ADSP}}$	Processor Address Status
85	$\overline{\text{ADSC}}$	Controller Address Status
31	MODE	Burst Mode: HIGH or NC (Interleaved burst) LOW (Linear burst)
64	ZZ	Asynchronous Power-Down (Snooze): HIGH (Sleep) LOW or NC (Wake up)
1,2, 3, 6 - 9, 12, 13, 18, 19, 22 - 25, 28, 29, 30,51,52, 53, 56 - 59, 62, 63, 68, 69, 72 - 75, 78, 79,80	I/O <sub>1</sub> - I/O <sub>36</sub>	Data Inputs/Outputs
15, 41, 65, 91	VCC	Power Supply
17, 40, 67, 90	GND	Ground
4, 11, 20, 27, 54, 61, 70, 77	VCCQ	Isolated Output Buffer Supply
5, 10, 21, 26, 55, 60, 71, 76	GNDQ	Isolated Output Buffer Ground

**Synchronous Truth Table (See Notes 1 Through 5)**

Operation	Address Used	$\overline{\text{CE}}$	$\overline{\text{CE2}}$	CE2	$\overline{\text{ADSP}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	$\overline{\text{WRITE}}$	$\overline{\text{OE}}$	CLK	I/O Operation
Deselected Cycle, Power-down	NONE	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	NONE	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	NONE	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	NONE	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	NONE	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Dout
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	Din
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Dout
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Dout
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Dout
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	Din
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	Din
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Dout
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Dout
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	Din
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	Din

Notes: 1. X = "Disregard", H = Logic High, L = Logic Low.

2.  $\overline{\text{WRITE}} = \text{L}$  means:

1) Any  $\overline{\text{BWx}}$  ( $\overline{\text{BW1}}$ ,  $\overline{\text{BW2}}$ ,  $\overline{\text{BW3}}$ , or  $\overline{\text{BW4}}$ ) and  $\overline{\text{BWE}}$  are low or

2)  $\overline{\text{GW}}$  is low.

3. All inputs except  $\overline{\text{OE}}$  must be synchronized with setup and hold times around the rising edge (L-H) of CLK.

4. For write cycles that follow read cycles,  $\overline{\text{OE}}$  must be HIGH before the input data request setup time and held HIGH throughout the input data hold time.

5. ADSP LOW always initiates an internal Read at the L-H edge of CLK. A Write is performed by setting one or more byte write enable signals and  $\overline{\text{BWE}}$  LOW or  $\overline{\text{GW}}$  LOW for the subsequent L-H edge of CLK. Refer to the Write timing diagram for clarification.

### Write Truth Table

Operation	$\overline{\text{GW}}$	$\overline{\text{BWE}}$	$\overline{\text{BW1}}$	$\overline{\text{BW2}}$	$\overline{\text{BW3}}$	$\overline{\text{BW4}}$
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE Byte 1	H	L	L	H	H	H
WRITE all bytes	H	L	L	L	L	L
WRITE all bytes	L	X	X	X	X	X

**Linear Burst Address Table (MODE = LOW)**

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X ... X00	X ... X01	X ... X10	X ... X11
X ... X01	X ... X10	X ... X11	X ... X00
X ... X10	X ... X11	X ... X00	X ... X01
X ... X11	X ... X00	X ... X01	X ... X10

**Interleaved Burst Address Table (MODE = HIGH or NC)**

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X ... X00	X ... X01	X ... X10	X ... X11
X ... X01	X ... X00	X ... X11	X ... X10
X ... X10	X ... X11	X ... X00	X ... X01
X ... X11	X ... X10	X ... X01	X ... X00

**Absolute Maximum Ratings\***

Power Supply Voltage (VCC) ..... -0.5V to +4.6V  
 Voltage Relative to GND for any Pin Except VCC (Vin, Vout) ..... -0.5V to VCC +0.5V  
 Power Dissipation (Pd) ..... 2W  
 Operating Temperature (Topr) ..... 0°C to 70°C  
 Storage Temperature (Tbias) ..... -10°C to 85 °C  
 Storage Temperature (Tstg) ..... -55°C to 125°C

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended DC Operating Conditions**

(0°C ≤ TA ≤ 70°C, VCC, VCCQ = 3.3V+10% or 3.3V-5%, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
VCC	Supply Voltage (Operating Voltage Range)	3.1	3.3	3.6	V	
VCCQ	Isolated Input Buffer Supply	3.1	3.3	VCC	V	
GND	Supply Voltage to GND	0.0	-	0.0	V	
VIH	Input High Voltage	2.0	-	VCC+0.3	V	1, 2
VIHQ	Input High Voltage (I/O Pins)	2.0	-	VCC+0.3	V	
VIL	Input Low Voltage	-0.3	-	0.8	V	1, 2



### DC Electrical Characteristics

(0°C ≤ T<sub>A</sub> ≤ 70°C, VCC, VCCQ = 3.3V+10% or 3.3V-5%, unless otherwise noted)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions	Note
I <sub>LI</sub>	Input Leakage Current	-	±2.0	μA	All inputs V <sub>IN</sub> = GND to VCC	
I <sub>LO</sub>	Output Leakage Current	-	±2.0	μA	$\overline{\text{OE}}$ = V <sub>IH</sub> , V <sub>out</sub> = GND to VCC	
I <sub>CC1</sub>	Supply Current	-	400	mA	Device selected; VCC = max. I <sub>out</sub> = 0mA, all inputs = V <sub>IH</sub> or V <sub>IL</sub> Cycle time = t <sub>kc</sub> min.	3, 11
I <sub>SB1</sub>	Standby Current	-	30	mA	Device deselected; VCC = max. All inputs are fixed. All inputs ≥ VCC - 0.2V or ≤ GND + 0.2V Cycle time = t <sub>kc</sub> min.	11
I <sub>SB2</sub>		-	15	mA	ZZ ≥ VCC - 0.2V	
V <sub>OL</sub>	Output Low Voltage	-	0.4	V	I <sub>OL</sub> = 8 mA	
V <sub>OH</sub>	Output High Voltage	2.4	-	V	I <sub>OH</sub> = -4 mA	

### Capacitance

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C <sub>IN</sub>	Input Capacitance	3	4	pF	T <sub>A</sub> = 25 °C; f = 1MHz VCC = 3.3V
C <sub>I/O</sub>	Input/Output Capacitance	4	5	pF	

\* These parameters are sampled and not 100% tested.

**AC Characteristics** ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 10\%$  or  $3.3\text{V} \pm 5\%$ )

Symbol	Parameter	-2.6		-2.8		-3.2		-3.5		-3.8		-4.2		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
t <sub>kc</sub>	Clock Cycle Time	4.0	-	4.4	-	5.0	-	6.0	-	6.7	-	7.5	-	ns	
t <sub>kH</sub>	Clock High Time	1.7	-	2.0	-	2.0	-	2.2	-	2.5	-	3.0	-	ns	
t <sub>kL</sub>	Clock Low Time	1.7	-	2.0	-	2.0	-	2.2	-	2.5	-	3.0	-	ns	
t <sub>kQ</sub>	Clock to Output Valid	-	2.6	-	2.8	-	3.2	-	3.5	-	3.8	-	4.2	ns	
t <sub>kQX</sub>	Clock to Output Invalid	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	ns	
t <sub>kQLZ</sub>	Clock to Output in Low-Z	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	ns	5, 6
t <sub>kQHZ</sub>	Clock to Output in High-Z	1.5	2.6	1.5	2.8	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.5	ns	5, 6
t <sub>OEQ</sub>	$\overline{\text{OE}}$ to Output Valid	-	2.6	-	2.8	-	3.2	-	3.5	-	3.8	-	4.2	ns	8
t <sub>OELZ</sub>	$\overline{\text{OE}}$ to Output in Low-Z	0	-	0	-	0	-	0	-	0	-	0	-	ns	5, 6
t <sub>OEHZ</sub>	$\overline{\text{OE}}$ to Output in High-Z	-	2.6	-	2.8	-	3.2	-	3.5	-	3.8	-	4.2	ns	5, 6
Setup Times															
t <sub>AS</sub>	Address	1.2	-	1.4	-	1.4	-	1.5	-	1.5	-	1.5	-	ns	7, 9
t <sub>ADSS</sub>	Address Status ( $\overline{\text{ADSC}}$ , $\overline{\text{ADSP}}$ )	1.2	-	1.4	-	1.4	-	1.5	-	1.5	-	1.5	-	ns	7, 9
t <sub>ADVS</sub>	Address Advance ( $\overline{\text{ADV}}$ )	1.2	-	1.4	-	1.4	-	1.5	-	1.5	-	1.5	-	ns	7, 9
t <sub>WS</sub>	Write Signals ( $\overline{\text{BW1}}$ , $\overline{\text{BW2}}$ , $\overline{\text{BW3}}$ , $\overline{\text{BW4}}$ , $\overline{\text{BWE}}$ , $\overline{\text{GW}}$ )	1.2	-	1.4	-	1.4	-	1.5	-	1.5	-	1.5	-	ns	7, 9
t <sub>DS</sub>	Data-in	1.2	-	1.4	-	1.4	-	1.5	-	1.5	-	1.5	-	ns	7, 9
t <sub>CES</sub>	Chip Enable ( $\overline{\text{CE}}$ , $\text{CE2}$ , $\overline{\text{CE2}}$ )	1.2	-	1.4	-	1.4	-	1.5	-	1.5	-	1.5	-	ns	7, 9

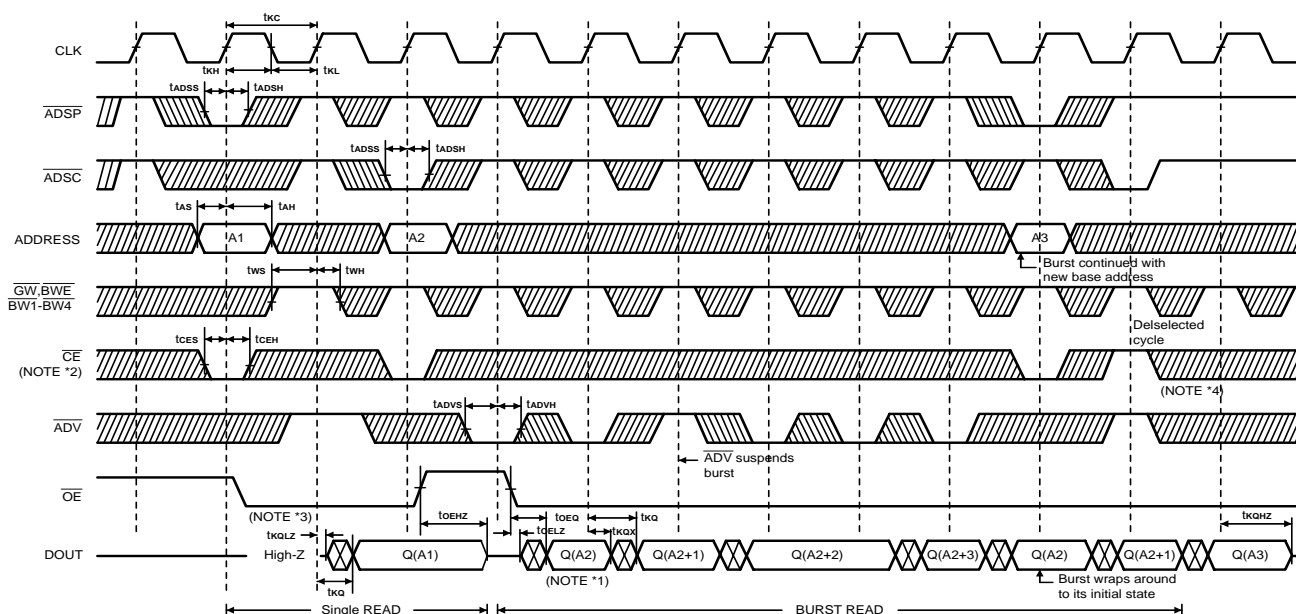
**AC Characteristics (continued)**

Symbol	Parameter	-2.6		-2.8		-3.2		-3.5		-3.8		-4.2		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min.	Max	Min	Max		
Hold Times															
t <sub>AH</sub>	Address	0.3	-	0.4	-	0.5	-	0.5	-	0.5	-	0.5	-	ns	7, 9
t <sub>ADVH</sub>	Address Status ( $\overline{\text{ADSC}}$ , $\overline{\text{ADSP}}$ )	0.3	-	0.4	-	0.5	-	0.5	-	0.5	-	0.5	-	ns	7, 9
t <sub>AAH</sub>	Address Advance ( $\overline{\text{ADV}}$ )	0.3	-	0.4	-	0.5	-	0.5	-	0.5	-	0.5	-	ns	7, 9
t <sub>WH</sub>	Write Signal ( $\overline{\text{BW1}}$ , $\overline{\text{BW2}}$ , $\overline{\text{BW3}}$ , $\overline{\text{BW4}}$ , $\overline{\text{BWE}}$ , $\overline{\text{GW}}$ )	0.3	-	0.4	-	0.5	-	0.5	-	0.5	-	0.5	-	ns	7, 9
t <sub>DH</sub>	Data-in	0.3	-	0.4	-	0.5	-	0.5	-	0.5	-	0.5	-	ns	7, 9
t <sub>CEH</sub>	Chip Enable ( $\overline{\text{CE}}$ , $\overline{\text{CE2}}$ , $\overline{\text{CE2}}$ )	0.3	-	0.4	-	0.5	-	0.5	-	0.5	-	0.5	-	ns	7, 9

**Notes:**

- All voltages refer to GND.
- Overshoot:  $V_{IH} \leq +4.6V$  for  $t \leq t_{kc}/2$ .  
Undershoot:  $V_{IH} \geq -0.7V$  for  $t \leq t_{kc}/2$ .  
Power-up:  $V_{IH} \leq +3.6$  and  $V_{CC} \leq 3.1V$   
for  $t \leq 200ms$
- I<sub>cc</sub> is given with no output current. I<sub>cc</sub> increases with greater output loading and faster cycle times.
- Test conditions assume the output loading shown in Figure 1, unless otherwise specified.
- For output loading, C<sub>L</sub> = 5pF, as shown in Figure 2. Transition is measured  $\pm 150mV$  from steady state voltage.
- At any given temperature and voltage condition, t<sub>KQHZ</sub> is less than t<sub>KQLZ</sub> and t<sub>OEHZ</sub> is less than t<sub>OEZ</sub>.
- A WRITE cycle is defined by at least one Byte Write enable LOW and  $\overline{\text{ADSP}}$  HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and ( $\overline{\text{ADSC}}$  or  $\overline{\text{ADV}}$  LOW) or  $\overline{\text{ADSP}}$  LOW for the required setup and hold times.
- $\overline{\text{OE}}$  has no effect when a Byte Write enable is sampled LOW.
- This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either  $\overline{\text{ADSP}}$  or  $\overline{\text{ADSC}}$  is LOW and the chip is enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when either  $\overline{\text{ADSP}}$  or  $\overline{\text{ADSC}}$  is LOW to remain enabled.
- The load used for V<sub>OH</sub>, V<sub>OL</sub> testing is shown in Figure 2. AC load current is higher than the given DC values. AC I/O curves are available upon request.
- "Device Deselected" means device is in POWER-DOWN mode, as defined in the truth table. "Device Selected" means device is active (not in POWER-DOWN mode).
- MODE pin has an internal pulled-up, and ZZ pin has an internal pulled-down. All of them exhibit an input leakage current of 10 $\mu A$ .
- Snooze (ZZ) input is recommended that users plan for four clock cycles to go into SLEEP mode and four clocks to emerge from SLEEP mode to ensure no data is lost.

## Timing Waveforms



## Read Timing

### Notes:

- \*1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the internal burst address immediately following A2.
- \*2. Timing for  $\overline{CE2}$  and CE2 is identical to that for  $\overline{CE}$ . As shown in this diagram, when  $\overline{CE}$  is LOW,  $\overline{CE2}$  is LOW and CE2 is HIGH. When  $\overline{CE}$  is HIGH,  $\overline{CE2}$  is HIGH and CE2 is LOW.
- \*3. Timing shown assumes that the device was not enabled before entering this sequence.  $\overline{OE}$  does not cause Q to be driven until after the rising edge of the following clock.



The timing diagram illustrates the relationship between various signals during three types of memory access: BURST READ, Single WRITE, and Extended BURST WRITE. The signals shown are CLK, ADSP, ADSC, ADDRESS, BWE, BW1-BW4 (NOTE \*5), GW, CE (NOTE \*2), ADV, OE, DIN, and DOUT.

Key timing parameters and annotations include:

- CLK:** Clock signal with parameters  $t_{KH}$ ,  $t_{KL}$ , and  $t_{KC}$ .
- ADSP:** Address Strobe Pulse with parameters  $t_{ADSS}$  and  $t_{ADSH}$ .
- ADSC:** Address Strobe Clock with parameters  $t_{ADSS}$  and  $t_{ADSH}$ .
- ADDRESS:** Address signal with parameters  $t_{AS}$  and  $t_{AH}$ . Annotations include "BYTE WRITE signals are ignored for first cycle when ADSP initiates burst" and "ADSC extends burst".
- BWE, BW1-BW4 (NOTE \*5):** Burst Write Enable signal with parameters  $t_{WS}$  and  $t_{WH}$ .
- GW:** Gate Write signal with parameters  $t_{WS}$  and  $t_{WH}$ .
- CE (NOTE \*2):** Chip Enable signal with parameters  $t_{CES}$  and  $t_{CEH}$ .
- ADV:** Address Valid signal with parameters  $t_{ADS}$  and  $t_{ADVH}$ . Annotations include "(NOTE \*4)" and "ADV suspends burst".
- OE:** Output Enable signal with parameters  $t_{DS}$  and  $t_{DH}$ . Annotations include "(NOTE \*3)".
- DIN:** Data In signal. Annotation: "High-Z".
- DOUT:** Data Out signal. Annotation: "High-Z".
- Data Access:** Data signals  $D(A)$ ,  $D(A+2)$ ,  $D(A+3)$ ,  $D(A+2)$ ,  $D(A+3)$ ,  $D(A+2)$ ,  $D(A+3)$ ,  $D(A+2)$ ,  $D(A+3)$ ,  $D(A+2)$ ,  $D(A+3)$ . Annotation: "(NOTE \*1)".

- \*2. Timing for  $\overline{\text{CE2}}$  and CE2 is identical to that for  $\overline{\text{CE}}$ . As shown in the above diagram, when  $\overline{\text{CE}}$  is LOW,  $\overline{\text{CE2}}$  is LOW and CE2 is HIGH. When  $\overline{\text{CE}}$  is HIGH,  $\overline{\text{CE2}}$  is HIGH and CE2 is LOW.
- \*3.  $\overline{\text{OE}}$  must be HIGH before the input data setup, and held HIGH throughout the data hold period. This prevents input/output data contention for the period prior to the time Byte Write enable inputs are sampled.
- \*4.  $\overline{\text{ADV}}$  must be HIGH to permit a Write to the loaded address.
- \*5. Byte Write enables are decided by means of a Write truth table.



The timing diagram illustrates the relationship between several signals and their timing parameters:

- CLK**: Clock signal with parameters  $t_{kc}$  (clock period),  $t_{KH}$  (clock high pulse width), and  $t_{KL}$  (clock low pulse width).
- ADSP**: Address Strobe Pulse with parameters  $t_{ADSS}$  (setup time) and  $t_{ADSH}$  (hold time).
- ADSC**: Address Strobe Clock.
- ADDRESS**: Address bus signals A1 through A6 with setup time  $t_{AS}$  and hold time  $t_{AH}$ .
- GW, BWE, BW1-BW4**: Data bus enable signals with setup time  $t_{WS}$  and hold time  $t_{WH}$ .
- CE**: Chip Enable with setup time  $t_{CES}$  and hold time  $t_{CEH}$ .
- ADV**: Address Valid signal.
- OE**: Output Enable.
- DIN**: Data Input, shown as High-Z and data D(A3), D(A5), and D(A6).
- DOUT**: Data Output, shown as High-Z and data Q(A1), Q(A2), Q(A3), Q(A4), Q(A4+1), Q(A4+2), and Q(A4+3).

Timing parameters for the data bus are also specified:

- $t_{KQ}$ : Delay from OE to output data.
- $t_{DS}$  and  $t_{DH}$ : Setup and hold times for data input D(A3).
- $t_{OELZ}$ : Delay from OE to output data becoming high-Z.
- $t_{KQLZ}$ : Delay from OE to output data becoming high-Z.
- $t_{OEZ}$ : Delay from OE to output data becoming high-Z.

The diagram is divided into four main sections:

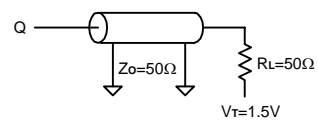
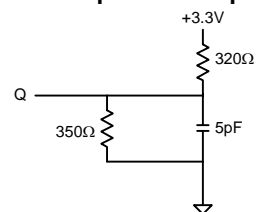
- Back-to-Back READS**: Shows two consecutive read operations.
- Single WRITE**: Shows a single write operation.
- Pass-through READ (NOTE \*4)**: Shows a read operation where the data is passed through the output.
- BURST READ**: Shows a burst of read operations.
- Back-to-Back WRITES**: Shows two consecutive write operations.

Notes:

- \*1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from the internal burst address immediately following A4.
- \*2. Timing for  $\overline{\text{CE2}}$  and CE2 is identical to that for  $\overline{\text{CE}}$ . As shown in this diagram, when  $\overline{\text{CE}}$  is LOW,  $\overline{\text{CE2}}$  is LOW and CE2 is HIGH. When  $\overline{\text{CE}}$  is HIGH,  $\overline{\text{CE2}}$  is HIGH and CE2 is LOW.
- \*3. Byte Write enables are decided by means of a Write truth table.
- \*4. Pass-through occurs when data is first written, then Read in sequence.

**AC Test Conditions**

Input Pulse Levels	GND to 3V
Input Rise and Fall Times	1.5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2


**Figure 1. Output Load Equivalent**

**Figure 2. Output Load Equivalent**

**Ordering Information**

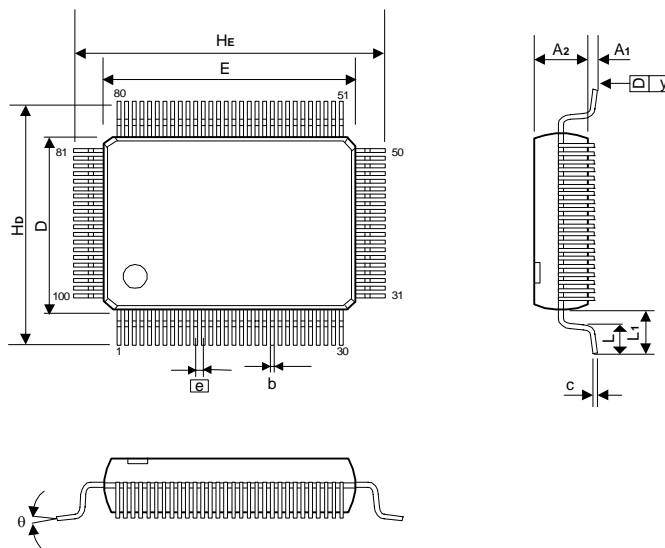
Part No.	Access Times (ns)	Frequency (MHz)	Package
A63L7336E-2.6	2.6	250	100L LQFP
A63L7336E-2.6F	2.6	250	100L Pb-Free LQFP
A63L7336E-2.8	2.8	225	100L LQFP
A63L7336E-2.8F	2.8	225	100L Pb-Free LQFP
A63L7336E-3.2	3.2	200	100L LQFP
A63L7336E-3.2F	3.2	200	100L Pb-Free LQFP
A63L7336E-3.5	3.5	166	100L LQFP
A63L7336E-3.5F	3.5	166	100L Pb-Free LQFP
A63L7336E-3.8	3.8	150	100L LQFP
A63L7336E-3.8F	3.8	150	100L Pb-Free LQFP
A63L7336E-4.2	4.2	133	100L LQFP
A63L7336E-4.2F	4.2	133	100L Pb-Free LQFP



## Package Information

### LQFP 100L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A1	0.002	-	-	0.05	-	-
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.011	0.013	0.015	0.27	0.32	0.37
c	0.005	-	0.008	0.12	-	0.20
HE	0.860	0.866	0.872	21.85	22.00	22.15
E	0.783	0.787	0.791	19.90	20.00	20.10
Hb	0.624	0.630	0.636	15.85	16.00	16.15
D	0.547	0.551	0.555	13.90	14.00	14.10
[e]	0.026 BSC			0.65 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	0.039 REF			1.00 REF		
y	-	-	0.004	-	-	0.1
theta	0°	3.5°	7°	0°	3.5°	7°

#### Notes:

- Dimensions D and E do not include mold protrusion.
- Dimensions b does not include dambar protrusion.  
Total in excess of the b dimension at maximum material condition.  
Dambar cannot be located on the lower radius of the foot.