

**AMIC**

***LP61L1008 Series***

***128K X 8 BIT 3.3V HIGH SPEED CENTER POWER CMOS SRAM***

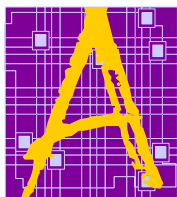
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**Document Title**

**128K X 8 BIT 3.3V HIGH SPEED CENTER POWER CMOS SRAM**

**Revision History**

<b><u>Rev. No.</u></b>	<b><u>History</u></b>	<b><u>Issue Date</u></b>	<b><u>Remark</u></b>
2.0	Add Product Family and 32-pin sTSP (Type I) package	June 11, 2002	

**AMIC**

## LP61L1008 Series

### 128K X 8 BIT 3.3V HIGH SPEED CENTER POWER CMOS SRAM

#### Features

- Single 3.3V  $\pm$  10% power supply
- Access times: 12/15 ns (max.)
- Current: Operating: 180mA (max.)  
Standby: 5mA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL compatible
- Center Power/Ground Pin Configuration
- Common I/O using three-state output
- Output enable and two chip enable inputs for easy application
- Data retention voltage: 2.0V (min.)
- Available in 32-pin SOJ 300 mil and 32-pin sTSOP packages

#### General Description

The LP61L1008 is a high speed 1,048,576-bit static random access memory organized as 131,072 words by 8 bits and operates on a single 3.3V power supply.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

The chip enable input is provided for POWER-DOWN and device enable and an output enable input is included for easy interfacing.

Data retention is guaranteed at a power supply voltage as low as 2.0V.

#### Product Family

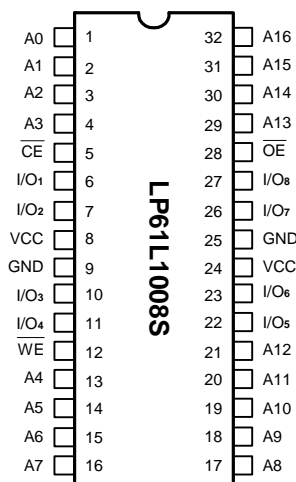
Product Family	Operating Temperature	VCC Range	Speed	Power Dissipation			Package Type
				Data Retention (I <sub>CCDR</sub> , Typ.)	Standby (I <sub>SB1</sub> , Typ.)	Operating (I <sub>CC2</sub> , Typ.)	
LP61L1008	0°C~70°C	3.0V~3.6V	12/15 ns	10 $\mu$ A	20 $\mu$ A	66mA	32L SOJ 32L sTSOP

1. Typical values are measured at VCC = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

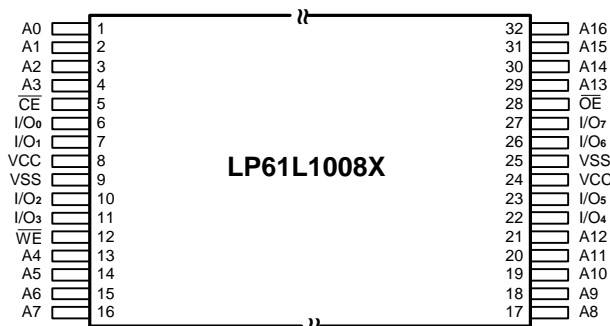
2. Data retention current VCC = 2.0V.

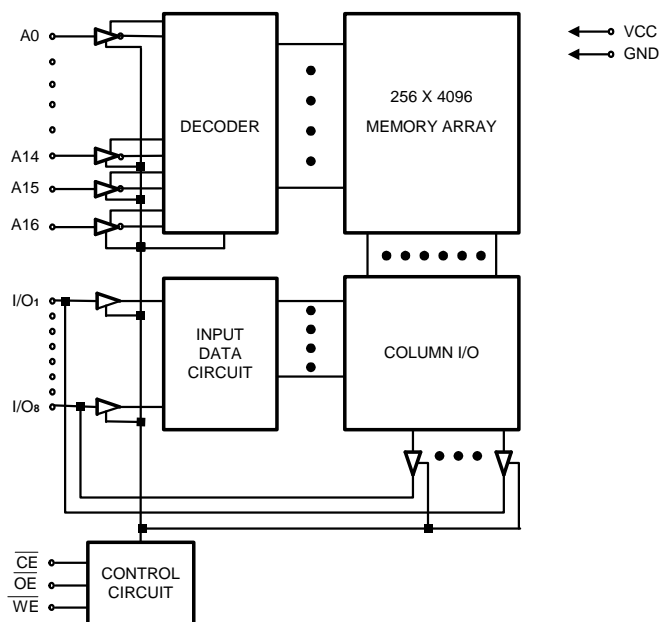
#### Pin Configuration

##### ■ SOJ



##### ■ sTSOP



**Block Diagram**

**Pin Description**

Pin No.	Symbol	Description
1 - 4, 13 - 21, 29- 32	A0 - A16	Address Inputs
12	$\overline{WE}$	Write Enable
28	$\overline{OE}$	Output Enable
5	$\overline{CE}$	Chip Enable
6 -7, 10 - 11, 22 - 23, 26 - 27	I/O <sub>1</sub> - I/O <sub>8</sub>	Data Input/Outputs
8, 24	VCC	Power Supply
9, 25	GND	Ground

**Recommended DC Operating Conditions**

(T<sub>A</sub> = 0°C to +70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	3.0	3.3	3.6	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	-	VCC + 0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	0	+0.8	V
C <sub>L</sub>	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

**Absolute Maximum Ratings\***

VCC to GND ..... -0.5V to +4.6V  
IN, IN/OUT Volt to GND ..... -0.5V to VCC +0.5V  
Operating Temperature, T<sub>opr</sub> ..... 0°C to +70°C  
Storage Temperature, T<sub>stg</sub> ..... -55°C to +125°C  
Temperature Under Bias, T<sub>bias</sub> ..... -10°C to +85°C  
Power Dissipation, P<sub>t</sub> ..... 1.0W  
Soldering Temp. & Time ..... 260°C, 10 sec

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics** (T<sub>A</sub> = 0°C to +70°C, VCC = 3.3V ± 10%, GND = 0V)

Symbol	Parameter	LP61L1008-12/15		Unit	Conditions
		Min.	Max.		
I <sub>LI</sub>	Input Leakage Current	-	2	μA	V <sub>IN</sub> = GND to VCC
I <sub>LO</sub>	Output Leakage Current	-	2	μA	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V <sub>I/O</sub> = GND to VCC
I <sub>CC1</sub> (1)	Dynamic Operating Current	-12	180	mA	$\overline{CE} = V_{IL}$ I <sub>I/O</sub> = 0 mA
		-15	170		
I <sub>SB</sub>	Standby Power Supply Current	-	20	mA	$\overline{CE} = V_{IH}$
I <sub>SB1</sub>		-	5	mA	$\overline{CE} \geq VCC - 0.2V$ , V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≥ VCC - 0.2V
V <sub>OL</sub>	Output Low Voltage	-	0.4	V	I <sub>OL</sub> = 8 mA
V <sub>OH</sub>	Output High Voltage	2.4	-	V	I <sub>OH</sub> = -4 mA

Note: 1. I<sub>CC1</sub> is dependent on output loading, cycle rates, and Read / Write patterns.

**Truth Table**

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	High Z	$I_{SB}, I_{SB1}$
Output Disable	L	H	H	High Z	$I_{CC1}$
Read	L	L	H	D <sub>OUT</sub>	$I_{CC1}$
Write	L	X	L	D <sub>IN</sub>	$I_{CC1}$

Note: X = H or L

**Capacitance** ( $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ )

Symbol	Parameter	Min.	Max.	Unit	Conditions
$C_{IN}^*$	Input Capacitance		8	pF	$V_{IN} = 0V$
$C_{IO}^*$	Input/Output Capacitance		10	pF	$V_{IO} = 0V$

\* These parameters are sampled and not 100% tested.

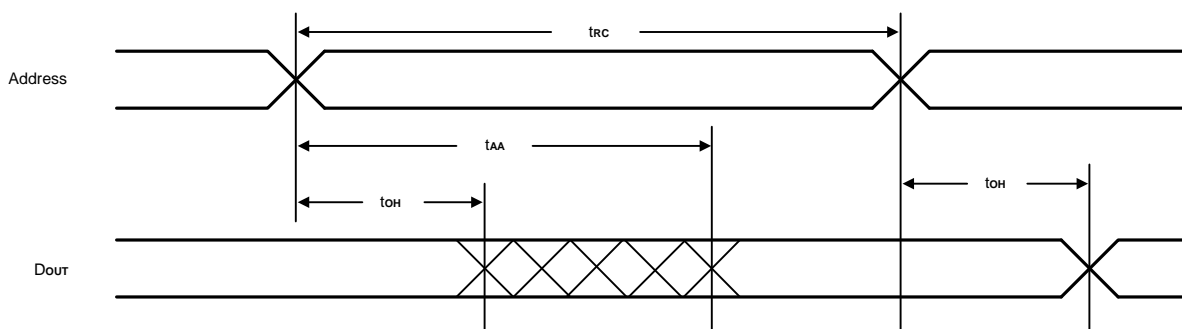
**AC Characteristics** ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3V \pm 10\%$ ,  $GND = 0V$ )

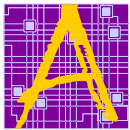
Symbol	Parameter		LP61L1008-12		LP61L1008-15		Unit
			Min.	Max.	Min.	Max.	
Read Cycle							
trc	Read Cycle Time		12	-	15	-	ns
tAA	Address Access Time		-	12	-	15	ns
tACE	Chip Enable Access Time	$\overline{CE}$	-	12	-	15	ns
toE	Output Enable to Output Valid		-	7	-	9	ns
tCLZ	Chip Enable to Output in Low Z	$\overline{CE}$	3	-	5	-	ns
toLZ	Output Enable to Output in Low Z		2	-	2	-	ns
tCHZ	Chip Disable to Output in High Z	$\overline{CE}$	-	7	-	10	ns
toHZ	Output Disable to Output in High Z		2	7	2	9	ns
toH	Output Hold from Address Change		2	-	5	-	ns

**AC Characteristics (continued)**

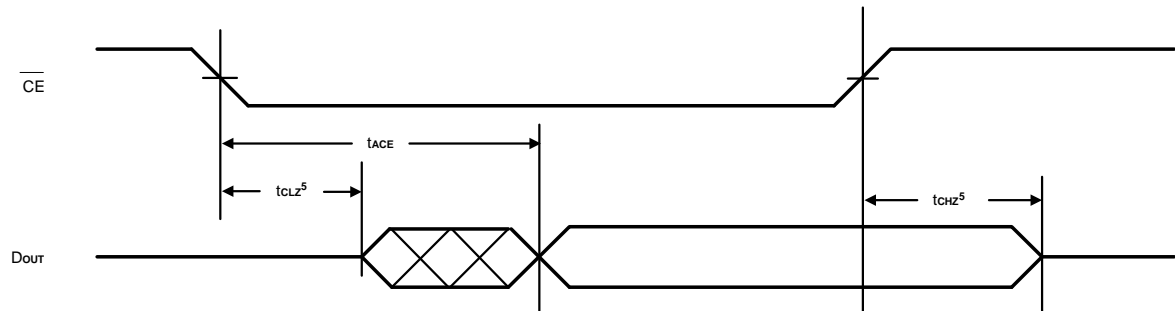
Symbol	Parameter	LP61L1008-12		LP61L1008-15		Unit
		Min.	Max.	Min.	Max.	
Write Cycle						
twc	Write Cycle Time	12	-	15	-	ns
tcw	Chip Enable to End of Write	10	-	12	-	ns
tas	Address Setup Time of Write	0	-	0	-	ns
taw	Address Valid to End of Write	10	-	12	-	ns
twp	Write Pulse Width	8	-	10	-	ns
twr	Write Recovery Time	0	-	0	-	ns
twhz	Write to Output in High Z	0	7	0	8	ns
tdw	Data to Write Time Overlap	8	-	10	-	ns
tdh	Data Hold from Write Time	0	-	0	-	ns
tow	Output Active from End of Write	5	-	5	-	ns

Notes: t<sub>chz1</sub>, t<sub>chz2</sub>, t<sub>ohz</sub>, and t<sub>whz</sub> are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

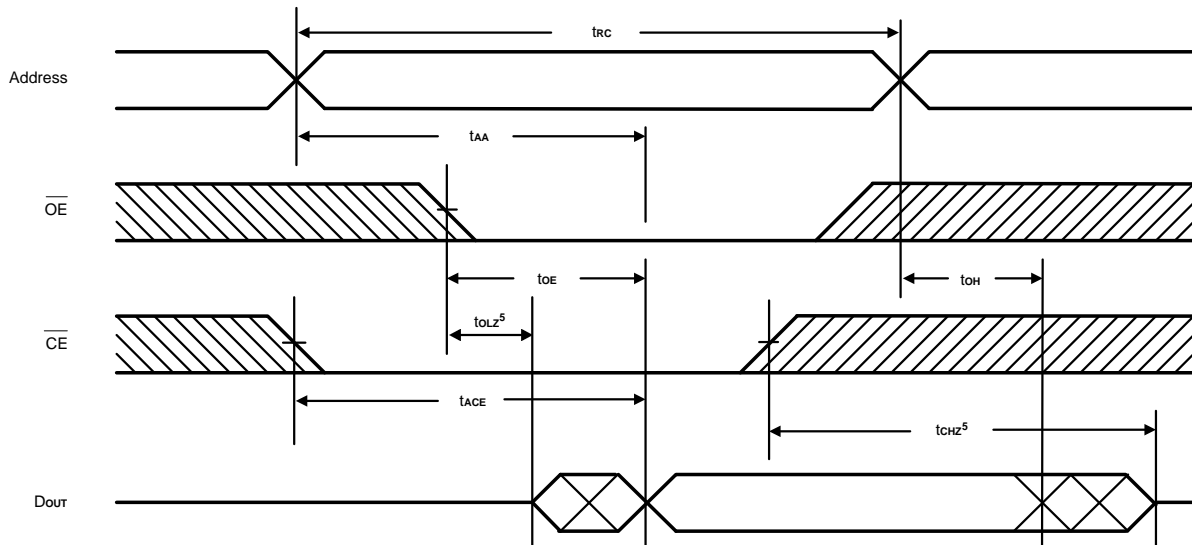
**Timing Waveforms**
**Read Cycle 1<sup>(1, 2, 4)</sup>**




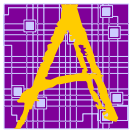
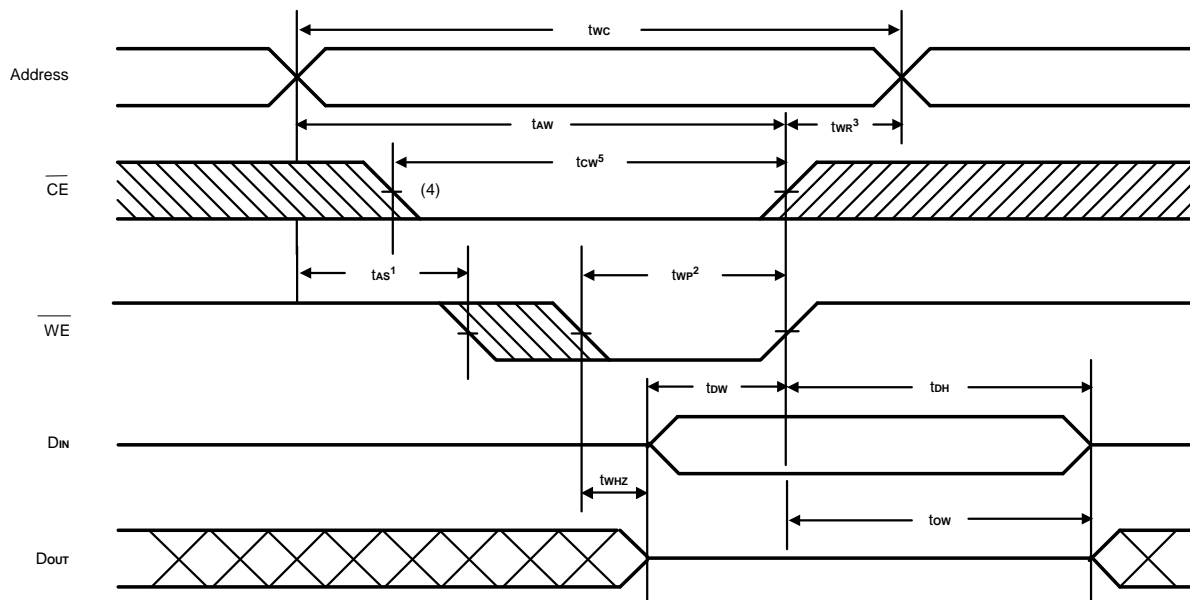
**Read Cycle 2<sup>(1, 3, 4, 6)</sup>**



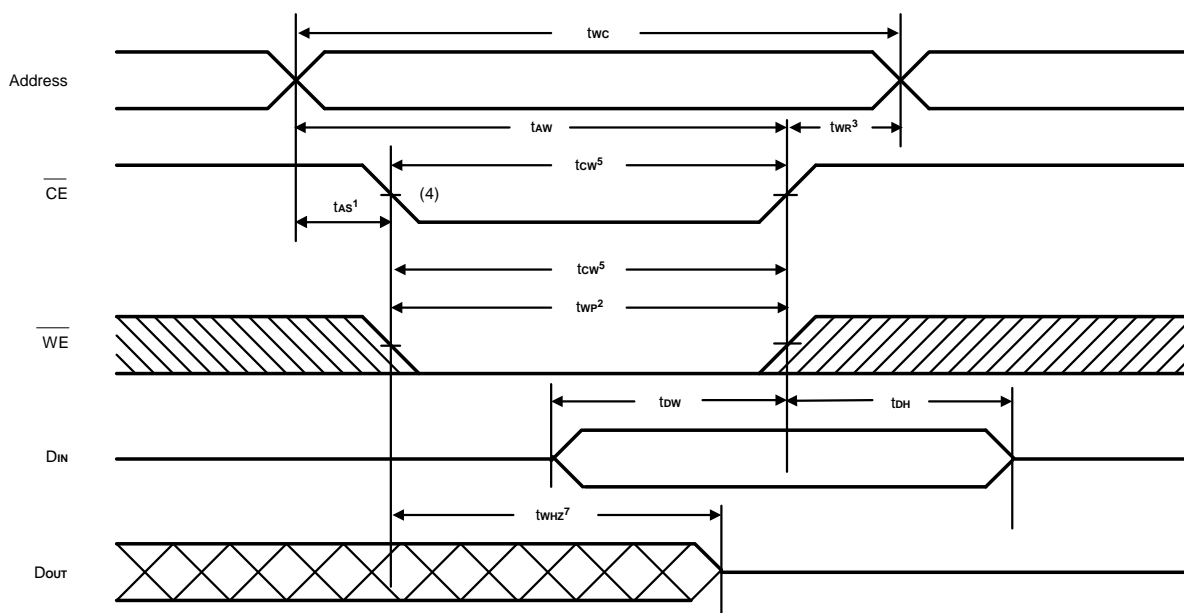
**Read Cycle 3<sup>(1)</sup>**



- Notes:
1.  $\overline{WE}$  is high for Read Cycle.
  2. Device is continuously enabled  $\overline{CE} = V_L$ .
  3. Address valid prior to or coincident with  $\overline{CE}$  transition low.
  4.  $\overline{OE} = V_{IL}$ .
  5. Transition is measured  $\pm 500\text{mV}$  from steady state. This parameter is sampled and not 100% tested.

**Timing Waveforms (continued)****Write Cycle 1<sup>(6)</sup>  
(Write Enable Controlled)**

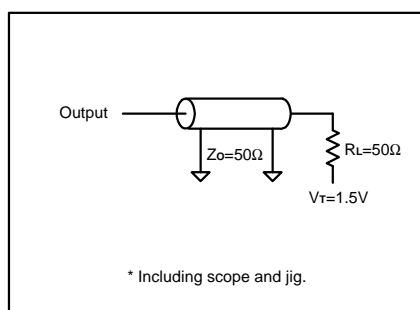
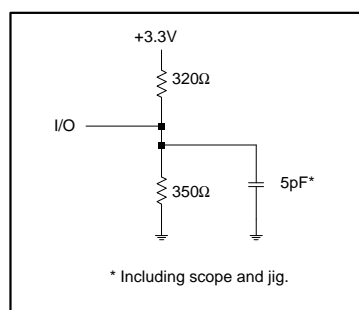


**Timing Waveforms (continued)**
**Write Cycle 2  
(Chip Enable Controlled)**


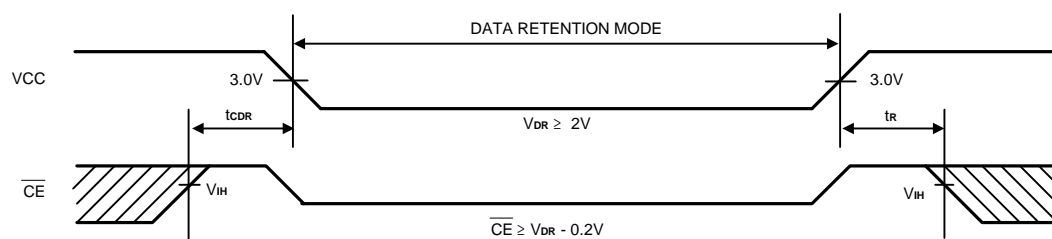
- Notes:
1.  $t_{as}$  is measured from the address valid to the beginning of Write.
  2. A Write occurs during the overlap ( $t_{wp}$ ) of a low  $\overline{CE}$  and a low  $\overline{WE}$ .
  3.  $t_{wr}$  is measured from the earliest of  $\overline{CE}$  or  $\overline{WE}$  going high to the end of the Write cycle.
  4. If the  $\overline{CE}$  low transition with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, outputs remain in a high impedance state.
  5.  $t_{cw}$  is measured from the later of  $\overline{CE}$  going low to the end of Write.
  6.  $\overline{OE}$  is continuously low. ( $\overline{OE} = V_{IL}$ )
  7. Transition is measured  $\pm 500\text{mV}$  from steady state. This parameter is sampled and not 100% tested.

**AC Test Conditions**

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2


**Figure 1. Output Load**

**Figure 2. Output Load for  $t_{CLZ}$ ,  $t_{OHZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{WHZ}$ , and  $t_{OW}$** 
**Data Retention Characteristics** ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

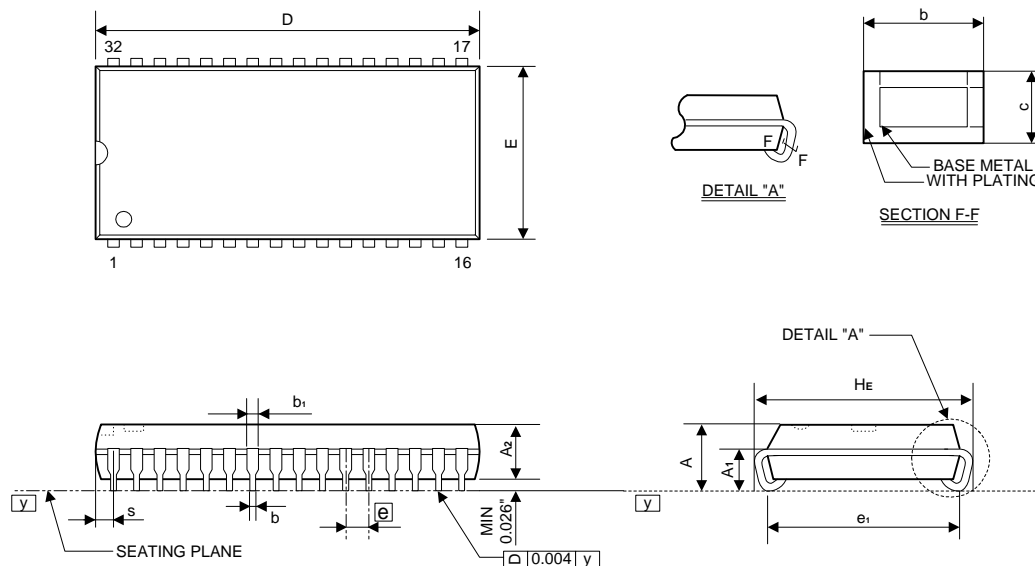
Symbol	Parameter	Min.	Max.	Unit	Conditions
$V_{DR1}$	VCC for Data Retention	2	3.6	V	$\overline{CE} \geq V_{CC} - 0.2V$
$I_{CCDR1}$	Data Retention Current	-	5	mA	$V_{CC} = 3.0V$ $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$
$t_{CDR}$	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
$t_R$	Operation Recovery Time	5	-	ms	

**Low VCC Data Retention Waveform ( $\overline{\text{CE}}$  Controlled)**

**Ordering Information**

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
LP61L1008S-12	12	180	5	32L SOJ (300 mil)
LP61L1008X-12	12	180	5	32L sTSOP (Type I)
LP61L1008S-15	15	170	5	32L SOJ (300 mil)
LP61L1008X-15	15	170	5	32L sTSOP (Type I)

**Package Information**
**SOJ 32/32LD (300mil BODY) Outline Dimensions**

unit: inches/mm



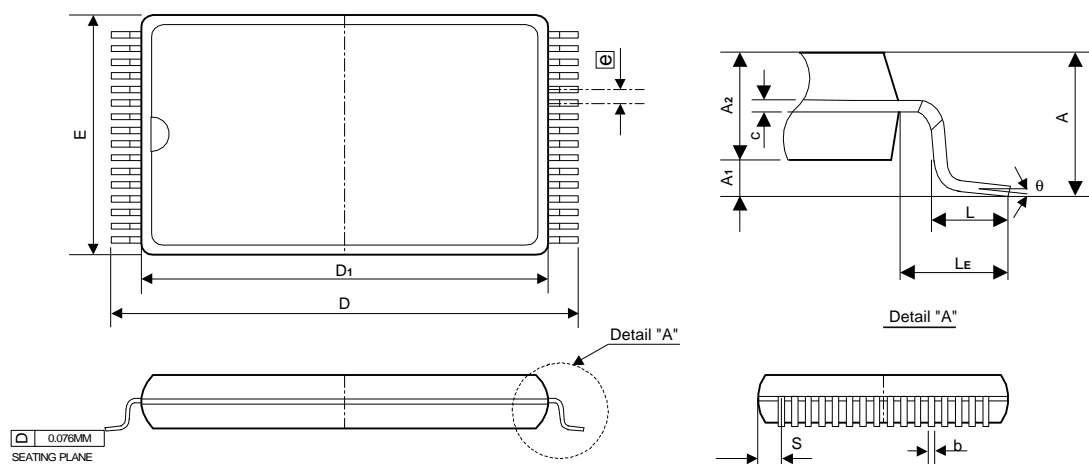
Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.128	0.132	0.140	3.25	3.35	3.56
A <sub>1</sub>	0.052	-	-	2.08	-	-
A <sub>2</sub>	0.095	0.100	0.105	2.41	2.54	2.67
b	0.016	0.018	0.020	0.41	0.46	0.51
b <sub>1</sub>	0.026	0.028	0.032	0.66	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.820	0.825	0.830	20.83	20.96	21.08
H <sub>E</sub>	0.330	0.335	0.340	8.39	8.51	8.63
E	0.295	0.300	0.305	7.49	7.62	7.75
e <sub>1</sub>	0.260	0.267	0.274	6.61	6.78	6.96
e	-	0.050	-	-	1.27	-
s	-	-	0.048	-	-	1.22
y	-	-	0.004	-	-	0.10

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E doesn't include resin fins.
3. Dimension e<sub>1</sub> is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

**Package Information**
**sTSOP 32L TYPE I (8 X 13.4mm) Outline Dimensions**

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.049	-	-	1.25
A1	0.002	-	-	0.05	-	-
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.0056	0.0059	0.0062	0.142	0.150	0.158
E	0.311	0.315	0.319	7.90	8.00	8.10
e	0.020 TYP			0.50 TYP		
D	0.520	0.528	0.535	13.20	13.40	13.60
D1	0.461	0.465	0.469	11.70	11.80	11.90
L	0.012	0.020	0.028	0.30	0.50	0.70
LE	0.0275	0.0315	0.0355	0.700	0.800	0.900
S	0.0109 TYP			0.278 TYP		
theta	0°	3°	5°	0°	3°	5°

**Notes:**

1. The maximum value of dimension D1 includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.