



## LP62E16128A-T Series

### 128K X 16 BIT LOW VOLTAGE CMOS SRAM

#### Features

- Operating voltage: 1.8V to 2.2V
- Access times: 70 ns (max.)
- Current:
  - Very low power version: Operating: 25mA (max.)
  - Standby: 10µA (max.)

- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 1.2V (min.)
- Available in 44-pin TSOP and 48-ball CSP (6 x 8mm) packages

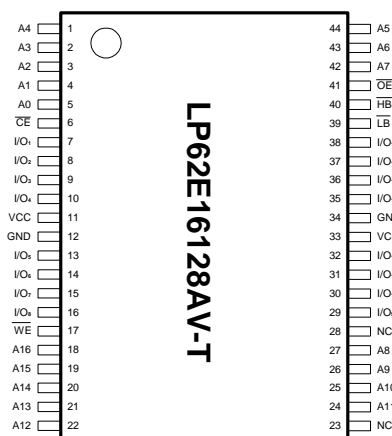
#### General Description

The LP62E16128A-T is a low operating current 2,097,152-bit static random access memory organized as 131,072 words by 16 bits and operates on low power voltage from 1.8V to 2.2V. It is built using AMIC's high performance CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

The chip enable input is provided for POWER-DOWN, device enable. Two byte enable inputs and an output enable input are included for easy interfacing. Data retention is guaranteed at a power supply voltage as low as 1.2V.

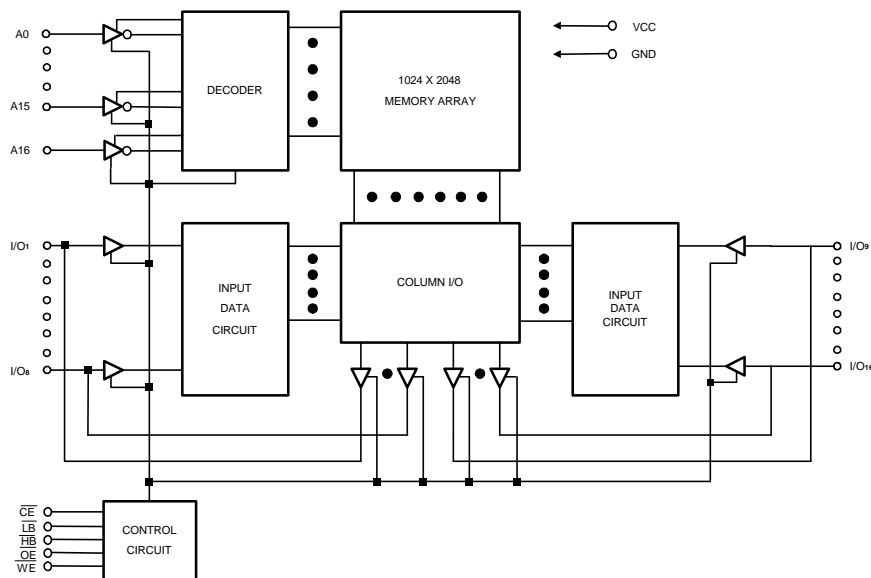
#### Pin Configurations

##### ■ TSOP



##### ■ CSP (Chip Size Package) 48-pin Top View

	1	2	3	4	5	6
A	$\overline{\text{LB}}$	$\overline{\text{OE}}$	A0	A1	A2	NC
B	I/O <sub>9</sub>	$\overline{\text{HB}}$	A3	A4	$\overline{\text{CE}}$	I/O <sub>1</sub>
C	I/O <sub>10</sub>	I/O <sub>11</sub>	A5	A6	I/O <sub>2</sub>	I/O <sub>3</sub>
D	GND	I/O <sub>12</sub>	NC	A7	I/O <sub>4</sub>	VCC
E	VCC	I/O <sub>13</sub>	NC	A16	I/O <sub>5</sub>	GND
F	I/O <sub>15</sub>	I/O <sub>14</sub>	A14	A15	I/O <sub>6</sub>	I/O <sub>7</sub>
G	I/O <sub>16</sub>	NC	A12	A13	$\overline{\text{WE}}$	I/O <sub>8</sub>
H	NC	A8	A9	A10	A11	NC

**Block Diagram**

**Pin Descriptions -- TSOP**

Pin No.	Symbol	Description
1 - 5, 18 - 22, 24 - 27, 42 - 44	A0 - A16	Address Inputs
6	$\overline{CE}$	Chip Enable Input
7 - 10, 13 - 16, 29 - 32, 35 - 38	I/O <sub>1</sub> - I/O <sub>16</sub>	Data Inputs/Outputs
17	$\overline{WE}$	Write Enable Input
39	$\overline{LB}$	Lower Byte Enable Input (I/O <sub>1</sub> to I/O <sub>8</sub> )
40	$\overline{HB}$	Higher Byte Enable Input (I/O <sub>9</sub> to I/O <sub>16</sub> )
41	$\overline{OE}$	Output Enable Input
11, 33	VCC	Power
12, 34	GND	Ground
23, 28	NC	No Connection

**Pin Description - CSP**

Symbol	Description	Symbol	Description
A0 - A16	Address Inputs	$\overline{\text{HB}}$	Higher Byte Enable Input (I/O <sub>9</sub> - I/O <sub>16</sub> )
$\overline{\text{CE}}$	Chip Enable	$\overline{\text{OE}}$	Output Enable
I/O <sub>1</sub> - I/O <sub>16</sub>	Data Input/Output	VCC	Power Supply
$\overline{\text{WE}}$	Write Enable Input	GND	Ground
$\overline{\text{LB}}$	Lower Byte Enable Input (I/O <sub>1</sub> - I/O <sub>8</sub> )	NC	No Connection

**Recommended DC Operating Conditions**

(T<sub>A</sub> = -25°C to + 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	1.8	2	2.2	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	1.4	-	VCC + 0.2	V
V <sub>IL</sub>	Input Low Voltage	-0.2	-	+0.4	V
C <sub>L</sub>	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

**Absolute Maximum Ratings\***

VCC to GND ..... -0.5V to +3.0V  
 IN, IN/OUT Volt to GND ..... -0.5V to VCC + 0.5V  
 Operating Temperature, T<sub>opr</sub> ..... -25°C to +85°C  
 Storage Temperature, T<sub>stg</sub> ..... -55°C to +125°C  
 Power Dissipation, P<sub>T</sub> ..... 0.7W

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics** (T<sub>A</sub> = -25°C to + 85°C, VCC = 1.8V to 2.2V, GND = 0V)

Symbol	Parameter	LP62E16128A-70LLT		Unit	Conditions
		Min.	Max.		
I <sub>LI</sub>	Input Leakage Current	-	1	μA	V <sub>IN</sub> = GND to VCC
I <sub>LO</sub>	Output Leakage Current	-	1	μA	$\overline{CE} = V_{IH}$ or $\overline{LB} = V_{IH}$ or $\overline{HB} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IH}$ V <sub>IO</sub> = GND to VCC
I <sub>CC</sub>	Active Power Supply Current	-	5	mA	$\overline{CE} = V_{IL}$ , I <sub>IO</sub> = 0mA
I <sub>CC1</sub>	Dynamic Operating Current	-	25	mA	Min. Cycle, Duty = 100% $\overline{CE} = V_{IL}$ , I <sub>IO</sub> = 0mA
I <sub>CC2</sub>		-	10	mA	$\overline{CE} = V_{IL}$ , V <sub>IH</sub> = VCC, V <sub>IL</sub> = 0V, f = 1MHz, I <sub>IO</sub> = 0 mA
I <sub>SB</sub>	Standby Power	-	0.3	mA	$\overline{CE} = V_{IH}$
I <sub>SB1</sub>		-	10	μA	$\overline{CE} \geq VCC - 0.2V$ , V <sub>IN</sub> ≥ 0V
V <sub>OL</sub>	Output Low Voltage	-	0.2	V	I <sub>OL</sub> = 0.1 mA
V <sub>OH</sub>	Output High Voltage	1.6	-	V	I <sub>OH</sub> = -0.1 mA

**Truth Table**

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{LB}}$	$\overline{\text{HB}}$	I/O <sub>1</sub> to I/O <sub>8</sub> Mode	I/O <sub>9</sub> to I/O <sub>16</sub> Mode	VCC Current
H	X	X	X	X	Not selected	Not selected	I <sub>SB1</sub> , I <sub>SB</sub>
X	X	X	H	H	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB</sub>
L	L	H	L	L	Read	Read	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
			L	H	Read	High - Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
			H	L	High - Z	Read	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
L	X	L	L	L	Write	Write	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
			L	H	Write	Not Write/Hi - Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
			H	L	No Write/Hi - Z	Write	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
L	H	H	X	L	High - Z	High - Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
			L	X	High - Z	High - Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>

Note: X = H or L

**Capacitance** (T<sub>A</sub> = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C <sub>IN</sub> *	Input Capacitance		6	pF	V <sub>IN</sub> = 0V
C <sub>I/O</sub> *	Input/Output Capacitance		8	pF	V <sub>I/O</sub> = 0V

\* These parameters are sampled and not 100% tested.

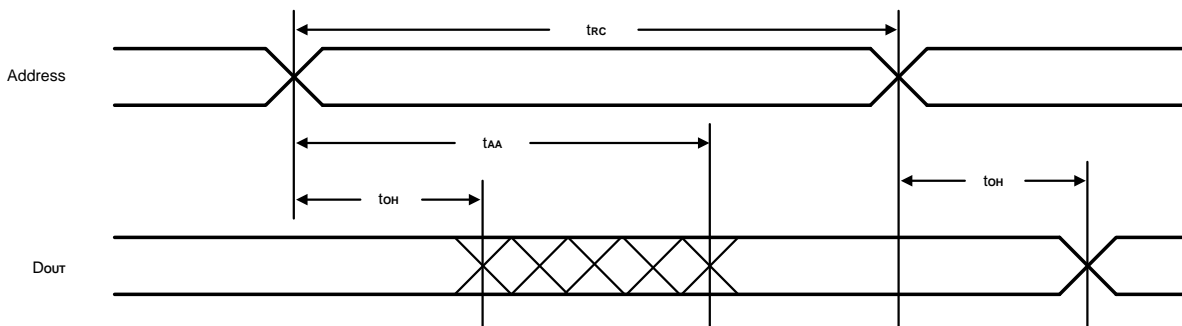
**AC Characteristics** ( $T_A = -25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 1.8\text{V}$  to  $2.2\text{V}$ )

Symbol	Parameter	LP62E16128A-70LLT		Unit
		Min.	Max.	
Read Cycle				
trc	Read Cycle Time	70	-	ns
tAA	Address Access Time	-	70	ns
tACE	Chip Enable Access Time	-	70	ns
tBE	Byte Enable Access Time	-	70	
toE	Output Enable to Output Valid	-	35	ns
tCLZ	Chip Enable to Output in Low Z	10	-	ns
tBLZ	Byte Enable to Outupt in Low Z	10	-	ns
toLZ	Output Enable to Output in Low Z	5	-	ns
tCHZ	Chip Disable to Output in High Z	-	25	ns
tBHZ	Byte Disable to Output in High Z	-	25	ns
toHZ	Output Disable to Output in High Z	-	25	ns
toH	Output Hold from Address Change	5	-	ns
Write Cycle				
twc	Write Cycle Time	70	-	ns
tcw	Chip Enable to End of Write	60	-	ns
tbw	Byte Enable to End of Write	60	-	ns
tAS	Address Setup Time	0	-	ns
tAW	Address Valid to End of Write	60	-	ns
tWP	Write Pulse Width	55	-	ns
tWR	Write Recovery Time	0	-	ns
tWHZ	Write to Output in High Z	-	25	ns
tdW	Data to Write Time Overlap	30	-	ns
tdH	Data Hold from Write Time	0	-	ns
tow	Output Active from End of Write	5	-	ns

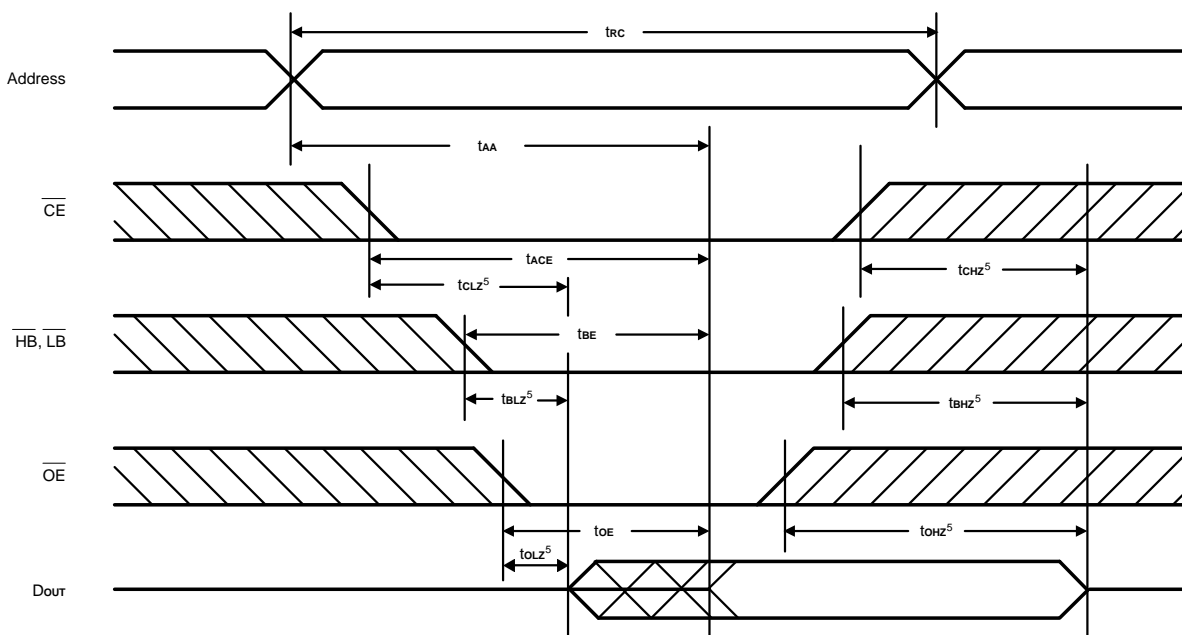
Note:  $t_{CHZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

## Timing Waveforms

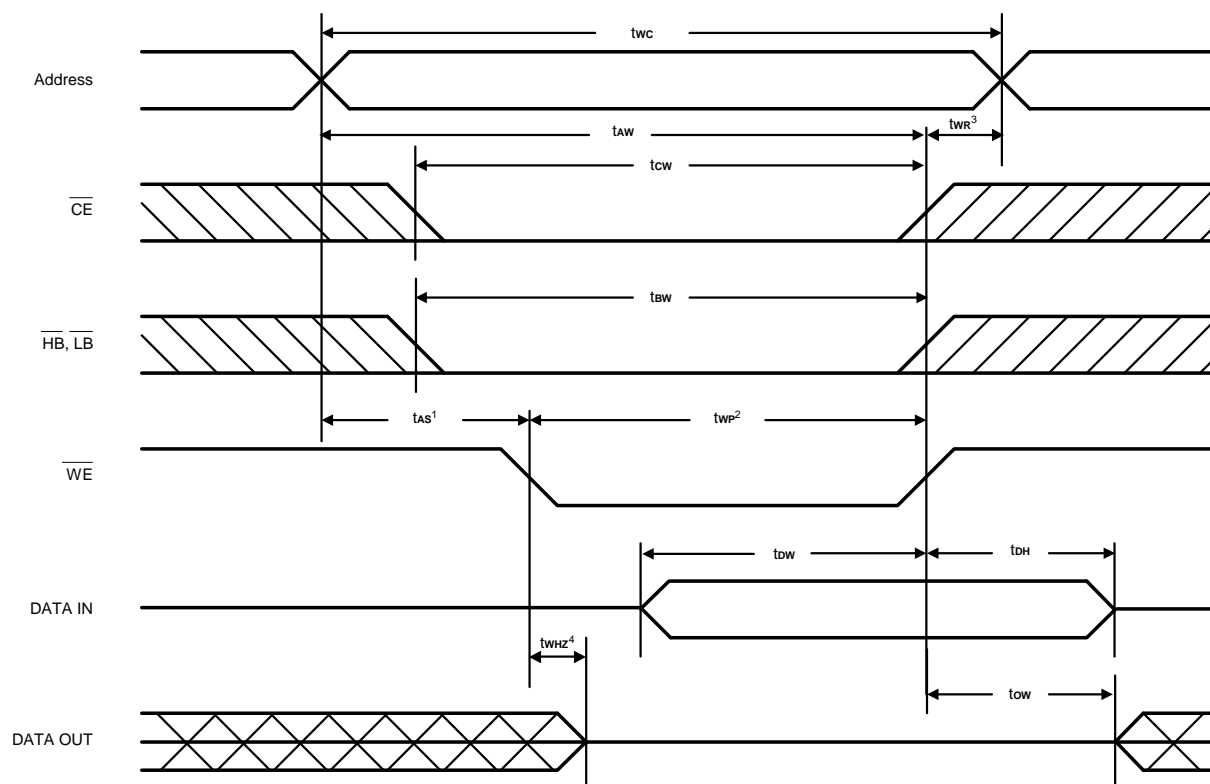
### Read Cycle 1<sup>(1, 2, 4)</sup>



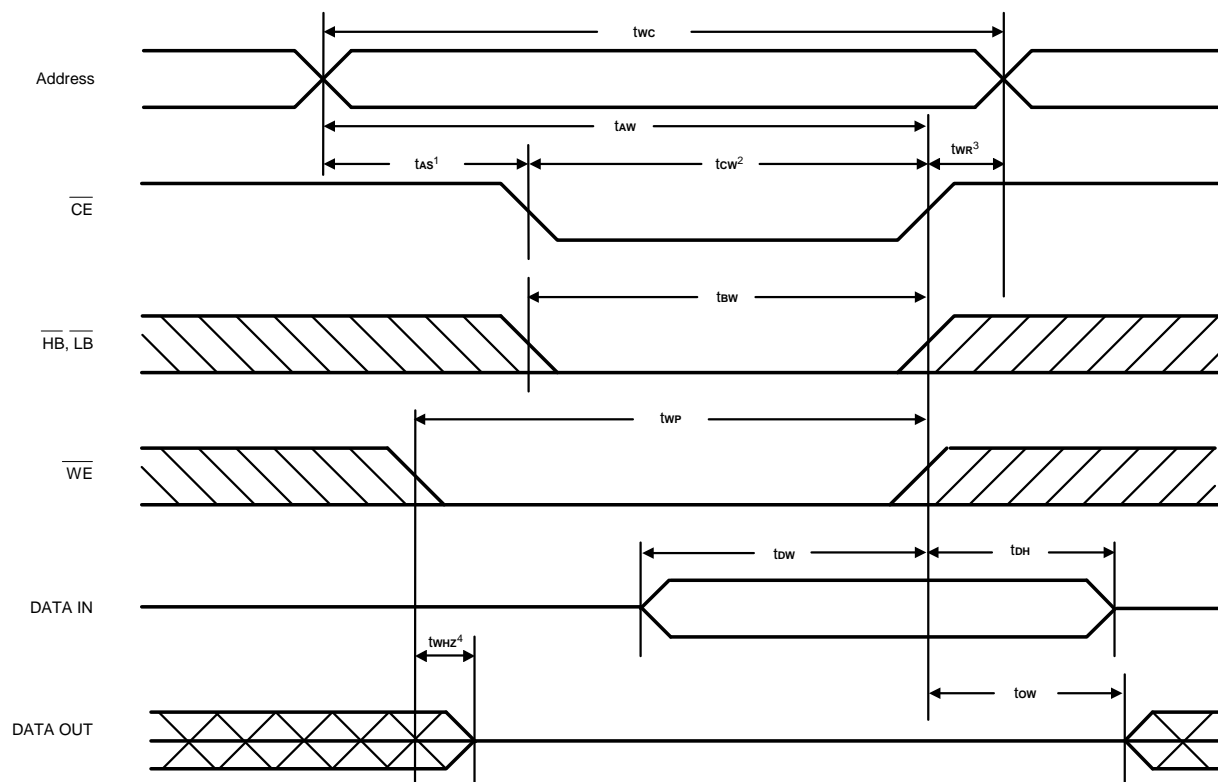
### Read Cycle 2<sup>(1, 2, 3)</sup>

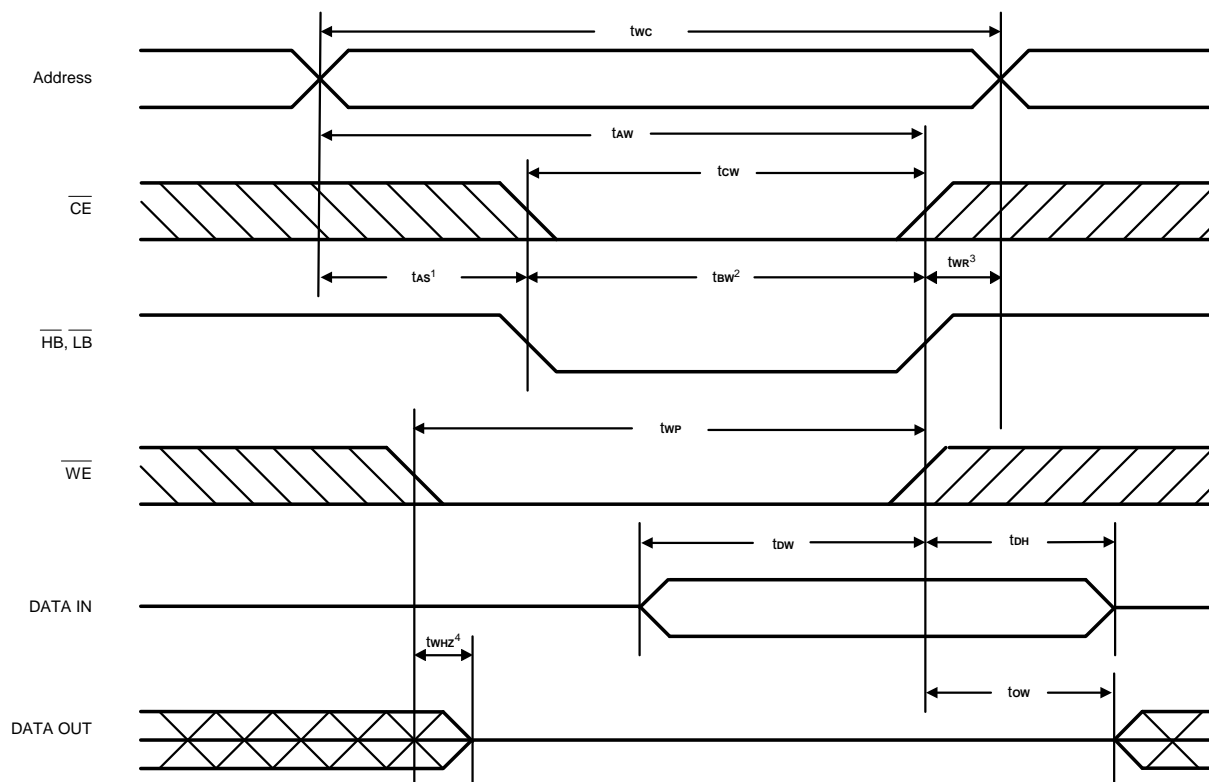


- Notes:
1.  $\overline{WE}$  is high for Read Cycle.
  2. Device is continuously enabled  $\overline{CE} = V_{IL}$ ,  $\overline{HB} = V_{IH}$  and, or  $\overline{LB} = V_{IL}$ .
  3. Address valid prior to or coincident with  $\overline{CE}$  and ( $\overline{HB}$  and, or  $\overline{LB}$ ) transition low.
  4.  $\overline{OE} = V_{IL}$ .
  5. Transition is measured  $\pm 500\text{mV}$  from steady state. This parameter is sampled and not 100% tested.

**Timing Waveforms (continued)**
**Write Cycle 1  
(Write Enable Controlled)**




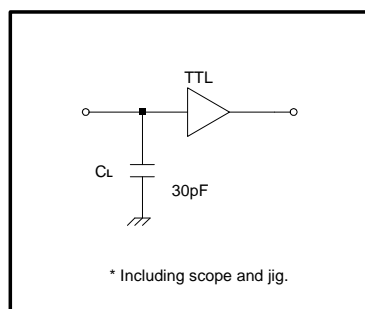
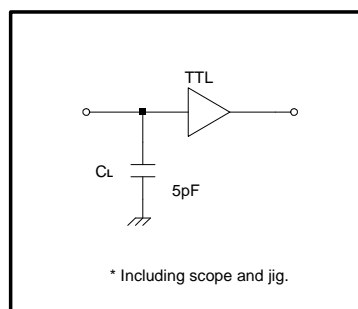
**Timing Waveforms (continued)**
**Write Cycle 2  
(Chip Enable Controlled)**


**Timing Waveforms (continued)**
**Write Cycle 3  
(Byte Enable Controlled)**


- Notes:
1.  $t_{as}$  is measured from the address valid to the beginning of Write.
  2. A Write occurs during the overlap ( $t_{wp}$ ,  $t_{BW}$ ) of a low  $\overline{CE}$ ,  $\overline{WE}$  and ( $\overline{HB}$  and , or  $\overline{LB}$ ).
  3.  $t_{wr}$  is measured from the earliest of  $\overline{CE}$  or  $\overline{WE}$  or ( $\overline{HB}$  and , or  $\overline{LB}$ ) going high to the end of the Write cycle.
  4.  $\overline{OE}$  level is high or low.
  5. Transition is measured  $\pm 500\text{mV}$  from steady state. This parameter is sampled and not 100% tested.

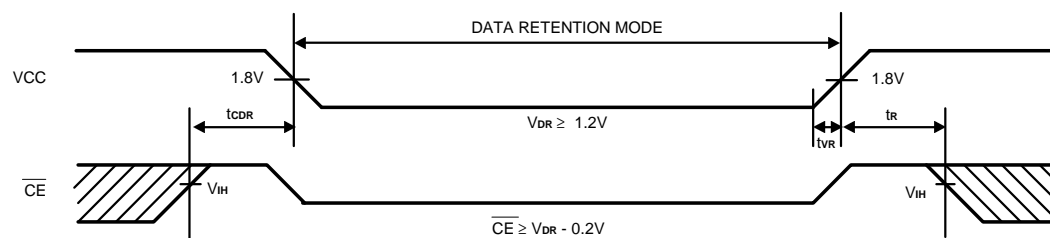
**AC Test Conditions**

Input Pulse Levels	0.2V to VCC - 0.2V
Input Rise And Fall Time	5 ns
Input and Output Timing Reference Levels	0.9V
Output Load	See Figures 1 and 2


**Figure 1. Output Load**

**Figure 2. Output Load for tCLZ, tOLZ, tCHZ, tOHZ, tWHZ, and tOW**
**Data Retention Characteristics** (TA = -25°C to 85°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
VDR	VCC for Data Retention	1.2	2.2	V	$\overline{CE} \geq VCC - 0.2V$
ICCDR	Data Retention Current	-	3*	μA	VCC = 1.2V, $\overline{CE} \geq VCC - 0.2V$ VIN ≥ 0V
tCDR	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
tR	Operation Recovery Time	trc	-	ns	
tVR	VCC Rising Time from Data Retention Voltage to Operating Voltage	5	-	ms	

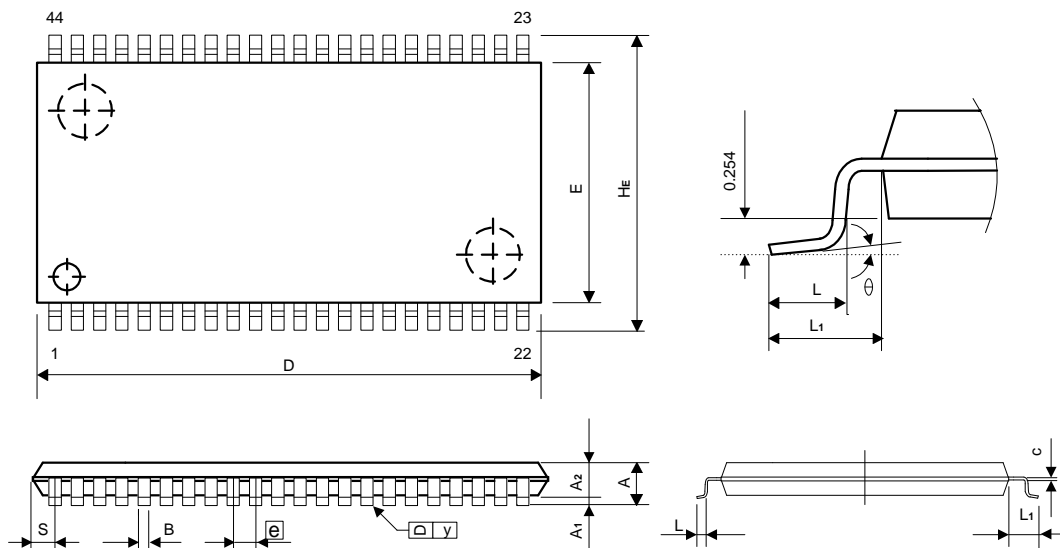
\* LP62E16128A-70LLT      ICCDR: max. 1μA at TA = 0°C to + 40°C

**Low VCC Data Retention Waveform**

**Ordering Information**

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
LP62E16128AV-70LLT	70	25	10	44L TSOP
LP62E16128AU-70LLT		25	10	48L CSP

**Package Information**
**TSOP 44L TYPE II Outline Dimensions**

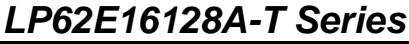
unit: inches/mm



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.047	-	-	1.20
A1	0.002	-	-	0.05	-	-
A2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.010	0.014	0.018	0.25	0.35	0.45
c	-	0.006	-	-	0.15	-
D	0.721	0.725	0.729	18.31	18.41	18.51
E	0.396	0.400	0.404	10.06	10.16	10.26
e	-	0.031	-	-	0.80	-
HE	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	-	0.031	-	-	0.80	-
S	-	-	0.036	-	-	0.93
y	-	-	0.004	-	-	0.10
$\theta$	0°	-	5°	0°	-	5°

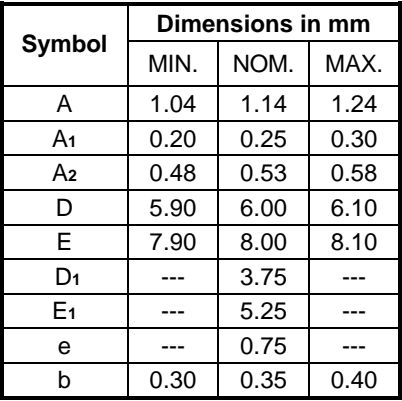
**Notes:**

1. Dimension D&E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Dimension S includes end flash.



### 48LD CSP ( 6 x 8 mm ) Outline Dimensions (48TFBGA)

unit: mm



1. THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC MO192 (LOW PROFILE BGA FAMILY).
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM.  
THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.