

## 20V P-Channel Enhancement Mode MOSFET

### ■ Features

- Advanced trench process technology
- High density cell design for ultra low on-resistance
- Excellent thermal and electrical capabilities
- Compact and low profile SOT-23 package

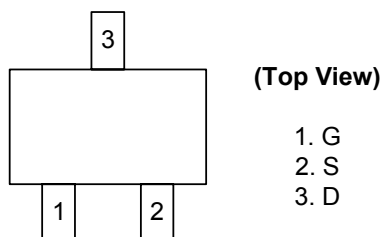
### ■ Product Summary

$V_{DS} = -20V$

$R_{DS(on)}, V_{GS}@-4.5V, I_{DS}@-2.8A = 130m\Omega$ .

$R_{DS(on)}, V_{GS}@-2.5V, I_{DS}@-2.0A = 190m\Omega$ .

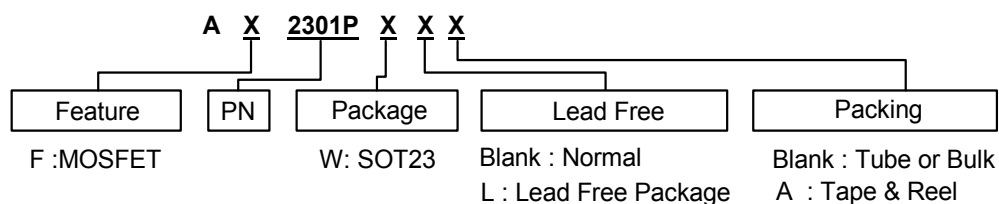
### ■ Pin Assignments



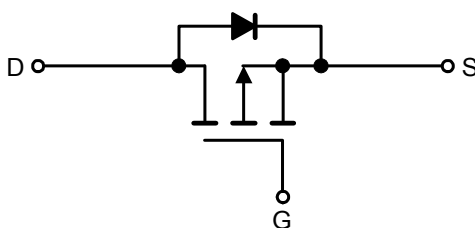
### ■ Pin Descriptions

Pin No.	Pin Name	Description
1	G	Gate
2	S	Source
3	D	Drain

### ■ Ordering information



### ■ Block Diagram





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■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-20	V
$V_{GS}$	Gate-Source Voltage	$\pm 8$	V
$I_D$	Continuous Drain Current	-2.3	A
$I_{DM}$	Pulsed Drain Current	-10	A
$P_D$	Maximum Power Dissipation	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
$T_J$	Operating Junction Temperature	+150	$^\circ\text{C}$
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

## ■ Thermal Performance

Symbol	Parameter	Limit	Units
$T_L$	Lead Temperature (1/8" from case)	5	S
$R_{\theta JA}$	Junction to Ambient Thermal Resistance (PCB mounted)	100	$^\circ\text{C/W}$

Note: Surface mounted on FR4 board  $t \leq 5$  sec.

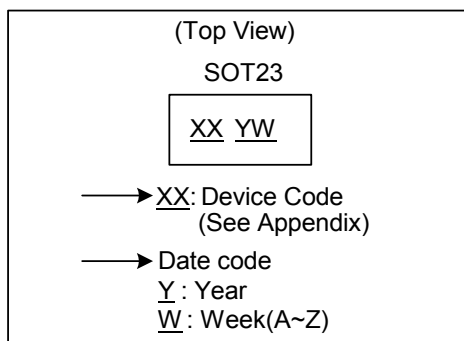
■ Electrical Characteristics Rate  $I_D=-2.3\text{A}$ , ( $T_A=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Static						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-20	-	-	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-2.8A	-	95	130	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-2.0A	-	122	190	
V <sub>GS(TH)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250uA	-0.45	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-16V, V <sub>GS</sub> =0V	-	-	-1.0	uA
I <sub>GSS</sub>	Gate Body Leakage	V <sub>GS</sub> =±8V, V <sub>DS</sub> =0V	-	-	±100	nA
I <sub>D(ON)</sub>	On-State Drain Current	V <sub>DS</sub> =-5V, V <sub>GS</sub> =-10V	-6	-	-	A
g <sub>fs</sub>	Forward Tranconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-2.8A	-	6.5	-	S
Dynamic						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-6V, I <sub>D</sub> =-2.8A, V <sub>GS</sub> =-4.5V	-	5.4	10	nC
Q <sub>gs</sub>	Gate-Source Charge		-	0.8	-	
Q <sub>gd</sub>	Gate-Drain Charge		-	1.1	-	
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-6V, R <sub>L</sub> =6Ω, I <sub>D</sub> =-1A, V <sub>GEN</sub> =-4.5V, R <sub>G</sub> =6Ω	-	5	25	nS
t <sub>r</sub>	Turn-On Rise Time		-	19	60	
t <sub>d(off)</sub>	Turn-Off Delay Time		-	95	110	
t <sub>f</sub>	Turn-Off Fall-Time		-	65	80	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-6V, V <sub>GS</sub> =0V, f=1.0MHz	-	447	-	pF
C <sub>oss</sub>	Output Capacitance		-	127	-	
C <sub>rss</sub>	Reverse Transfer Capacitance		-	80	-	
Source-Drain Diode						
I <sub>s</sub>	Max. Diode Forward Current		-	-	-1.6	A
V <sub>SD</sub>	Diode Forward Voltage	I <sub>s</sub> =-1.6A, V <sub>GS</sub> =0V	-	-0.8	-1.2	V

Note: Pulse test: pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$

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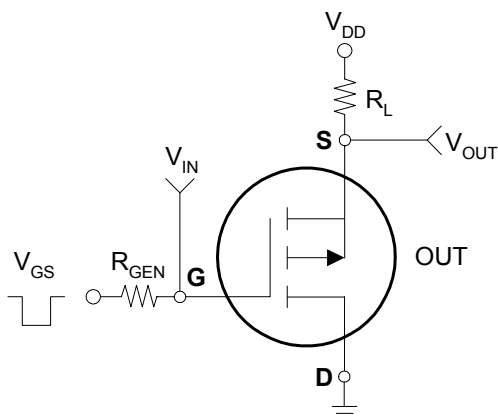
### ■ Marking Information



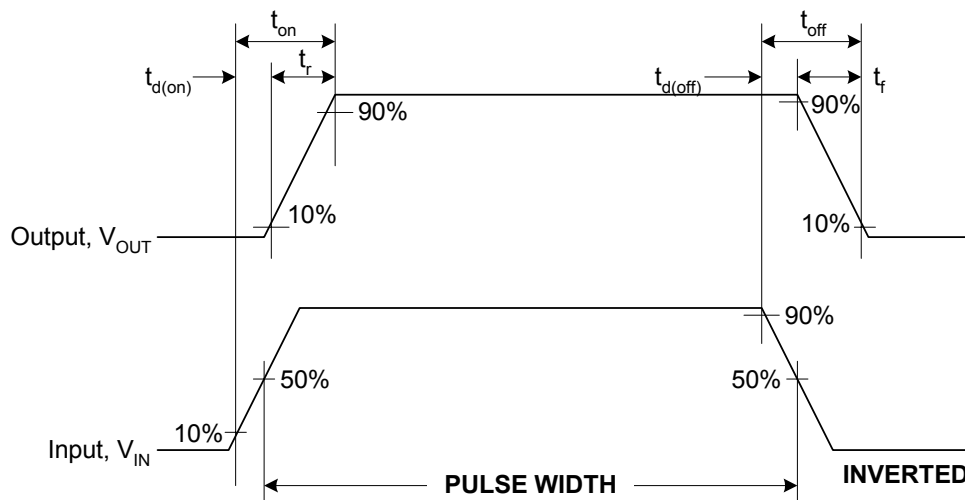
#### Appendix

Part Number	Package	Device Code
AF2301P	SOT23-3	01

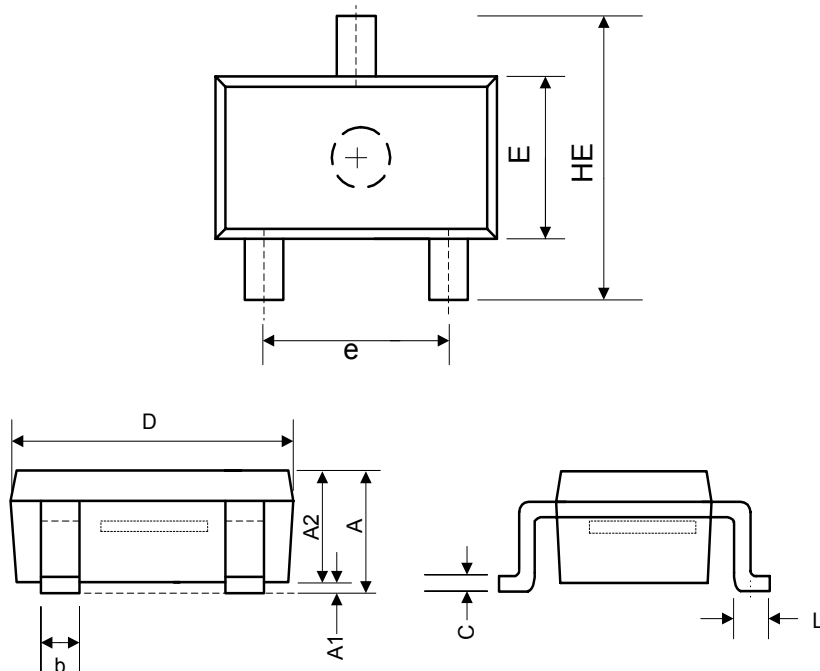
### ■ Switching Test Circuit



### ■ Switching Waveforms



### ■ Package Information



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.00	1.20	1.40	0.039	0.047	0.055
A1	0.00	-	0.10	0.000	-	0.004
A2	1.00	1.15	1.30	0.039	0.045	0.051
b	0.35	-	0.50	0.014	-	0.020
C	0.10	0.175	0.25	0.004	0.007	0.010
D	2.70	2.90	3.10	0.106	0.114	0.122
E	1.40	1.60	1.80	0.055	0.063	0.071
e	1.70	2.00	2.30	0.067	0.079	0.091
HE	2.40	2.70	3.00	0.094	0.106	0.118
L	0.30	-	0.55	0.012	-	0.022