

P-Channel 30-V (D-S) MOSFET

■ Features

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Extended V_{GS} range (± 25) for battery pack applications

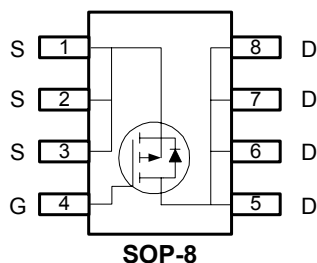
■ General Description

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWM DC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

■ Product Summary

V_{DS} (V)	$r_{DS(on)}$ (m Ω)	I_D (A)
-30	30@ $V_{GS}=-10V$	9.5
	52@ $V_{GS}=-4.5V$	7.5

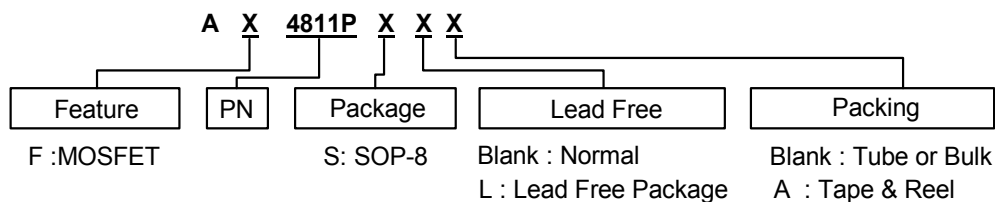
■ Pin Assignments



■ Pin Descriptions

Pin Name	Description
S	Source
G	Gate
D	Drain

■ Ordering information



**AF4811P****P-Channel 30-V (D-S) MOSFET****■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)**

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 25	V
I_D	Continuous Drain Current (Note 1)	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	
I_{DM}	Pulsed Drain Current (Note 2)	± 50	A
I_S	Continuous Source Current (Diode Conduction) (Note 1)	-2.1	A
P_D	Power Dissipation (Note 1)	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

■ Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{\theta JC}$	Maximum Junction-to-Case (Note 1) $t \leq 5 \text{ sec}$	25	$^\circ\text{C/W}$
$R_{\theta JA}$	Maximum Junction-to-Ambient (Note 1) $t \leq 10 \text{ sec}$	50	$^\circ\text{C/W}$

Note 1: surface Mounted on 1"x 1" FR4 Board.**Note 2:** Pulse width limited by maximum junction temperature**■ Specifications ($T_A=25^\circ\text{C}$ unless otherwise noted)**

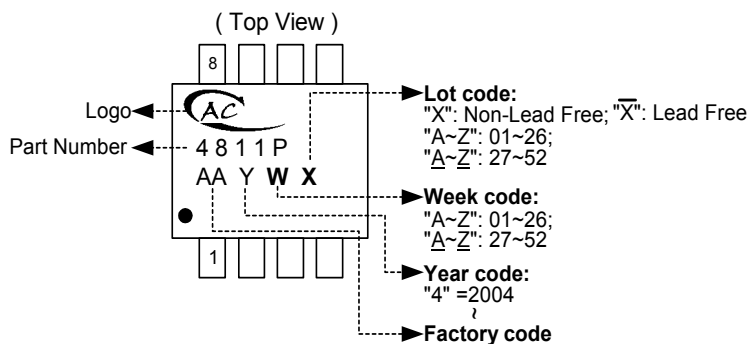
Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Static						
V _{(BR)DSS}	Drain-Source breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	-	-	V
V _{GS(th)}	Gate-Threshold Voltage	V _{DS} = V _{GS} , I _D =-250uA	-1	-1.6	-3	V
I _{GSS}	Gate-Body Leakage	V _{DS} =0V, V _{GS} =±25V	-	-	±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V V _{DS} =-24V, V _{GS} =0V, T _J =55°C	-	-	-1 -5	uA
I _{D(on)}	On-State Drain Current (Note 3)	V _{DS} =-5V, V _{GS} =-10V	-50	-	-	A
r _{DS(on)}	Drain-Source On-Resistance (Note 3)	V _{GS} =-10V, I _D =-9.5A	-	24	30	mΩ
		V _{GS} =-4.5V, I _D =-7.5A	-	44	52	
		V _{GS} =-10V, I _D =-9.5A, T _J =55°C	-	29	36	
g _{fs}	Forward Tranconductance (Note 3)	V _{GS} =-15V, I _D =-9.5A	-	31	-	S
V _{SD}	Diode Forward Voltage	I _S =-2.1A, V _{GS} =0V	-	-0.7	-1.2	V
Dynamic (Note 4)						
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V, I _D =-9.5A	-	15	26	nC
Q _{gs}	Gate-Source Charge		-	5.8	-	
Q _{gd}	Gate-Drain Charge		-	12	-	
Switching						
t _{d(on)}	Turn-On Delay Time	V _{DD} =-15, R _L =15Ω, ID=-1A, VGEN=-10V, RG=6Ω	-	15	26	nS
t _r	Rise Time		-	12	21	
t _{d(off)}	Turn-Off Delay Time		-	62	108	
t _f	Fall-Time		-	46	71	

Note 3: Pulse test: $PW \leq 300\mu s$ duty cycle $\leq 2\%$.**Note 4:** Guaranteed by design, not subject to production testing.

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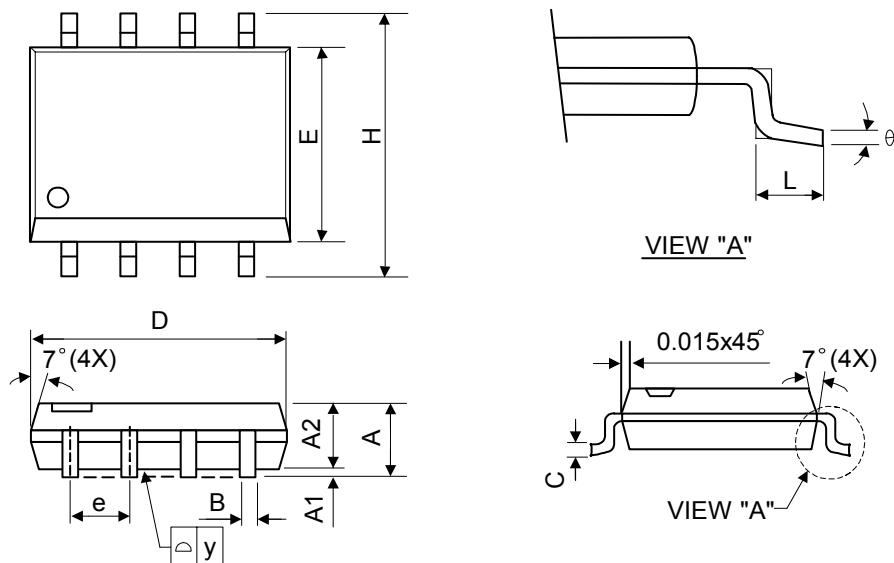
■ Marking Information

SOP-8L



■ Package Information

Package Type: SOP-8L



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	-	-	0.10	-	-	0.004
θ	0°	-	8°	0°	-	8°