

## General Description

The AAT7357 is a low threshold dual MOSFET designed for the battery, cell phone, and PDA markets. Using AnalogicTech™'s ultra high density MOSFET process and space saving small outline J-lead package, performance superior to that normally found in a TSSOP-8 footprint has been squeezed into the footprint of a TSOPJW-8 package.

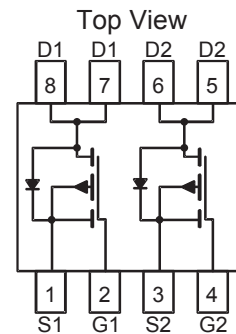
## Features

- $V_{DS(MAX)} = -20V$
- $I_{D(MAX)}^1 = -5A @ 25^{\circ}C$
- Low  $R_{DS(ON)}$ :
  - $39 m\Omega @ V_{GS} = -4.5V$
  - $63 m\Omega @ V_{GS} = -2.5V$

## Applications

- Battery Packs
- Cellular & Cordless Telephones
- Battery-powered portable equipment

## Dual TSOPJW-8 Package



## Absolute Maximum Ratings ( $T_A = 25^{\circ}C$ unless otherwise noted)

Symbol	Description	Value	Units
$V_{DS}$	Drain-Source Voltage	-20	V
$V_{GS}$	Gate-Source Voltage	$\pm 12$	
$I_D$	Continuous Drain Current @ $T_J = 150^{\circ}C$ <sup>1</sup>	<div><math>T_A = 25^{\circ}C</math> <math>\pm 5</math></div> <div><math>T_A = 70^{\circ}C</math> <math>\pm 4</math></div>	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	$\pm 12$	
$I_S$	Continuous Source Current (Source-Drain Diode) <sup>1</sup>	-1.3	
$P_D$	Maximum Power Dissipation <sup>1</sup>	<div><math>T_A = 25^{\circ}C</math> 1.6</div> <div><math>T_A = 70^{\circ}C</math> 1.0</div>	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	

## Thermal Characteristics

Symbol	Description	Typ	Max	Units
$R_{\theta JA}$	Junction-to-Ambient steady state, one FET on <sup>1</sup>	115	140	$^{\circ}C/W$
$R_{\theta JA2}$	Junction-to-Ambient $t < 5$ seconds <sup>1</sup>	64	78	$^{\circ}C/W$
$R_{\theta JF}$	Junction-to-Foot <sup>1</sup>	60	72	$^{\circ}C/W$

**Electrical Characteristics** ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Description	Conditions	Min	Typ	Max	Units
DC Characteristics						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-20			V
R <sub>DS(ON)</sub>	Drain-Source ON-Resistance <sup>2</sup>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-5A		30	39	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-4A		49	63	
I <sub>D(ON)</sub>	On-State Drain Current <sup>2</sup>	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-5V (Pulsed)	-12			A
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250μA	-0.6			V
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V			±100	nA
I <sub>DSS</sub>	Drain Source Leakage Current	V <sub>GS</sub> =0V, V <sub>DS</sub> =-20V			-1	μA
		V <sub>GS</sub> =0V, V <sub>DS</sub> =-16V, T <sub>J</sub> =70°C <sup>3</sup>			-5	
g <sub>fs</sub>	Forward Transconductance <sup>2</sup>	V <sub>DS</sub> =-5V, I <sub>D</sub> =-5A		12		S
Dynamic Characteristics <sup>3</sup>						
Q <sub>G</sub>	Total Gate Charge	V <sub>DS</sub> =-10V, R <sub>D</sub> =2.0Ω, V <sub>GS</sub> =-4.5V		14		nC
Q <sub>GS</sub>	Gate-Source Charge	V <sub>DS</sub> =-10V, R <sub>D</sub> =2.0Ω, V <sub>GS</sub> =-4.5V		3.5		
Q <sub>GD</sub>	Gate-Drain Charge	V <sub>DS</sub> =-10V, R <sub>D</sub> =2.0Ω, V <sub>GS</sub> =-4.5V		5.6		
t <sub>D(ON)</sub>	Turn-ON Delay	V <sub>DS</sub> =-10V, R <sub>D</sub> =2.0Ω, V <sub>GS</sub> =-4.5V, R <sub>G</sub> =6Ω		TBD		ns
t <sub>R</sub>	Turn-ON Rise Time	V <sub>DS</sub> =-10V, R <sub>D</sub> =2.0Ω, V <sub>GS</sub> =-4.5V, R <sub>G</sub> =6Ω		TBD		
t <sub>D(OFF)</sub>	Turn-OFF Delay	V <sub>DS</sub> =-10V, R <sub>D</sub> =2.0Ω, V <sub>GS</sub> =-4.5V, R <sub>G</sub> =6Ω		TBD		
t <sub>F</sub>	Turn-OFF Fall Time	V <sub>DS</sub> =-10V, R <sub>D</sub> =2.0Ω, V <sub>GS</sub> =-4.5V, R <sub>G</sub> =6Ω		TBD		
Source-Drain Diode Characteristics						
V <sub>SD</sub>	Source-Drain Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0, I <sub>S</sub> =-5A			-1.2	V
I <sub>S</sub>	Continuous Diode Current <sup>1</sup>				-1.3	A

**Notes:**

1. Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 5 second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications.  $R_{\theta JF} + R_{\theta FA} = R_{\theta JA}$  where the foot thermal reference is defined as the normal solder mounting surface of the device's leads.  $R_{\theta JF}$  is guaranteed by design, however  $R_{\theta CA}$  is determined by the PCB design. Actual maximum continuous current is limited by the application's design.

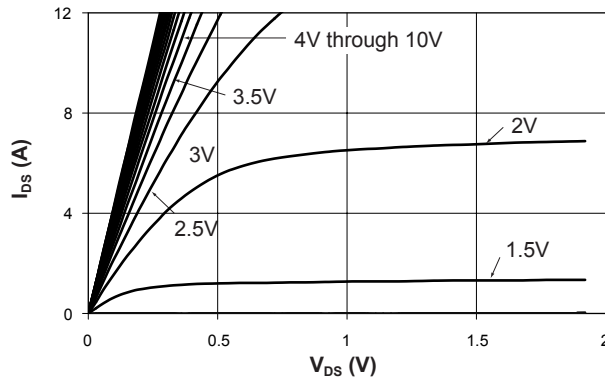
2. Pulse test: Pulse Width = 300  $\mu s$

3. Guaranteed by design. Not subject to production testing.

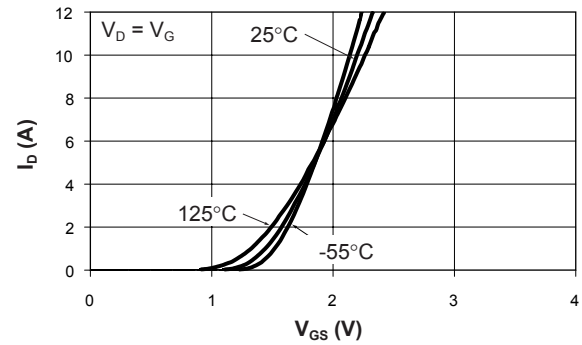
## Typical Characteristics

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

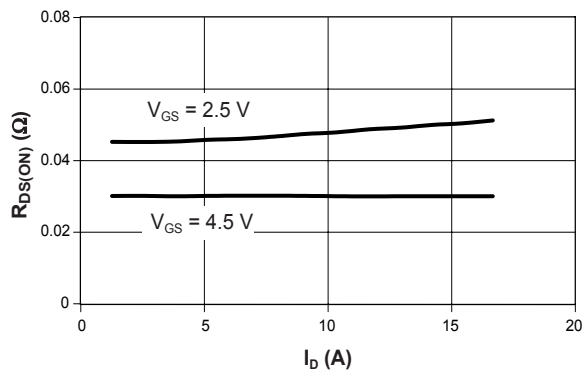
**Output Characteristics**



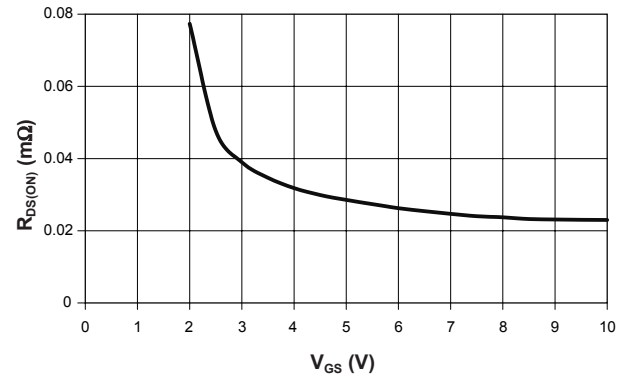
**Transfer Characteristics**



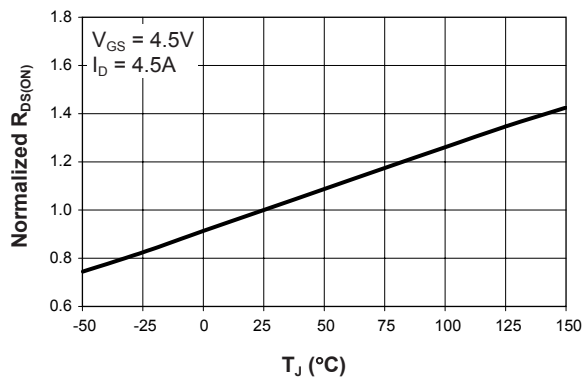
**On-Resistance vs. Drain Current**



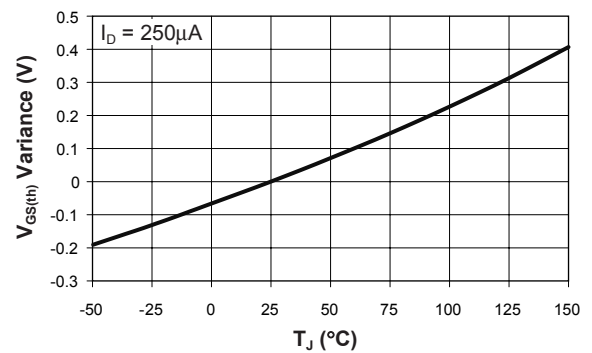
**On-Resistance vs. Gate to Source Voltage**



**On-Resistance vs. Junction Temperature**



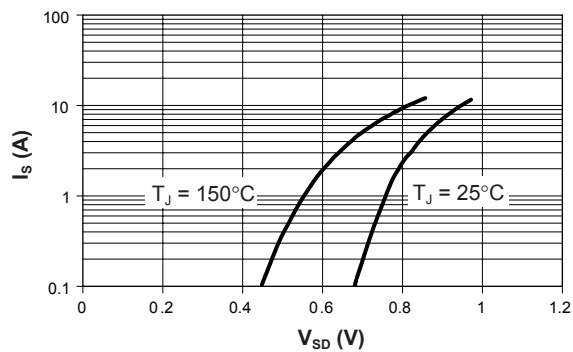
**Threshold Voltage**



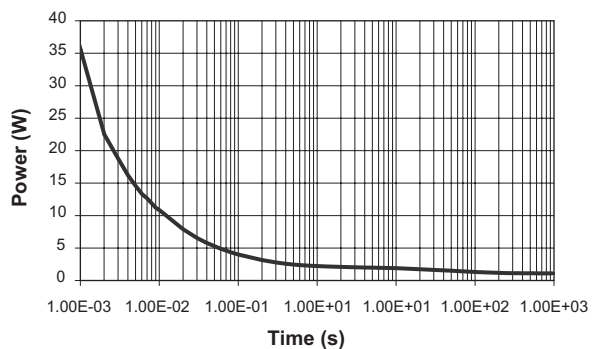
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( $T_J = 25^\circ\text{C}$  unless otherwise noted)

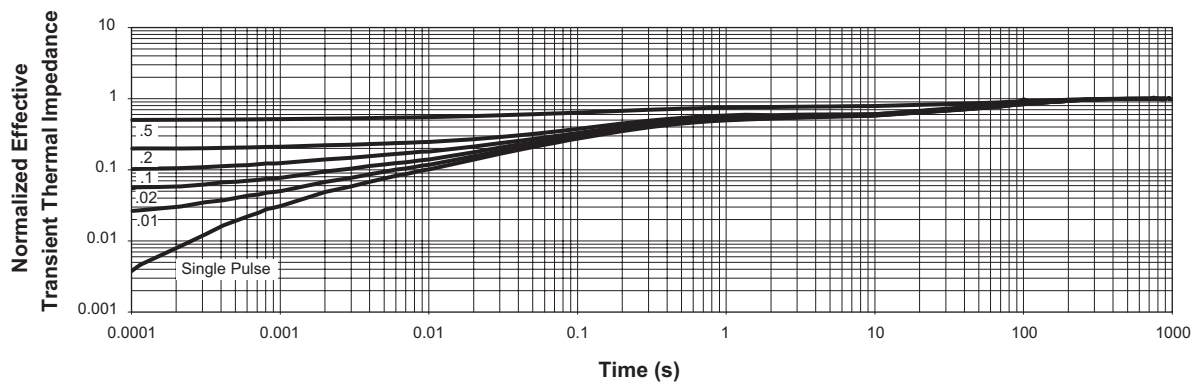
**Source-Drain Diode Forward Voltage**



**Single Pulse Power, Junction to Ambient**



**Transient Thermal Response, Junction to Ambient**

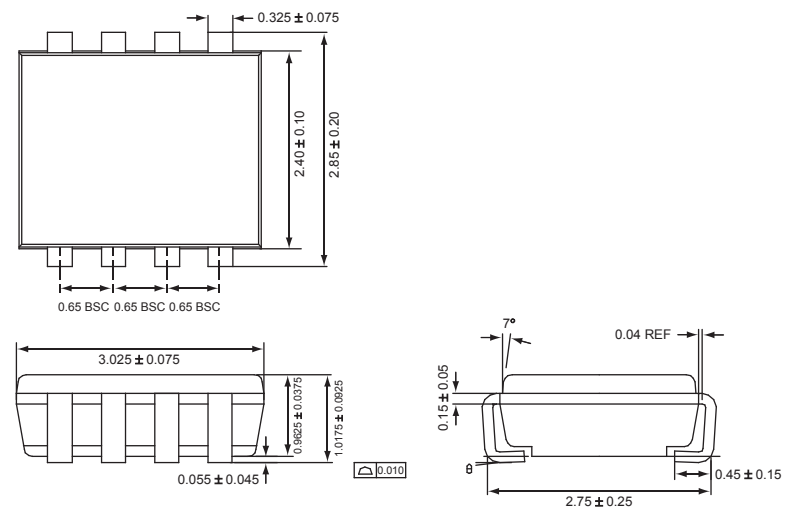


## Ordering Information

Package	Marking	Part Number (Tape and Reel)
TSOPJW-8		AAT7357ITS-T1

## Package Information

### TSOPJW-8



All dimensions in millimeters.

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