

## General Description

The AAT8343 is a low threshold P-channel MOSFET designed for the battery, cell phone, and PDA markets. Using AnalogicTech's ultra-high-density proprietary TrenchDMOS™ technology, this product demonstrates high power handling and small size.

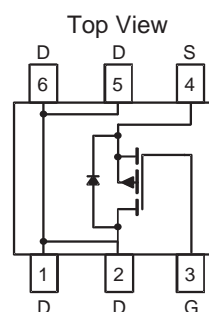
## Applications

- Battery Packs
- Battery-Powered Portable Equipment
- Cellular and Cordless Telephones

## Features

- Drain-Source Voltage (max): -20V
- Continuous Drain Current<sup>1</sup> (max):  
-4.5A @ 25°C
- Low On-Resistance:
  - 60mΩ @  $V_{GS} = -4.5V$
  - 110mΩ @  $V_{GS} = -2.5V$

## TSOP-6 Package



## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Symbol	Description	Value	Units
$V_{DS}$	Drain-Source Voltage	-20	V
$V_{GS}$	Gate-Source Voltage	$\pm 12$	
$I_D$	Continuous Drain Current @ $T_J = 150^\circ\text{C}^1$	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	$\pm 16$	
$I_S$	Continuous Source Current (Source-Drain Diode) <sup>1</sup>	-1.3	
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$

## Thermal Characteristics<sup>1</sup>

Symbol	Description	Typ	Max	Units
$R_{\theta JA}$	Junction-to-Ambient Steady State	95	115	$^\circ\text{C}/\text{W}$
$R_{\theta JA2}$	Junction-to-Ambient $t < 5$ Seconds	51	62	$^\circ\text{C}/\text{W}$
$R_{\theta JF}$	Junction-to-Foot	25	30	$^\circ\text{C}/\text{W}$
$P_D$	Maximum Power Dissipation	$T_A = 25^\circ\text{C}$	2.0	W
		$T_A = 70^\circ\text{C}$	1.3	

1. Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 5-second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications.  $R_{\theta JF} + R_{\theta FA} = R_{\theta JA}$  where the foot thermal reference is defined as the normal solder mounting surface of the device's leads.  $R_{\theta JF}$  is guaranteed by design; however,  $R_{\theta CA}$  is determined by the PCB design. Actual maximum continuous current is limited by the application's design.

2. Pulse test: Pulse Width = 300μs.

## Electrical Characteristics

$T_J = 25^\circ\text{C}$ , unless otherwise noted.

Symbol	Description	Conditions	Min	Typ	Max	Units
DC Characteristics						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-20			V
R <sub>DS(ON)</sub>	Drain-Source On-Resistance <sup>1</sup>	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4.5A		49	60	mΩ
		V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -3.3A		85	110	
I <sub>D(ON)</sub>	On-State Drain Current <sup>1</sup>	V <sub>GS</sub> = -4.5V, V <sub>DS</sub> = -5V (pulsed)	-16			A
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250μA	-0.6			V
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±12V, V <sub>DS</sub> = 0V			±100	nA
I <sub>DSS</sub>	Drain Source Leakage Current	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -20V			-1	μA
		V <sub>GS</sub> = 0V, V <sub>DS</sub> = -16V, T <sub>J</sub> = 70°C <sup>2</sup>			-5	
g <sub>fs</sub>	Forward Transconductance <sup>1</sup>	V <sub>DS</sub> = -5V, I <sub>D</sub> = -4.5A		7		S
Dynamic Characteristics <sup>2</sup>						
Q <sub>G</sub>	Total Gate Charge	V <sub>DS</sub> = -10V, R <sub>D</sub> = 2.2Ω, V <sub>GS</sub> = -4.5V		8.5		nC
Q <sub>GS</sub>	Gate-Source Charge	V <sub>DS</sub> = -10V, R <sub>D</sub> = 2.2Ω, V <sub>GS</sub> = -4.5V		1.8		
Q <sub>GD</sub>	Gate-Drain Charge	V <sub>DS</sub> = -10V, R <sub>D</sub> = 2.2Ω, V <sub>GS</sub> = -4.5V		2.9		
t <sub>D(ON)</sub>	Turn-On Delay	V <sub>DS</sub> = -10V, R <sub>D</sub> = 2.2Ω, V <sub>GS</sub> = -4.5V, R <sub>G</sub> = 6Ω		12		ns
t <sub>R</sub>	Turn-On Rise Time	V <sub>DS</sub> = -10V, R <sub>D</sub> = 2.2Ω, V <sub>GS</sub> = -4.5V, R <sub>G</sub> = 6Ω		32		
t <sub>D(OFF)</sub>	Turn-Off Delay	V <sub>DS</sub> = -10V, R <sub>D</sub> = 2.2Ω, V <sub>GS</sub> = -4.5V, R <sub>G</sub> = 6Ω		64		
t <sub>F</sub>	Turn-Off Fall Time	V <sub>DS</sub> = -10V, R <sub>D</sub> = 2.2Ω, V <sub>GS</sub> = -4.5V, R <sub>G</sub> = 6Ω		40		
Source-Drain Diode Characteristics						
V <sub>SD</sub>	Source-Drain Forward Voltage <sup>1</sup>	V <sub>GS</sub> = 0, I <sub>S</sub> = -4.5A			-1.3	V
I <sub>S</sub>	Continuous Diode Current <sup>3</sup>				-1.3	A

1. Pulse test: Pulse Width = 300 $\mu$ s.

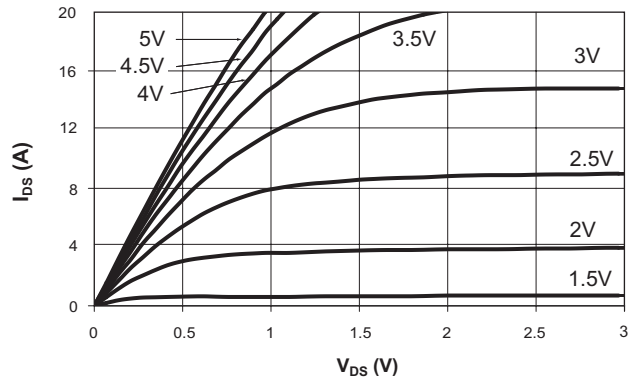
2. Guaranteed by design. Not subject to production testing.

3. Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 5-second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications.  $R_{\theta JF} + R_{\theta FA} = R_{\theta JA}$  where the foot thermal reference is defined as the normal solder mounting surface of the device's leads.  $R_{\theta JF}$  is guaranteed by design; however,  $R_{\theta CA}$  is determined by the PCB design. Actual maximum continuous current is limited by the application's design.

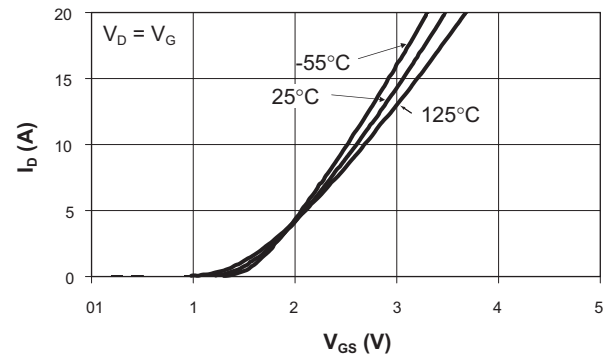
## Typical Characteristics

$T_J = 25^\circ\text{C}$ , unless otherwise noted.

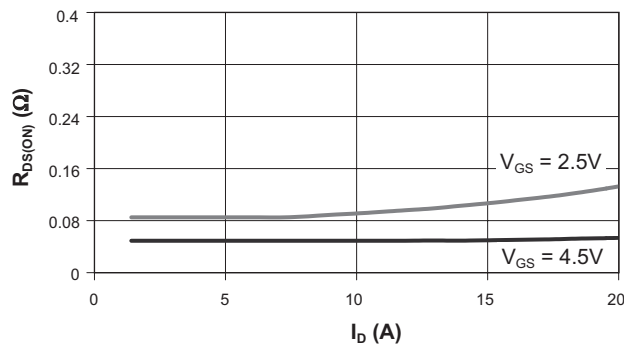
**Output Characteristics**



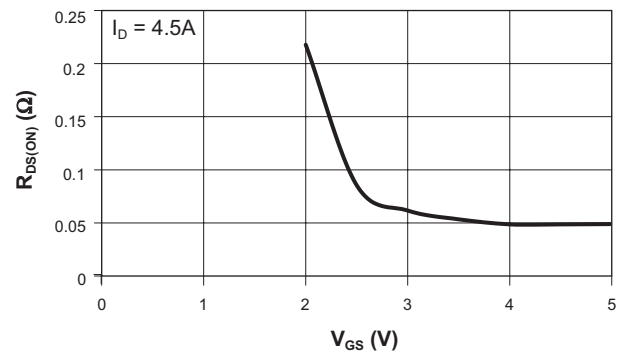
**Transfer Characteristics**



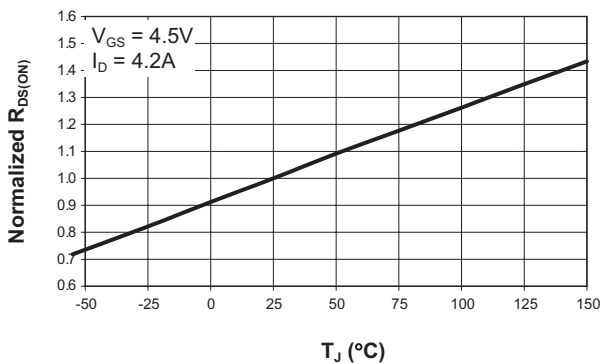
**On-Resistance vs. Drain Current**



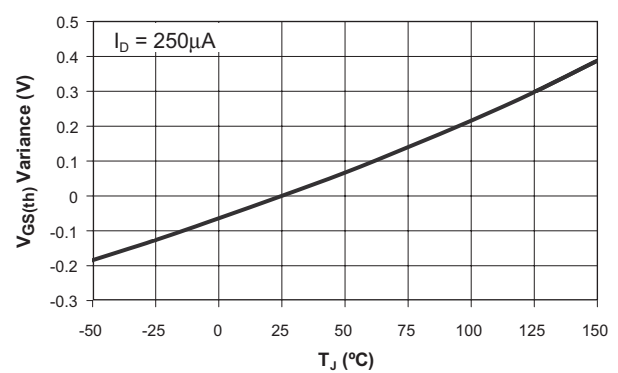
**On-Resistance vs. Gate-to-Source Voltage**



**On-Resistance vs. Junction Temperature**



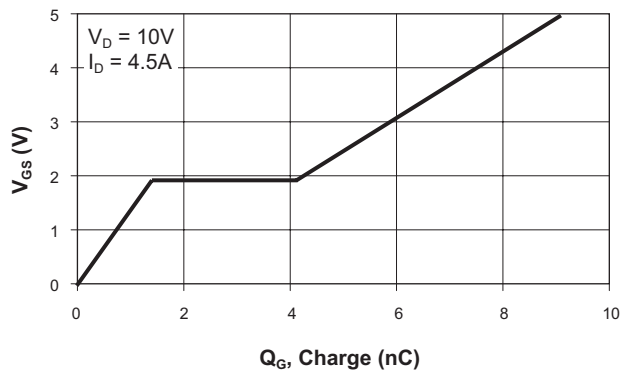
**Threshold Voltage**



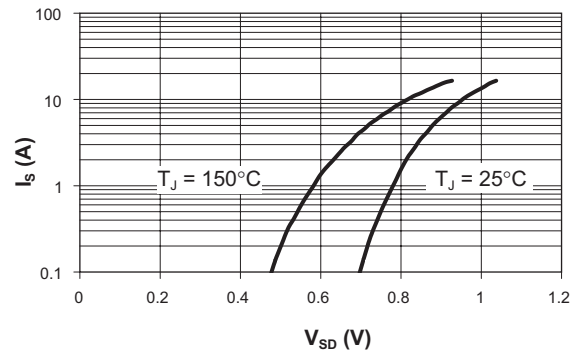
## Typical Characteristics

$T_J = 25^\circ\text{C}$ , unless otherwise noted.

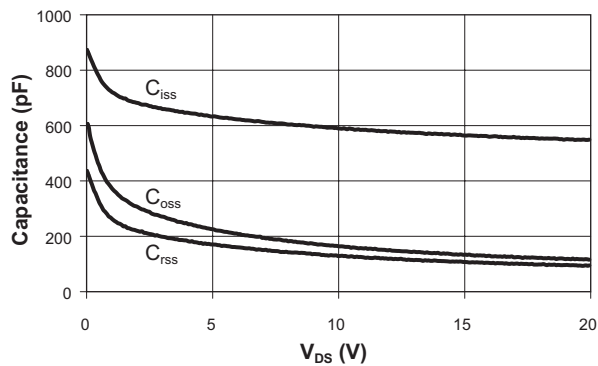
**Gate Charge**



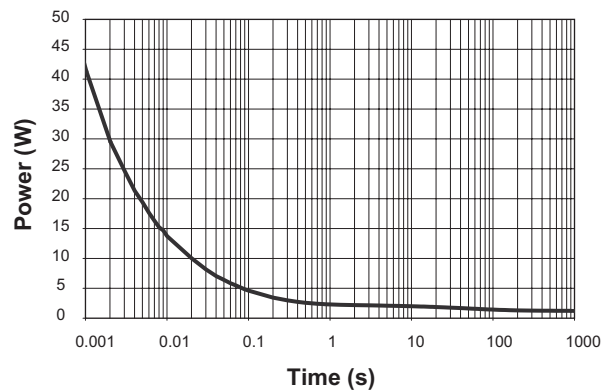
**Source-Drain Diode Forward Voltage**



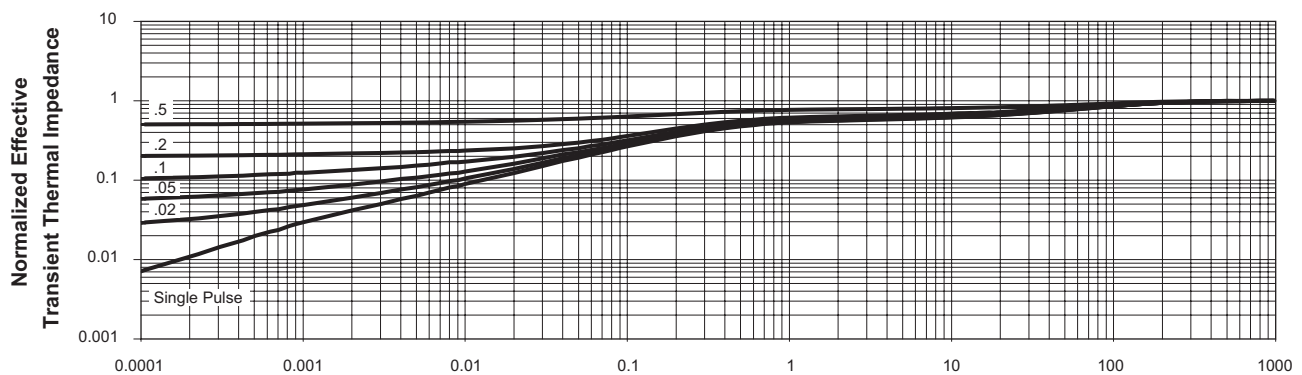
**Capacitance**



**Single Pulse Power, Junction to Ambient**



**Transient Thermal Response, Junction to Ambient**

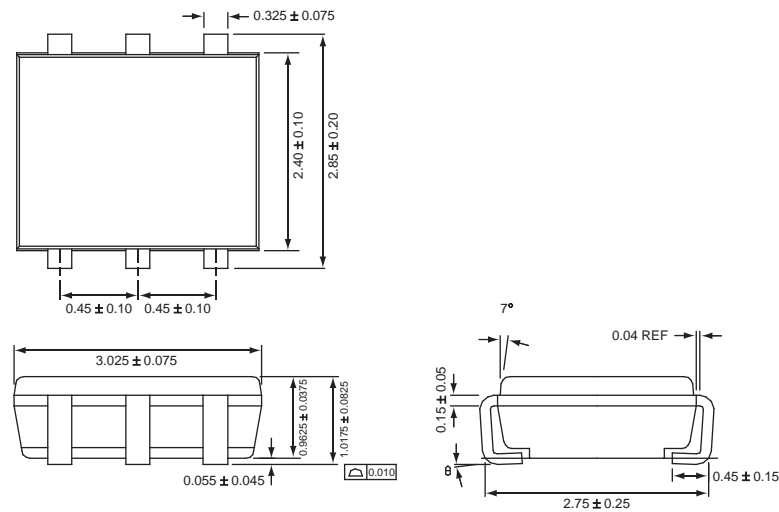


## Ordering Information

Package	Marking <sup>1</sup>	Part Number (Tape and Reel) <sup>2</sup>
TSOP-6	KEXYY	<b>AAT8343IDU-T1</b>

## Package Information

### TSOP-6



All dimensions in millimeters.

1. XYY = assembly and date code.

2. Sample stock is generally held on part numbers listed in **BOLD**.

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