

## Features

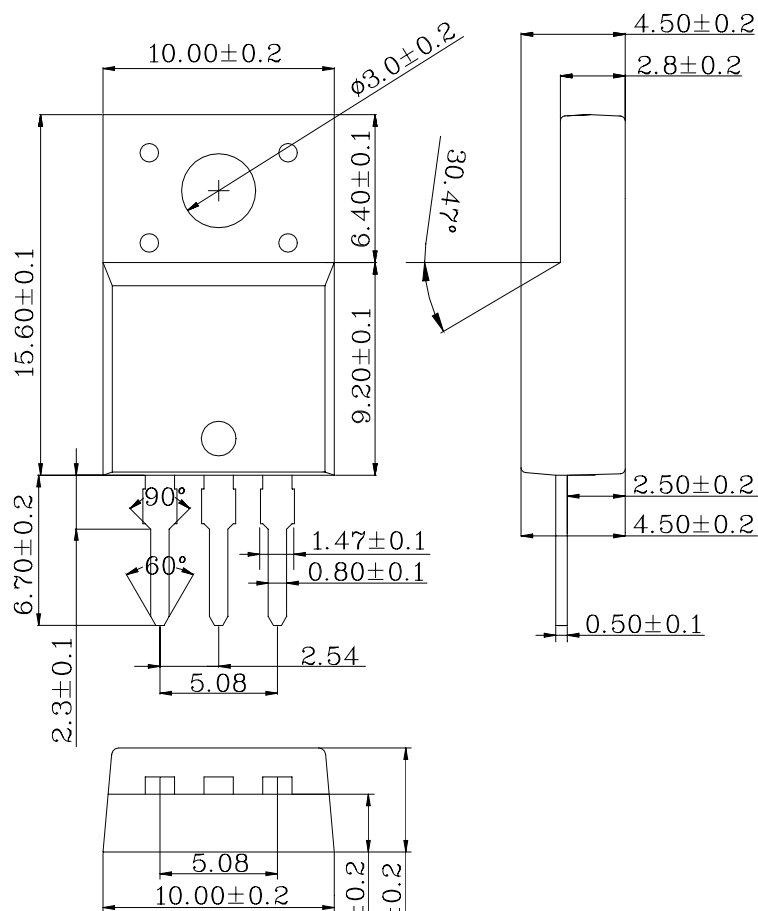
- Avalanche rugged technology.
- Low input capacitance.
- Improved gate charge.
- Low leakage current : 10uA (Max.) @  $V_{DS}=500V$ .
- Low  $R_{DS(ON)}$  :  $1.17\Omega$  (Typ.)

## Ordering Information

Type NO.	Marking	Package Code
STK830FC	STK830	TO-220F-3SL

## Outline Dimensions

unit : mm



### PIN Connections

1. Gate
2. Drain
3. Source

## Absolute maximum ratings

Characteristic	Symbol	Rating	Unit
Drain-Source voltage	$V_{DSS}$	500	V
Gate-Source voltage	$V_{GS}$	$\pm 30$	V
Continuous Drain current ( $T_c=25^\circ\text{C}$ )	$I_D$	4.5*	A
Continuous Drain current ( $T_c=100^\circ\text{C}$ )	$I_D$	2.9*	A
Drain Current-Pulsed ①	$I_{DM}$	18	A
Power Dissipation ( $T_c=25^\circ\text{C}$ )	$P_D$	38	W
Linear Derating Factor		0.3	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy ②	$E_{AS}$	270	mJ
Avalanche current ①	$I_{AR}$	4.5	A
Repetitive Avalanche Energy ①	$E_{AR}$	7.3	mJ
Peak Diode Recovery dv/dt	dv/dt	5.5	V/ns
Operating Junction and Storage temperature range	$T_J, T_{stg}$	-55~150	$^\circ\text{C}$
Maximum lead temp. for soldering Purpose, 1/8" from case for 5-seconds	$T_L$	300	$^\circ\text{C}$

\* Limited by Maximum junction Temperature

## Thermal Resistance

Characteristic	Symbol	Typ.	Max	Units
Junction-to-Case	$R_{\theta JC}$		3.31	$^\circ\text{C}/\text{W}$
Case-to-Sink	$R_{\theta CS}$	0.5		
Junction-to-Ambient	$R_{\theta JA}$		62.5	

**Electrical Characteristics (T<sub>c</sub>=25°C unless otherwise specified)**

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-Source breakdown voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0	500			V
Gate-Threshold voltage	V <sub>GS(th)</sub>	I <sub>D</sub> =250μA, V <sub>DS</sub> =5V	2.0		4.0	V
Drain-source leakage current	I <sub>DSS</sub>	V <sub>DS</sub> =500V			10	μA
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±30V			±100	nA
Drain-Source on-resistance ④	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =2.25A			1.5	Ω
Forward transconductance ④	g <sub>fs</sub>	V <sub>DS</sub> =50V, I <sub>D</sub> =2.25A		3.87		S
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz		760	900	pF
Output capacitance	C <sub>oss</sub>			85	100	
Reverse transfer capacitance	C <sub>rss</sub>			15	22	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> =250V, I <sub>D</sub> =4.5A R <sub>G</sub> =12Ω ④⑤		15	40	ns
Rise time	t <sub>r</sub>			16	40	
Turn-off delay time	t <sub>d(off)</sub>			66	140	
Fall time	t <sub>f</sub>			22	55	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> =400V, V <sub>GS</sub> =10V, I <sub>D</sub> =4.5A ④⑤		33	43	nC
Gate-source charge	Q <sub>gs</sub>			4.4		
Gate-drain("Miller")charge	Q <sub>gd</sub>			16.6		

**Source-Drain Diode Ratings and Characteristics**

Characteristic	Symbol	Test Condition	Min	Typ	Max	Units
Continuous source current	I <sub>S</sub>	Integral reverse pn-diode in the MOSFET			4.5	A
Pulsed-source current ①	I <sub>SM</sub>				18	
Diode forward voltage ④	V <sub>SD</sub>	T <sub>J</sub> =25°C, V <sub>GS</sub> =0V, I <sub>S</sub> =4.5A			1.4	V
Reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> =25°C, I <sub>F</sub> =4.5A di <sub>F</sub> /dt=100A/us ④		285		ns
Reverse recovery charge	Q <sub>rr</sub>			2.0		uC

Note ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② L=30mH, I<sub>AS</sub>=4.5A, V<sub>DD</sub>=50V, R<sub>G</sub>=27Ω, starting T<sub>J</sub>=25°C
- ③ I<sub>SD</sub> ≤ 4.5A, di/dt ≤ 130A/us, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub>=25°C
- ④ Pulse Test : Pulse Width=250us, Duty cycle ≤ 2%
- ⑤ Essentially independent of operating temperature

## Electrical Characteristic Curves

Fig. 1  $I_D - V_{DS}$

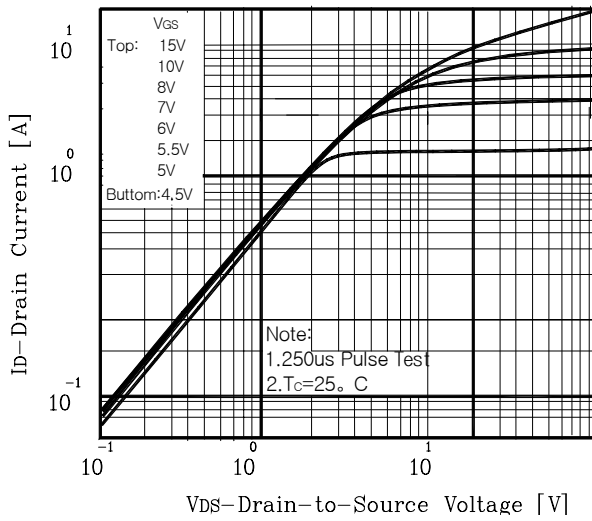


Fig. 2  $I_D - V_{GS}$

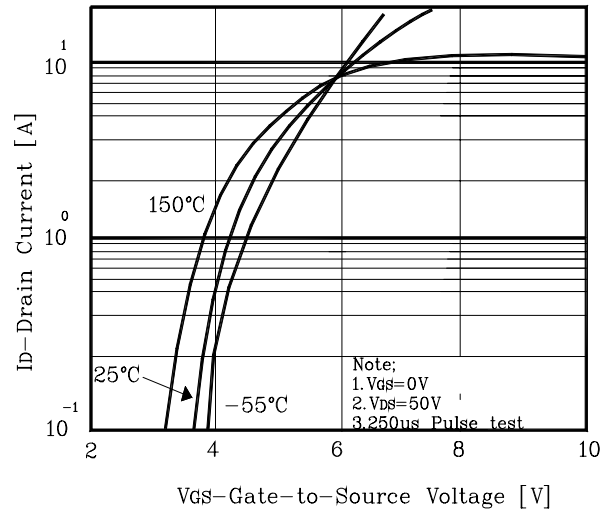


Fig. 3  $R_{DS(on)} - I_D$

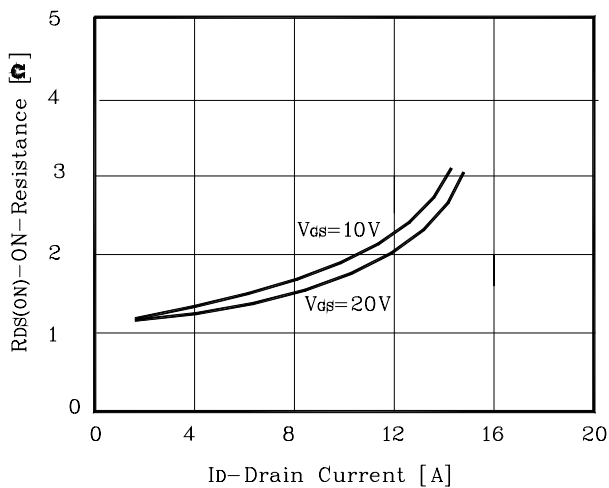


Fig. 4  $I_{DR} - V_{SD}$

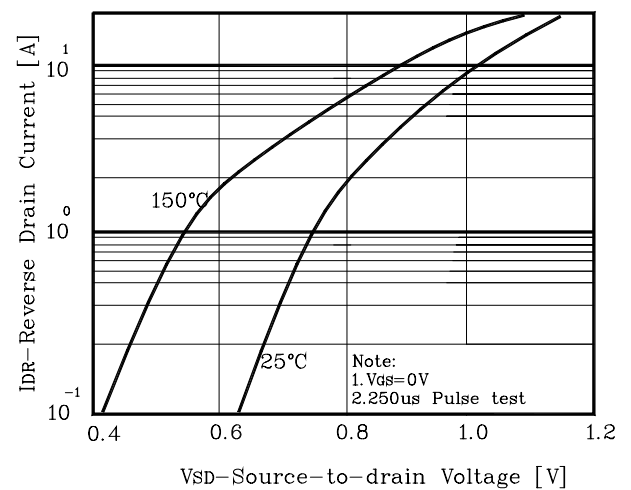


Fig. 5 Capacitance -  $V_{DS}$

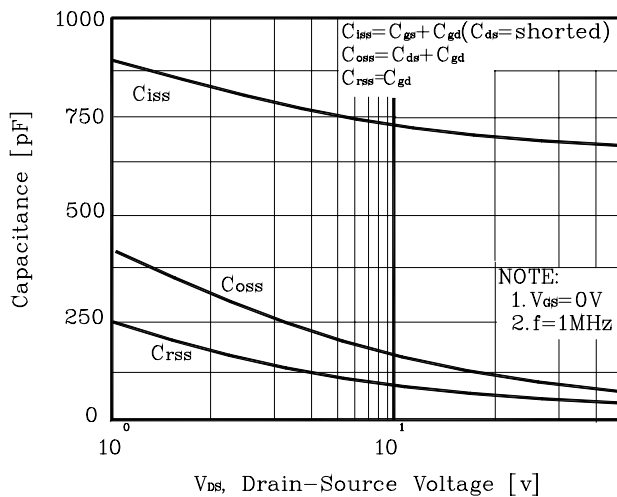
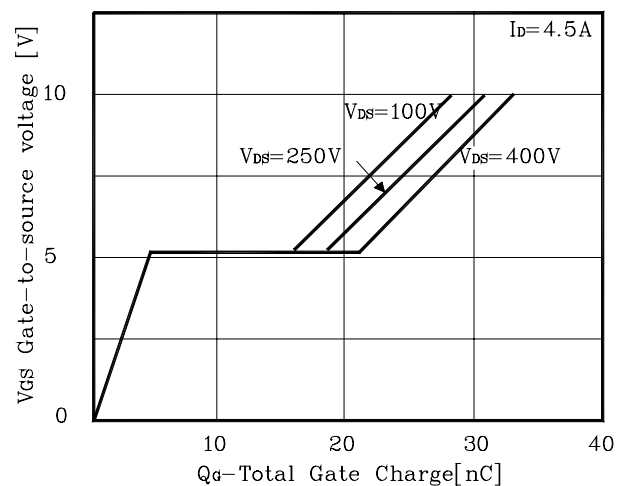
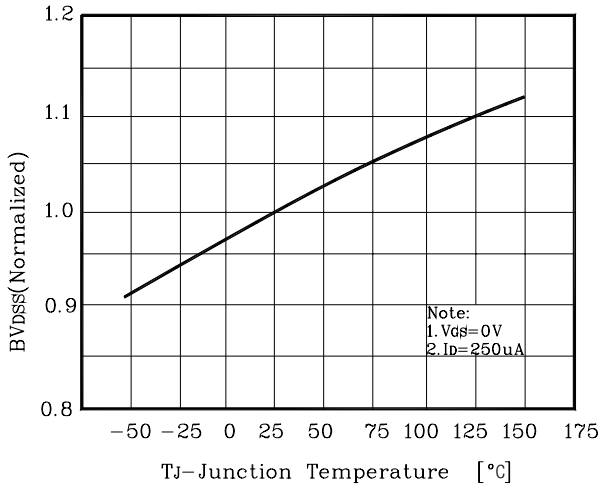


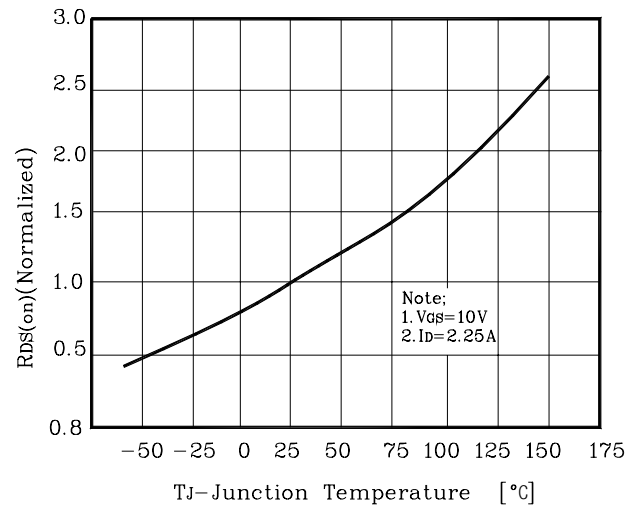
Fig. 6  $V_{GS} - Q_G$



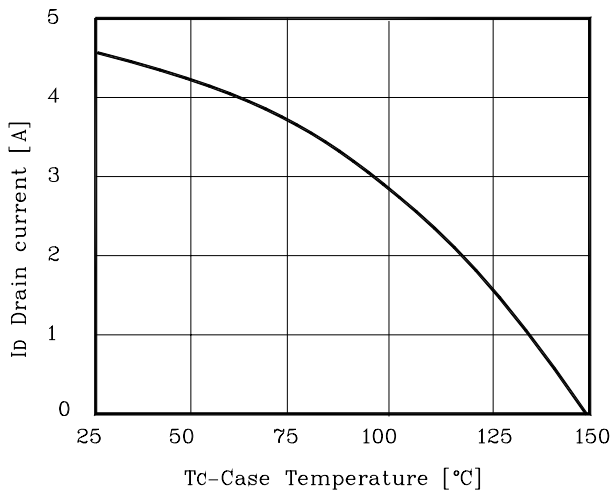
**Fig. 7  $BV_{DSS} - T_J$**



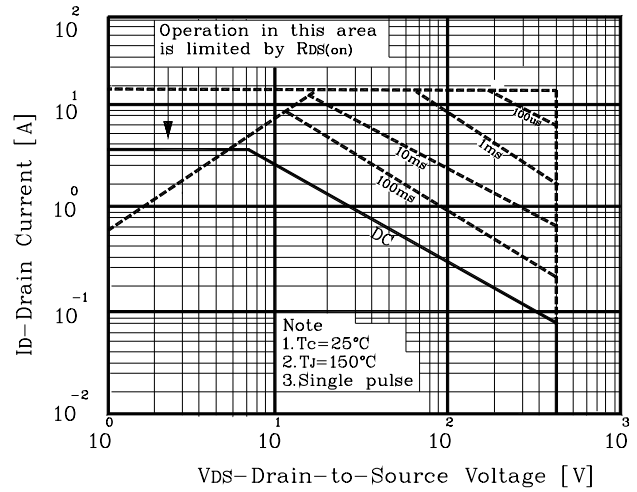
**Fig. 8  $R_{DS(on)} - T_J$**



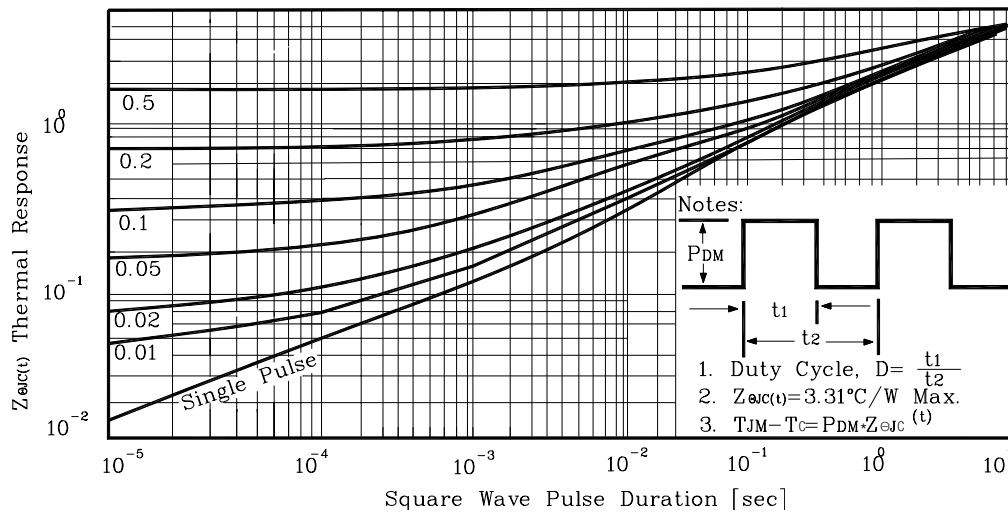
**Fig. 9  $I_D - T_C$**



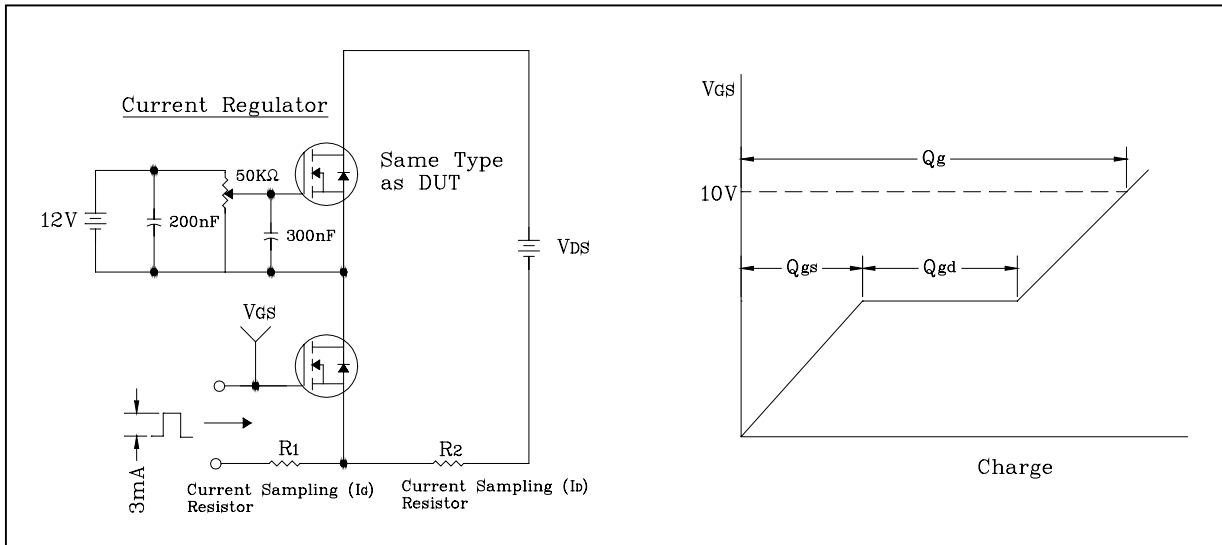
**Fig. 10 Safe operating Area**



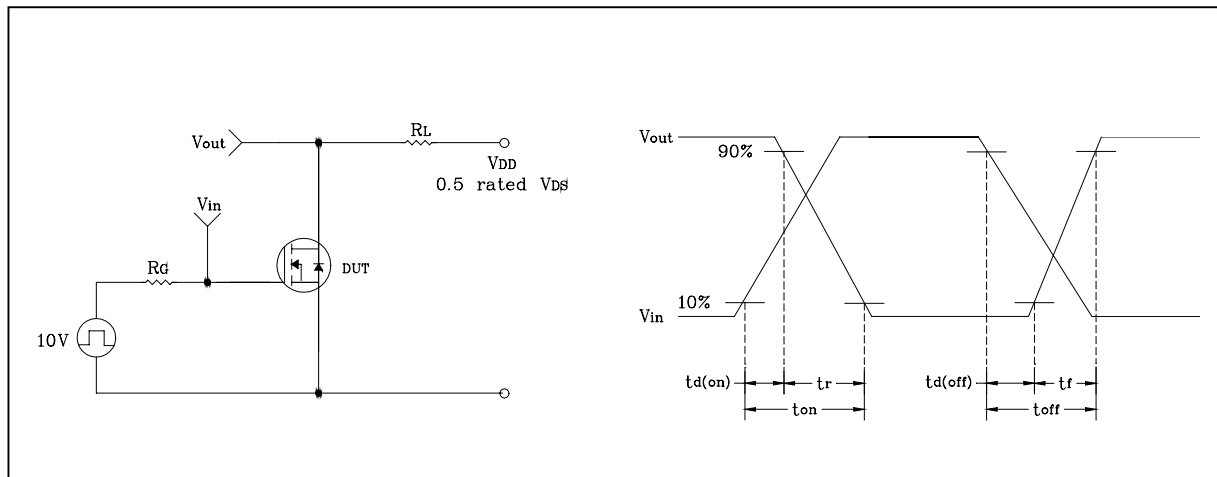
**Fig. 11 Thermal Response**



**Fig. 12 Gate Charge Test Circuit & Waveform**



**Fig. 13 Resistive Switching Test Circuit & Waveform**



**Fig. 14 Unclamped Inductive Switching Test Circuit & Waveform**

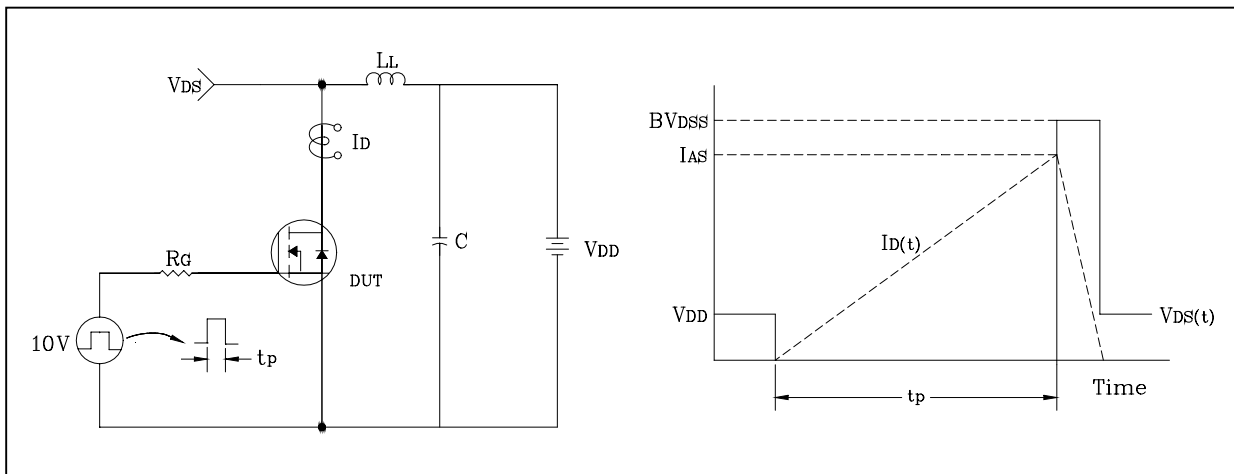
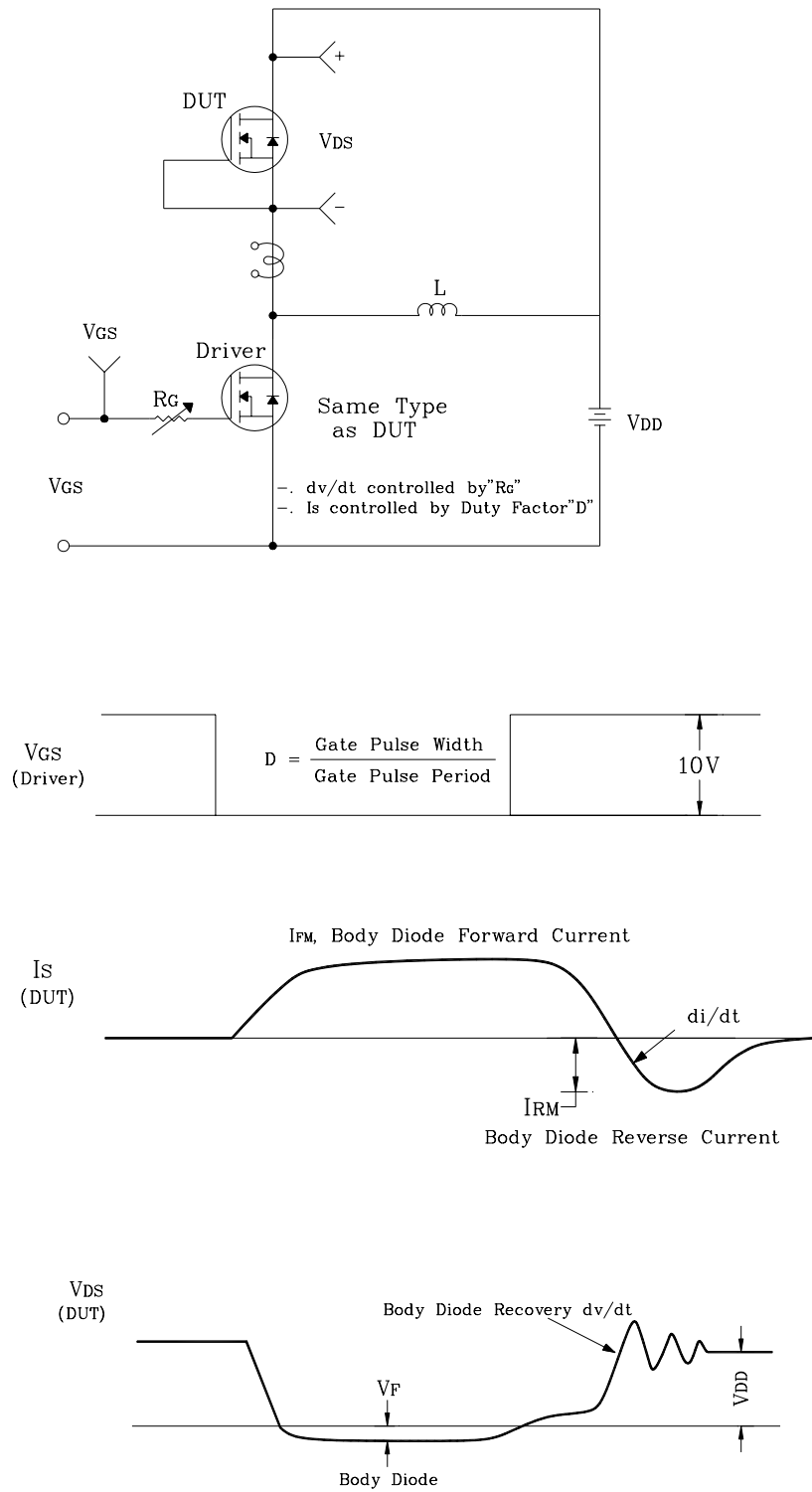


Fig. 15 Peak Diode Recovery dv/dt Test Circuit & Waveform



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