

Description

- High speed switching application.

Features

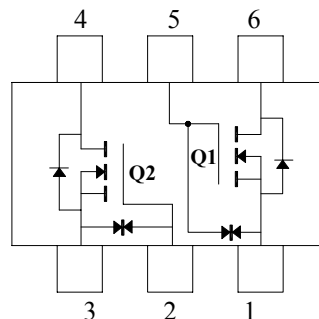
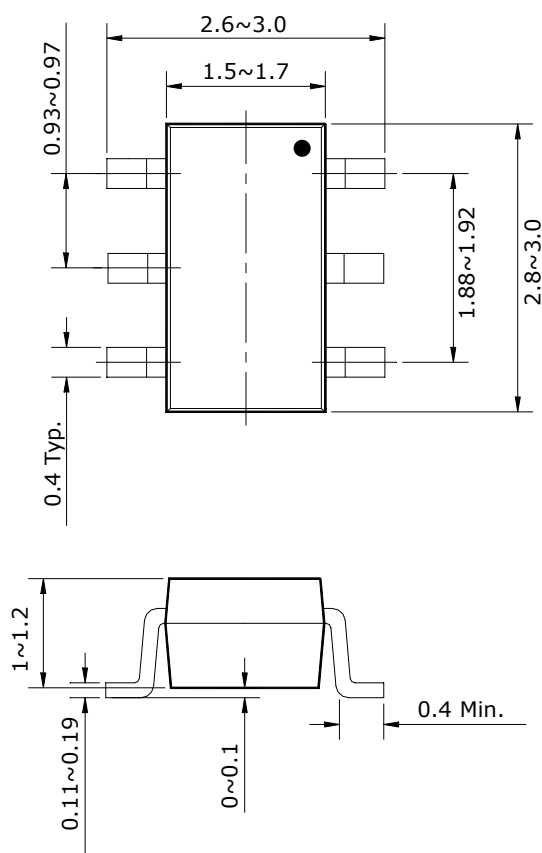
- High density cell design for low $R_{DS(ON)}$.
- Voltage controlled small signal switch
- Include Zener protection for ESD ruggedness.
- Two STK0602 Chips in SOT-26 Package

Ordering Information

Type NO.	Marking	Package Code
SUF623N	623	SOT-26

Outline Dimensions

unit : mm



PIN Connections

1. Source 1
2. Gate 2
3. Source 2
4. Drain 2
5. Gate 1
6. Drain 1

Absolute maximum ratings (Q1,Q2 Common)

Ta=25°C

Characteristic	Symbol	Rating	Unit
Drain-Source voltage	V_{DSS}	60	V
Gate-Source voltage	V_{GS}	±8	V
Maximum Drain current	I_D	200	mA
Pulsed Drain Current	I_{DP}	800	mA
Drain Power dissipation	P_D	200	mW
Operating Junction and Storage temperature range	T_J, T_{stg}	-55~150	°C

Electrical Characteristics (Q1,Q2 Common)

Ta=25°C

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-Source breakdown voltage	BV_{DSS}	$I_D=10\mu A, V_{GS}=0$	60	-	-	V
Gate-Threshold voltage	$V_{GS(th)}$	$I_D=1\mu A, V_{DS}=5V$	0.8	-	1.8	V
Zero Gate voltage drain current	I_{DSS}	$V_{DS}=60V, V_{GS}=0$	-	-	1.0	μA
Gate-body leakage	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 6V$	-	-	±1.0	μA
Drain-Source on-resistance	$R_{DS(on)}$	$V_{GS}=5V, I_D=10mA$	-	2.5	6.0	Ω
		$V_{GS}=10V, I_D=10mA$	-	2.0	4.0	
Forward transconductance	g_{fs}	$V_{DS}=5V, I_D=20mA$	20	65	-	mS
Input capacitance	C_{iss}	$V_{DS}=5V, V_{GS}=0, f=1MHz$	-	26	-	pF
Output capacitance	C_{oss}		-	20	-	
Reverse Transfer capacitance	C_{rss}		-	10	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=5V, I_D=10mA$ $V_{GS}=5V$ $R_L=500\Omega$		150		ns
Rise time	t_r			240		
Turn-off delay time	$t_{d(off)}$		-	200	-	
Fall time	t_f		-	300	-	

Electrical Characteristic Curves

Fig. 1 $I_D - V_{DS}$

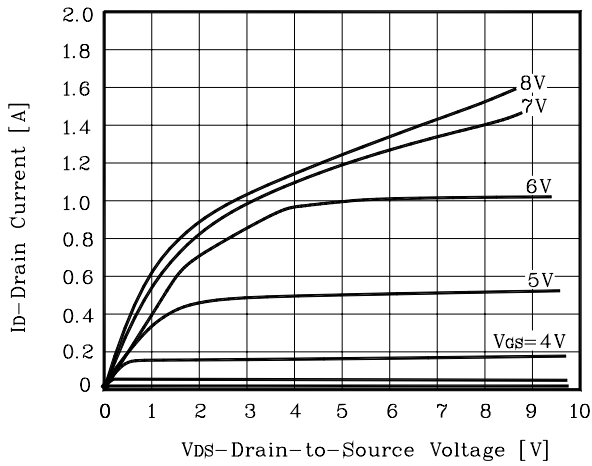


Fig. 2 $I_D - V_{DS}$

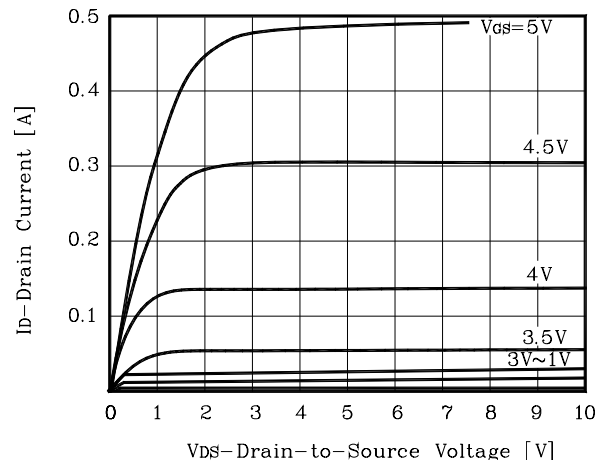


Fig. 3 $I_D - V_{GS}$

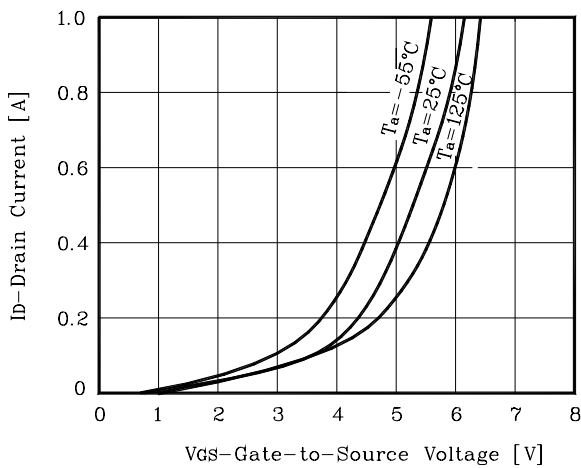


Fig. 4 $r_{DS(on)} - I_D$

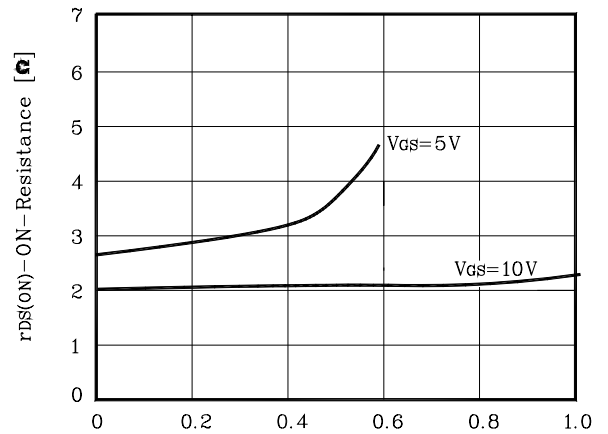


Fig. 5 C - V_{DS}

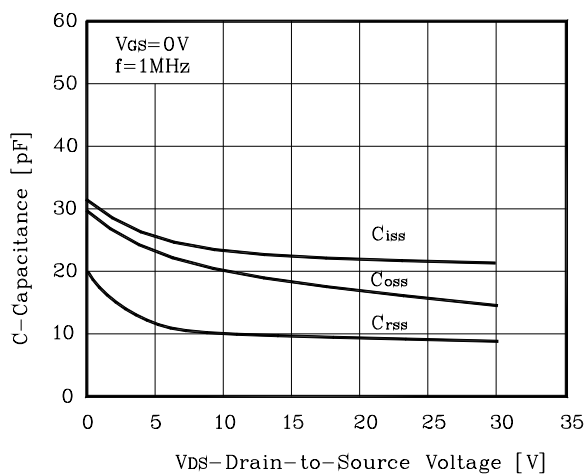
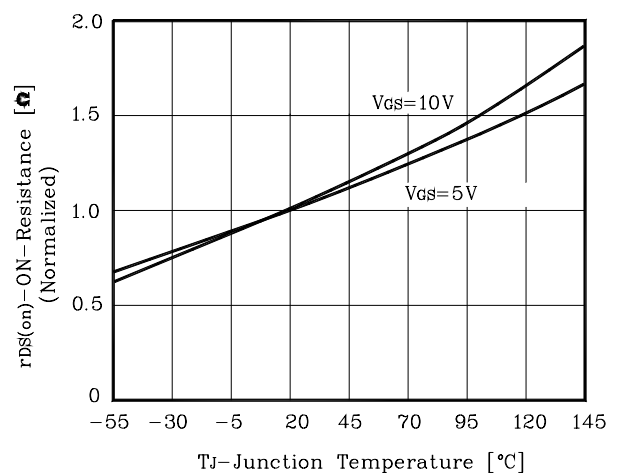


Fig. 6 $r_{DS(on)} - T_J$



Electrical Characteristic Curves

Fig. 7 $r_{DS(on)}$ - V_{GS}

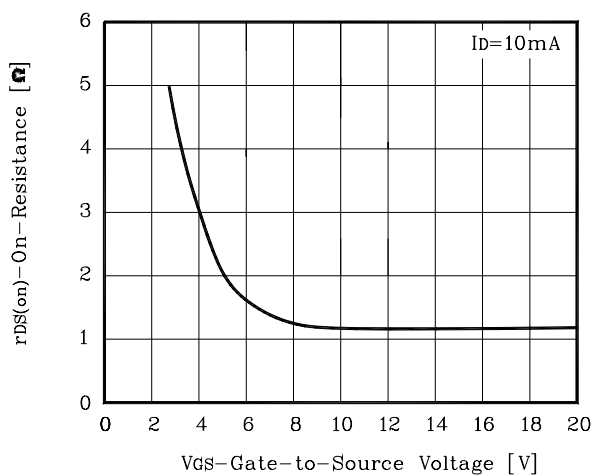


Fig. 8 I_S - V_{SD}

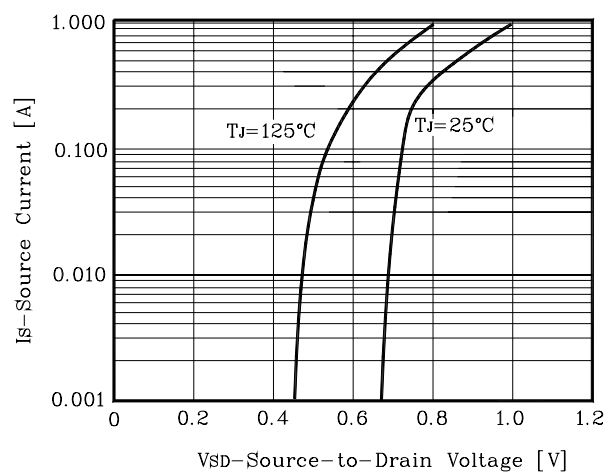
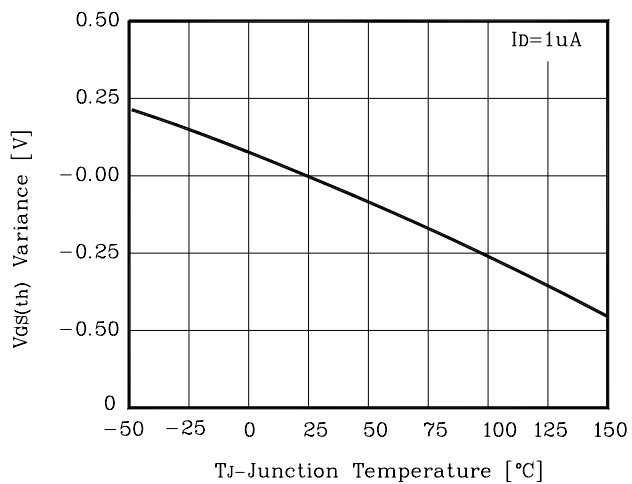


Fig. 9 $V_{GS(th)}$ - T_J



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