



## UNIDIRECTIONAL P-GATE THYRISTOR OVERVOLTAGE AND OVERCURRENT PROTECTOR

### TISP8250D Overvoltage and Overcurrent Protector

Telecommunication System 30 A 10/1000 Protector

**Ion-Implanted Breakdown Region**  
- Precise and Stable Voltage

| Device Name | $V_{DRM}$<br>V | $V_{(BO)}$<br>V |
|-------------|----------------|-----------------|
| TISP8250D   | 250            | 340             |

**Rated for International Surge Wave Shapes**

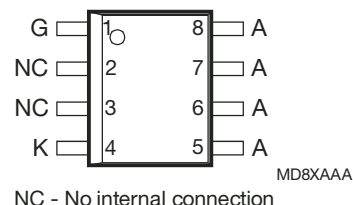
| Wave Shape | Standard      | $I_{PPSM}$<br>A |
|------------|---------------|-----------------|
| 2/10       | GR-1089-CORE  | 75              |
| 0.5/700    | CNET I 31-24  | 40              |
| 10/700     | ITU-T K.20/21 | 40              |
| 10/1000    | GR-1089-CORE  | 30              |

**Functional Replacement for TPP25011**

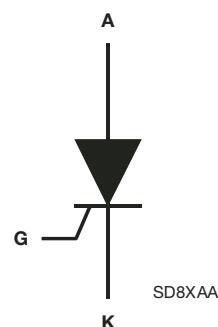


..... UL Recognized Component

**8-SOIC Package (Top View)**



**Device Symbol**



#### Description

The TISP8250D is a P-gate reverse-blocking thyristor (SCR) designed for the protection of telecommunications equipment against overvoltages and overcurrents on the telephone line caused by lightning, a.c. power contact and induction. The fixed voltage and current triggered modes make the TISP8250D particularly suitable for the protection of ungrounded customer premise equipment. Connected across the d.c. side of a telephone set polarity bridge, in fixed voltage mode these devices can protect the ringer in the on-hook condition. In an off-hook condition, either the fixed voltage or current triggered modes can protect the following telephone electronics.

Without external gate activation, the TISP8250D is a fixed voltage protector. The maximum working voltage without clipping is 250 V and the protection voltage is 340 V. Lower values of protection voltage may be set by connecting an avalanche breakdown diode of less than 250 V between the TISP8250D gate and anode (see Figure 2.)

By connecting a small value resistor in series with the line conductor and connecting the TISP8250D gate cathode terminals in parallel with the resistor, conductor overcurrents can gate trigger the TISP8250D into conduction.

Overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on state. Overcurrents develop sufficient voltage across the external gate-cathode resistor to trigger the device into a low-voltage on state. This low-voltage on state causes the current resulting from the overstress to be safely diverted through the device. The high crowbar holding current prevents d.c. latchup as the diverted current subsides.

#### How To Order

| Device    | Package | Carrier              | For Standard Termination Finish Order As | For Lead Free Termination Finish Order As | Marking Code | Standard Quantity |
|-----------|---------|----------------------|--|---|--------------|-------------------|
| TISP8250D | 8-SOIC  | Embossed Tape Reeled | TISP8250DR                               | TISP8250DR-S                              | 8250         | 2500              |
|           |         | Tube                 | TISP8250D                                | TISP8250D-S                               |              | 1500              |

# TISP8250D Overvoltage and Overcurrent Protector

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## Absolute Maximum Ratings, $T_A = 25^\circ\text{C}$ (Unless Otherwise Noted)

| Rating  | Symbol            | Value                      | Unit             |
|---|-------------------|----------------------------|------------------|
| Repetitive peak off-state voltage (see Note 1)  | $V_{\text{DRM}}$  | 250                        | V                |
| Non-repetitive peak impulse current (see Notes 2, 3 and 4)<br>2/10 $\mu\text{s}$ (Telcordia GR-1089-CORE, 2/10 $\mu\text{s}$ waveshape)<br>0.2/310 (CNET I 31-24, 0.5/700 $\mu\text{s}$ waveshape)<br>5/310 $\mu\text{s}$ (ITU-T K.20/21, 10/700 $\mu\text{s}$ voltage waveshape)<br>5/310 $\mu\text{s}$ (FTZ R12, 10/700 $\mu\text{s}$ voltage waveshape)<br>10/1000 $\mu\text{s}$ (Telcordia GR-1089-CORE, 10/1000 $\mu\text{s}$ voltage waveshape) | $I_{\text{PPSM}}$ | 75<br>40<br>40<br>40<br>30 | A                |
| Non-repetitive peak on-state current, 50 Hz (see Notes 2, 3 and 4)<br>10 ms half sine wave<br>1 s rectified sine wave<br>1000 s rectified sine wave   | $I_{\text{TSM}}$  | 5<br>3.5<br>0.7            | A                |
| Junction temperature  | $T_J$             | -40 to +150                | $^\circ\text{C}$ |
| Storage temperature range   | $T_{\text{stg}}$  | -65 to +150                | $^\circ\text{C}$ |

- NOTES: 1. For voltage values at lower temperatures, derate at 0.13 %/ $^\circ\text{C}$ .  
2. Initially the device must be in thermal equilibrium, with  $T_J = 25^\circ\text{C}$ .  
3. The surge may be repeated after the device returns to its initial conditions.  
4. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A printed wiring track widths. Derate current values at -0.61 %/ $^\circ\text{C}$  for ambient temperatures above  $25^\circ\text{C}$ .

## Electrical Characteristics, $T_A = 25^\circ\text{C}$ (Unless Otherwise Noted)

| Parameter  | Test Conditions  | Min | Typ | Max     | Unit          |
|--|--|-----|-----|---------|---------------|
| $I_{\text{DRM}}$ Repetitive peak off-state current | $V_D = V_{\text{DRM}}$<br>$T_A = 25^\circ\text{C}$<br>$T_A = 85^\circ\text{C}$ |     |     | 5<br>10 | $\mu\text{A}$ |
| $V_{\text{(BO)}}$ Breakover voltage                | $dv/dt = 250 \text{ V/ms}$ , $R_{\text{SOURCE}} = 300 \Omega$                  |     |     | 340     | V             |
| $I_{\text{(BO)}}$ Breakover current                | $dv/dt = 250 \text{ V/ms}$ , $R_{\text{SOURCE}} = 300 \Omega$                  | 15  |     | 200     | mA            |
| $I_H$ Holding current                              | $I_T = 5 \text{ A}$ , $di/dt = -30 \text{ mA/ms}$                              | 180 |     |         | mA            |
| $V_{\text{GK}}$ Gate-cathode voltage               | $I_G = 30 \text{ mA}$  | 0.6 |     | 1.2     | V             |
| $I_{\text{GT}}$ Gate trigger current               | $V_{\text{AK}} = 100 \text{ V}$  |     |     | 40      | mA            |
| $I_D$ Off-state current                            | $V_D = 60 \text{ V}$   |     |     | 5       | $\mu\text{A}$ |
| $C_O$ Off-state capacitance                        | $f = 1 \text{ MHz}$ , $V_d = 1 \text{ V rms}$ , $V_D = 5 \text{ V}$            |     |     | 100     | pF            |

## Thermal Characteristics, $T_A = 25^\circ\text{C}$ (Unless Otherwise Noted)

| Parameter  | Test Conditions  | Min | Typ | Max | Unit               |
|--|--|-----|-----|-----|--------------------|
| $R_{\theta\text{JA}}$ Junction to ambient thermal resistance | EIA/JESD51-3 PCB, $I_T = I_{\text{TSM}(1000)}$<br>(see Note 5) |     |     | 170 | $^\circ\text{C/W}$ |

- NOTE 5. EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5A rated printed wiring track widths.

# TISP8250D Overvoltage and Overcurrent Protector

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## Parameter Measurement Information

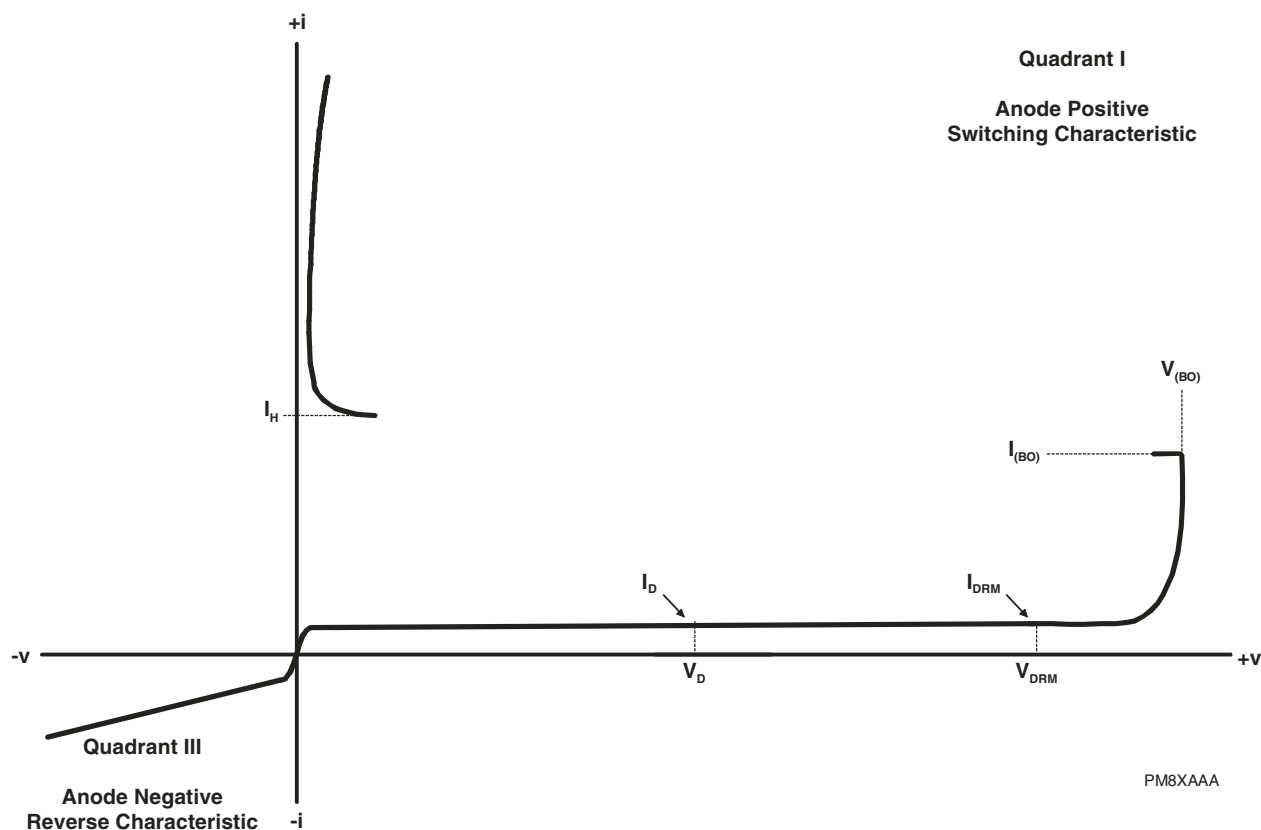


Figure 1. Voltage-Current Characteristic for A and K Terminals  
All Measurements are Referenced to the K Terminal

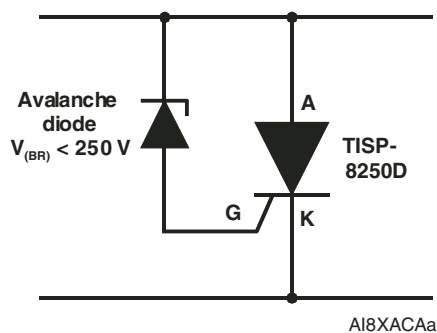


Figure 2. Overvoltage Protection Circuit

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