

Quad, Serial Input, 12-Bit, Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **LOW POWER:** 3mW
- **SETTLING TIME:** 10 μ s to 0.012%
- **12-BIT LINEARITY AND MONOTONICITY:** -40°C to $+85^{\circ}\text{C}$
- **DOUBLE-BUFFERED DATA INPUTS**
- **SO-16 or SSOP-20 PACKAGES**
- **SINGLE-SUPPLY +3V OPERATION**

APPLICATIONS

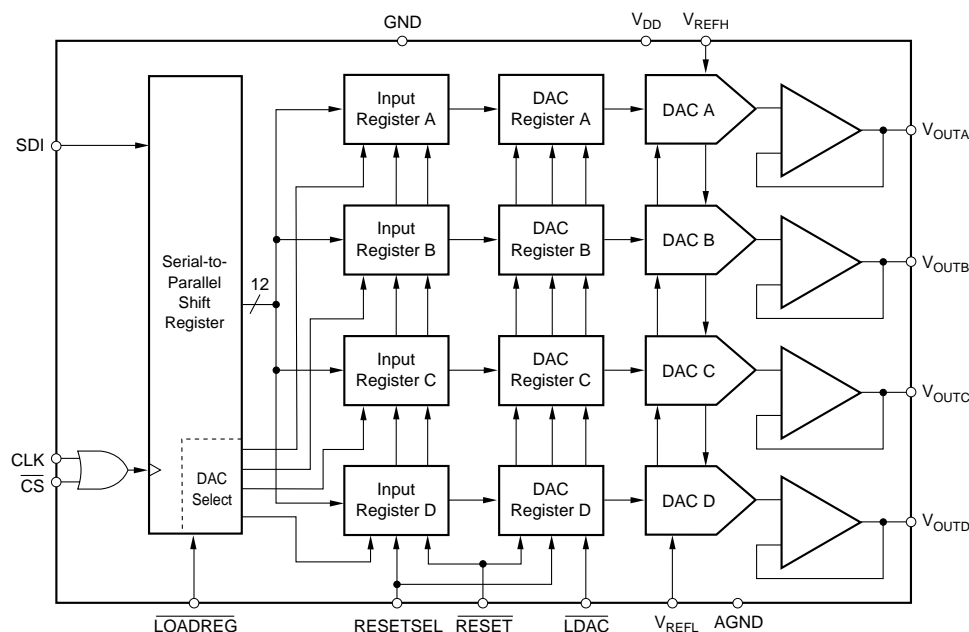
- **PROCESS CONTROL**
- **ATE PIN ELECTRONICS**
- **CLOSED-LOOP SERVO-CONTROL**
- **MOTOR CONTROL**
- **DATA ACQUISITION SYSTEMS**
- **DAC-PER-PIN PROGRAMMERS**

DESCRIPTION

The DAC7617 is a quad, serial input, 12-bit, voltage output Digital-to-Analog Converter (DAC) with guaranteed 12-bit monotonic performance over the -40°C to $+85^{\circ}\text{C}$ temperature range. An asynchronous reset clears all registers to either mid-scale (800_{H}) or zero-scale (000_{H}), selectable via the RESETSEL pin. The individual DAC inputs are double buffered to allow

for simultaneous update of all DAC outputs. The device is powered from a single +3V supply.

Low power and small size makes the DAC7617 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The device is available in SO-16 and SSOP-20 packages and is guaranteed over the -40°C to $+85^{\circ}\text{C}$ temperature range.



SPECIFICATIONS

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = +3\text{V}$, $V_{REFH} = +1.25\text{V}$, and $V_{REFL} = 0\text{V}$, unless otherwise noted.

| | | DAC7617E, U | | | DAC7617EB, UB | | | |
|---|---|-------------------------------|-------------------------------------|--|---------------------------------------|---------------------------------------|---|---|
| PARAMETER | CONDITIONS | MIN | TYP | MAX | MIN | TYP | MAX | UNITS |
| ACCURACY Linearity Error ⁽¹⁾ Linearity Matching ⁽³⁾ Differential Linearity Error Monotonicity Zero-Scale Error Zero-Scale Drift Zero-Scale Matching ⁽³⁾ Full-Scale Error Full-Scale Matching ⁽³⁾ Power Supply Rejection | Code = 00A _H Code = FFF _H | 12 | 5 ±1 ±1 30 | ±2 ±2 ±1 ±2.4 10 ±2 ±2.4 ±2 | * | * * * * * | ±1 ±1 ±1 * * ±1.2 * ±1.2 | LSB ⁽²⁾ LSB LSB Bits mV ppm/°C mV mV mV ppm/V |
| ANALOG OUTPUT Voltage Output ⁽⁴⁾ Output Current Load Capacitance Short-Circuit Current Short-Circuit Duration | No Oscillation | V _{REFL} −625 | 100 +8, −2 Indefinite | V _{REFH} +625 | * * | * * * | * * | V μA pF mA |
| REFERENCE INPUT V _{REFH} Input Range V _{REFL} Input Range | | 0 0 | | +1.25 | * * | | * | V V |
| DYNAMIC PERFORMANCE Settling Time Channel-to-Channel Crosstalk Output Noise Voltage | To ±0.012% Full-Scale Step On Any Other DAC Bandwidth: 0Hz to 1MHz | | 5 0.1 65 | 10 | | * * * | * * * | μs LSB nV/√Hz |
| DIGITAL INPUT/OUTPUT Logic Family Logic Levels V _{IH} V _{IL} Data Format | I _{IH} ≤ 10μA I _{IL} ≤ 10μA | V _{DD} • 0.7 −0.3 | CMOS Straight Binary | V _{DD} V _{DD} • 0.3 | * * | * * | * * | V V |
| POWER SUPPLY REQUIREMENTS V _{DD} I _{DD} Power Dissipation | | 3.0 | 3.3 0.8 2.4 | 3.6 1 3 | * * | * * * | * * * | V mA mW |
| TEMPERATURE RANGE Specified Performance | | −40 | | +85 | * | | * | °C |

* Specification same as DAC7617E, U.

NOTES: (1) Specification applies at code 00A_H and above. (2) LSB means Least Significant Bit, with V_{REFH} equal to +1.25V and V_{REFL} equal to 0V, one LSB is 0.305mV. (3) All DAC outputs will match within the specified error band. (4) Ideal output voltage does not take into account zero or full-scale error.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | |
|---|-----------------------------|
| V_{DD} to GND | –0.3V to +5.5V |
| V_{REFL} to GND | –0.3V to (V_{DD} + 0.3V) |
| V_{DD} to V_{REFH} | –0.3V to V_{DD} |
| V_{REFH} to V_{REFL} | –0.3V to V_{DD} |
| Digital Input Voltage to GND | –0.3V to V_{DD} + 0.3V |
| Maximum Junction Temperature | +150°C |
| Operating Temperature Range | –40°C to +85°C |
| Storage Temperature Range | –65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

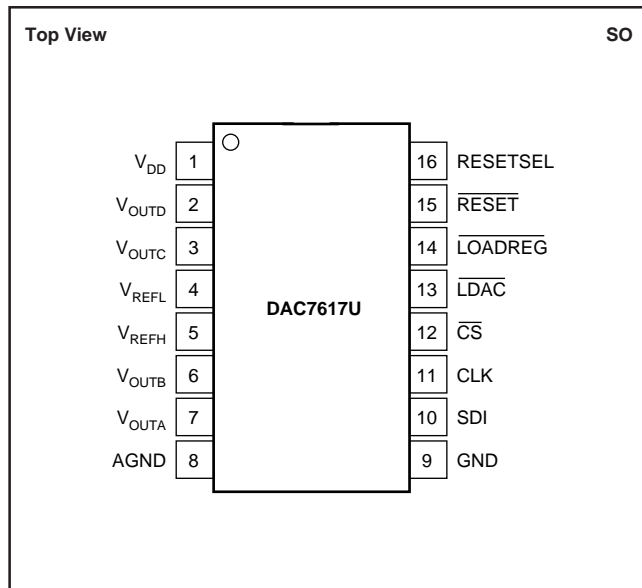
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

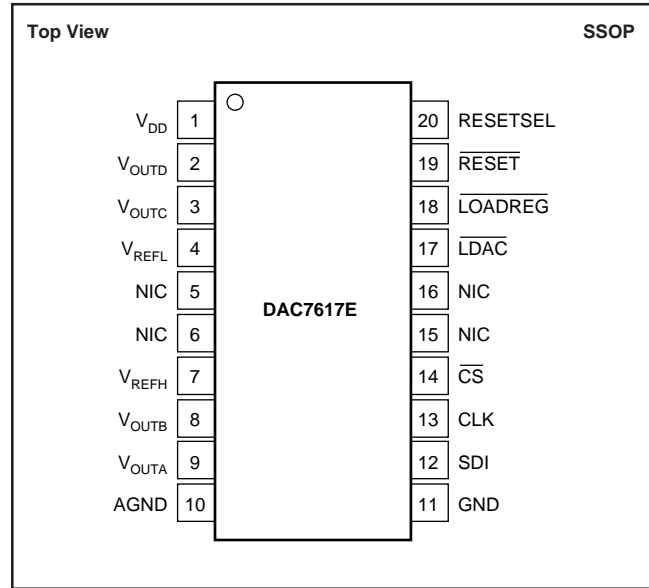
| PRODUCT | MAXIMUM LINEARITY ERROR (LSB) | MAXIMUM DIFFERENTIAL LINEARITY (LSB) | PACKAGE | PACKAGE DRAWING NUMBER | SPECIFICATION TEMPERATURE RANGE | ORDERING NUMBER ⁽¹⁾ | TRANSPORT MEDIA |
|----------------|-------------------------------|--------------------------------------|--------------|------------------------|---------------------------------|--------------------------------|------------------------|
| DAC7617U " | ±2 " | ±1 " | SO-16 " | 211 " | –40°C to +85°C " | DAC7617U DAC7617U/1K | Rails Tape and Reel |
| DAC7617UB " | ±1 " | ±1 " | SO-16 " | 211 " | –40°C to +85°C " | DAC7617UB DAC7617UB/1K | Rails Tape and Reel |
| DAC7617E " | ±2 " | ±1 " | SSOP-20 " | 334 " | –40°C to +85°C " | DAC7617E DAC7617E/1K | Rails Tape and Reel |
| DAC7617EB " | ±1 " | ±1 " | SSOP-20 " | 334 " | –40°C to +85°C " | DAC7617EB DAC7617EB/1K | Rails Tape and Reel |

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of “DAC7617EB/1K” will get a single 1000-piece Tape and Reel.

PIN CONFIGURATION—U Package



PIN CONFIGURATION—E Package



PIN DESCRIPTIONS—U Package

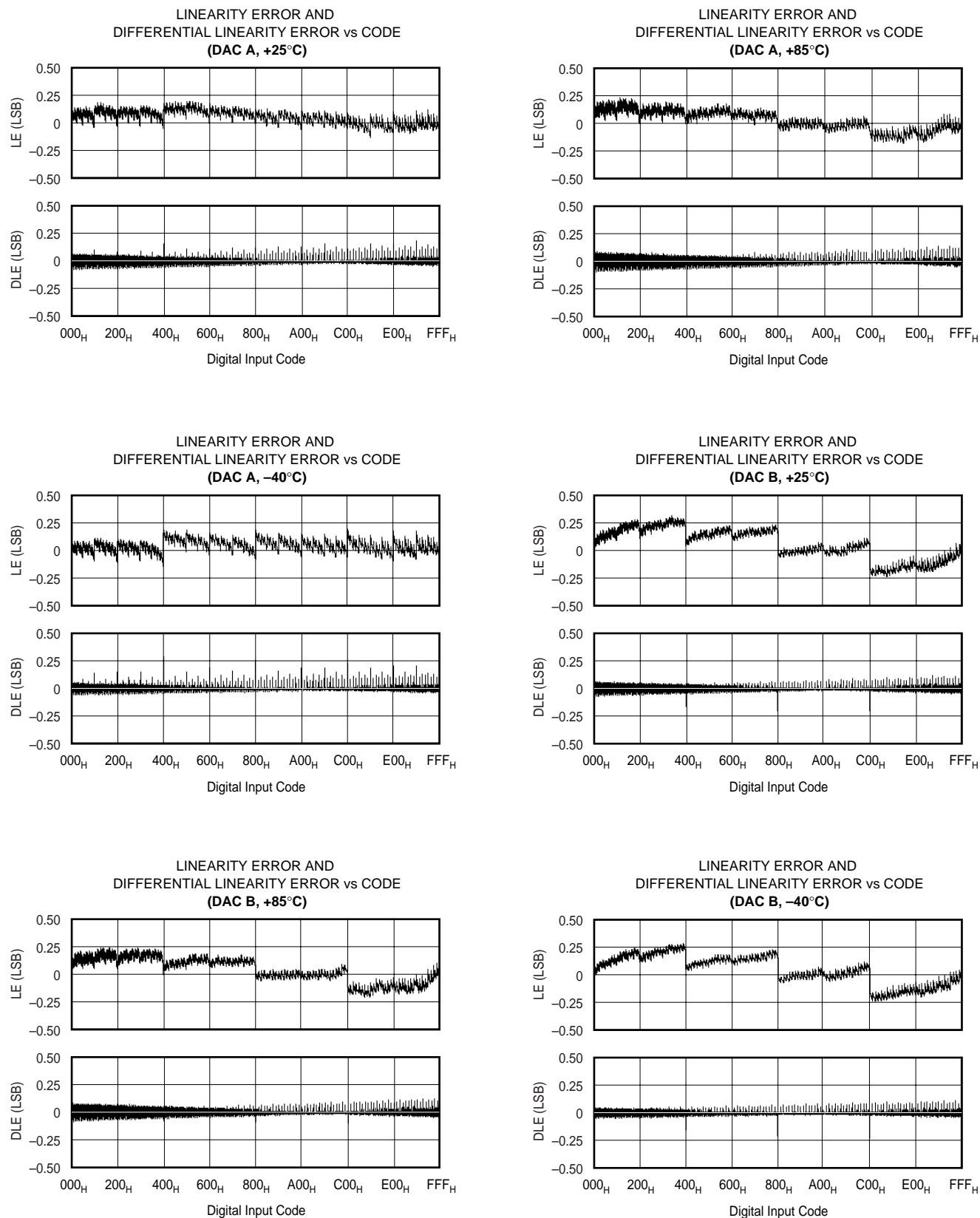
| PIN | LABEL | DESCRIPTION |
|-----|----------------------|--|
| 1 | V_{DD} | Positive Analog Supply Voltage, +3V nominal. |
| 2 | V_{OUTD} | DAC D Voltage Output |
| 3 | V_{OUTC} | DAC C Voltage Output |
| 4 | V_{REFL} | Reference Input Voltage Low. Sets minimum output voltage for all DACs. |
| 5 | V_{REFH} | Reference Input Voltage High. Sets maximum output voltage for all DACs. |
| 6 | V_{OUTB} | DAC B Voltage Output |
| 7 | V_{OUTA} | DAC A Voltage Output |
| 8 | AGND | Analog Ground |
| 9 | GND | Ground |
| 10 | SDI | Serial Data Input |
| 11 | CLK | Serial Data Clock |
| 12 | \overline{CS} | Chip Select Input |
| 13 | \overline{LDAC} | All DAC registers become transparent when \overline{LDAC} is LOW. They are in the latched state when \overline{LDAC} is HIGH. |
| 14 | $\overline{LOADREG}$ | The selected input register becomes transparent when $\overline{LOADREG}$ is LOW. It is in the latched state when $\overline{LOADREG}$ is HIGH. |
| 15 | \overline{RESET} | Asynchronous Reset Input. Sets DAC and input registers to either zero-scale (000 _H) or mid-scale (800 _H) when LOW. RESETSEL determines which code is active. |
| 16 | RESETSEL | When LOW, a LOW on \overline{RESET} will cause the DAC and input registers to be set to code 000 _H . When RESETSEL is HIGH, a LOW on \overline{RESET} will set the registers to code 800 _H . |

PIN DESCRIPTIONS—E Package

| PIN | LABEL | DESCRIPTION |
|-----|----------------------|--|
| 1 | V_{DD} | Positive Analog Supply Voltage, +3V nominal. |
| 2 | V_{OUTD} | DAC D Voltage Output |
| 3 | V_{OUTC} | DAC C Voltage Output |
| 4 | V_{REFL} | Reference Input Voltage Low. Sets minimum output voltage for all DACs. |
| 5 | NIC | Not Internally Connected. |
| 6 | NIC | Not Internally Connected. |
| 7 | V_{REFH} | Reference Input Voltage High. Sets maximum output voltage for all DACs. |
| 8 | V_{OUTB} | DAC B Voltage Output |
| 9 | V_{OUTA} | DAC A Voltage Output |
| 10 | AGND | Analog Ground |
| 11 | GND | Ground |
| 12 | SDI | Serial Data Input |
| 13 | CLK | Serial Data Clock |
| 14 | \overline{CS} | Chip Select Input |
| 15 | NIC | Not Internally Connected. |
| 16 | NIC | Not Internally Connected. |
| 17 | \overline{LDAC} | All DAC registers becomes transparent when \overline{LDAC} is LOW. They are in the latched state when \overline{LDAC} is HIGH. |
| 18 | $\overline{LOADREG}$ | The selected input register becomes transparent when $\overline{LOADREG}$ is LOW. It is in the latched state when $\overline{LOADREG}$ is HIGH. |
| 19 | \overline{RESET} | Asynchronous Reset Input. Sets all DAC registers to either zero-scale (000 _H) or mid-scale (800 _H) when LOW. RESETSEL determines which code is active. |
| 20 | RESETSEL | When LOW, a LOW on \overline{RESET} will cause all DAC registers to be set to code 000 _H . When RESETSEL is HIGH, a LOW on \overline{RESET} will set the registers to code 800 _H . |

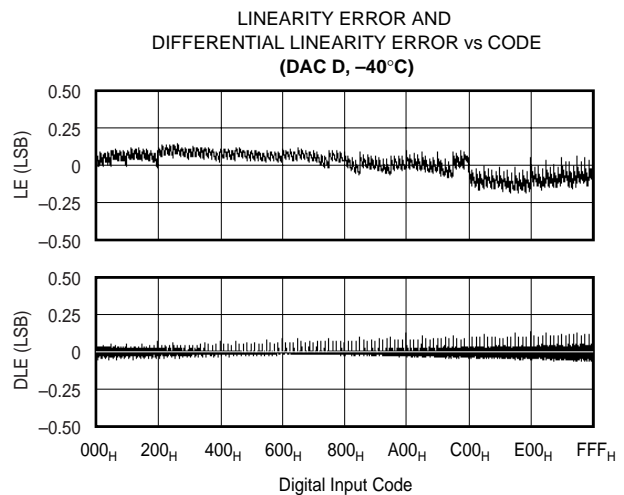
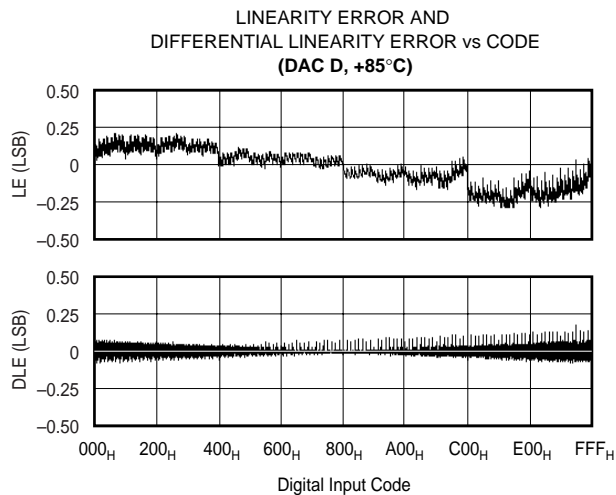
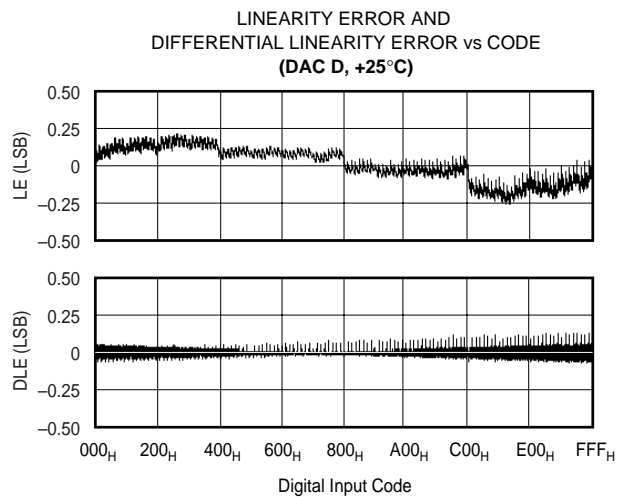
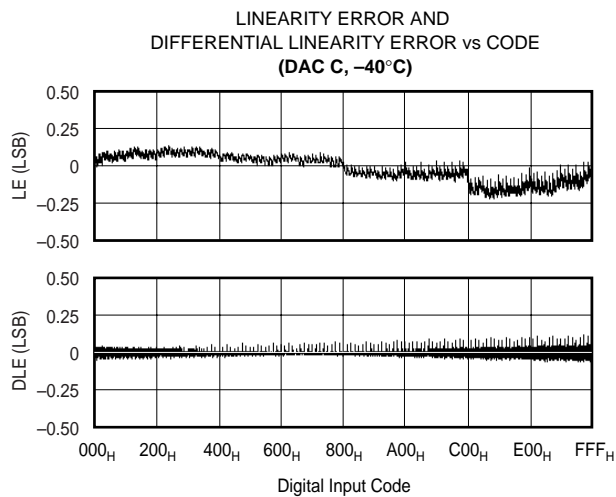
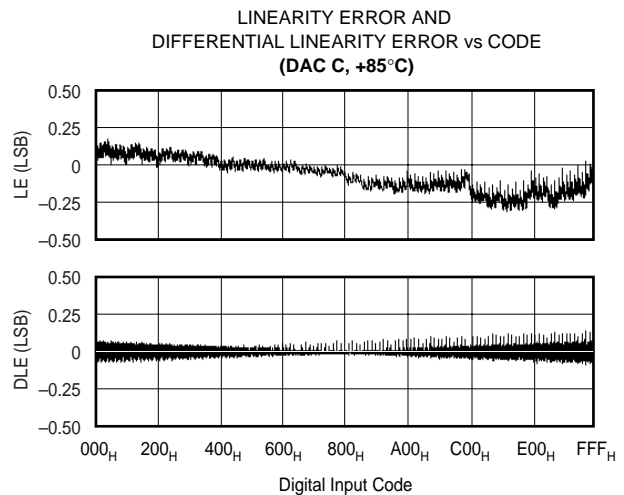
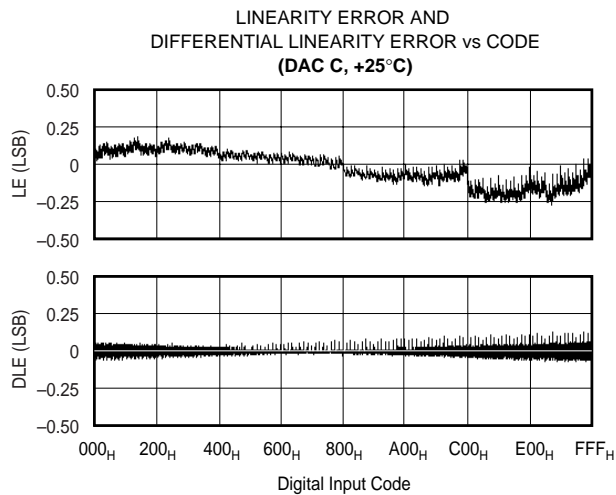
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_{DD} = +3\text{V}$, $V_{REFH} = +1.25\text{V}$, and $V_{REFL} = 0\text{V}$, representative unit, unless otherwise specified.



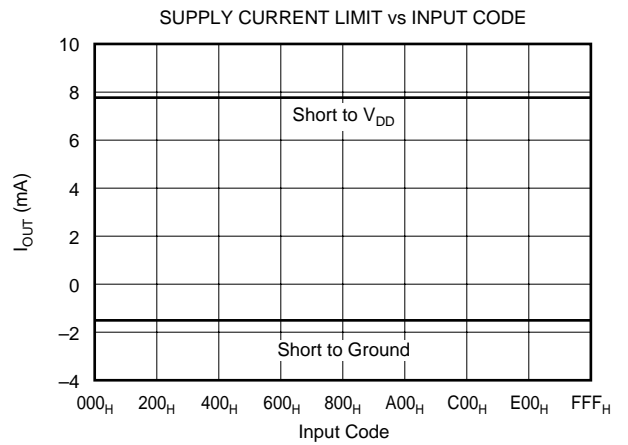
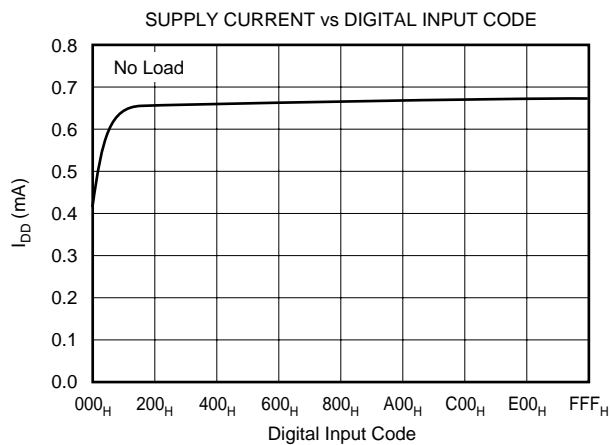
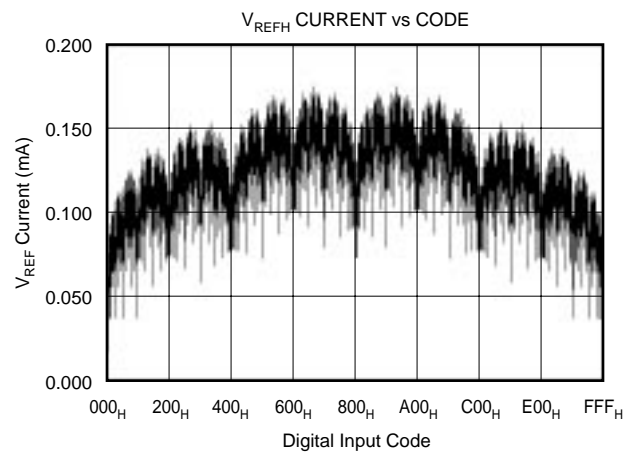
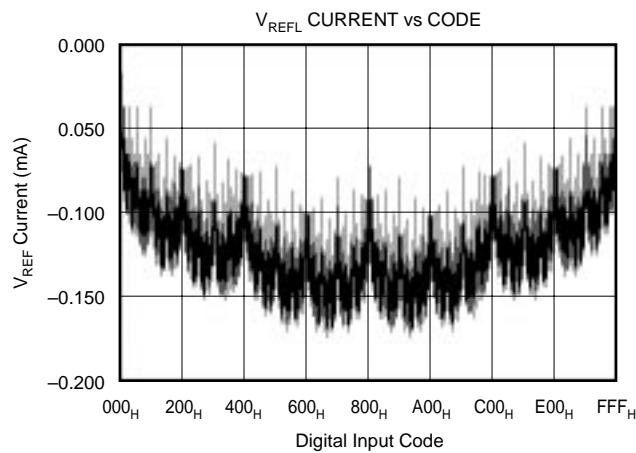
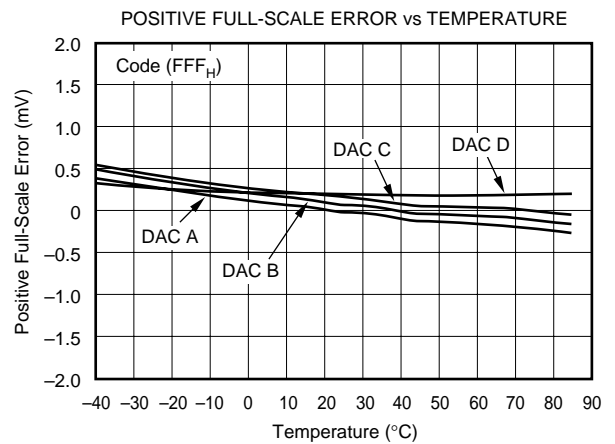
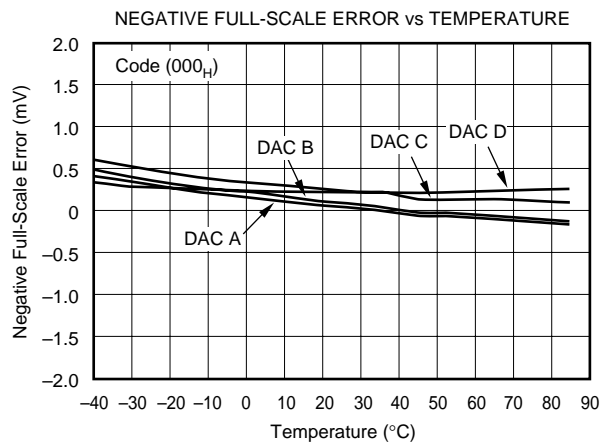
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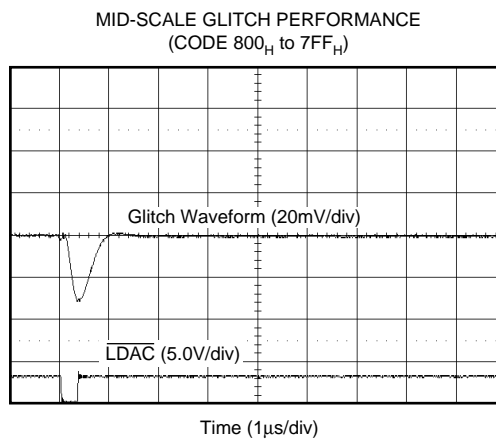
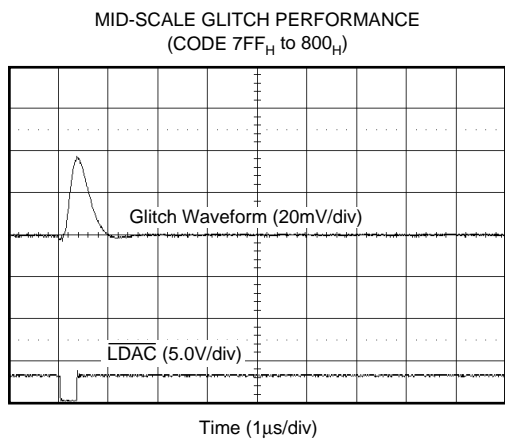
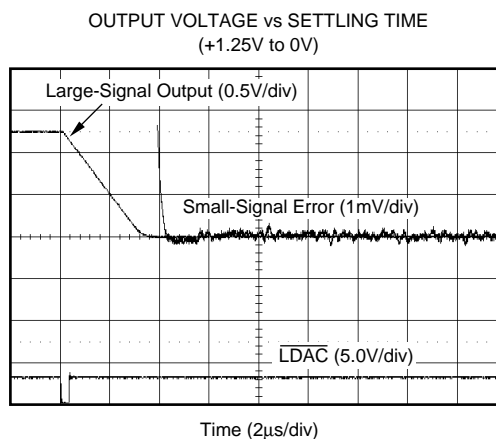
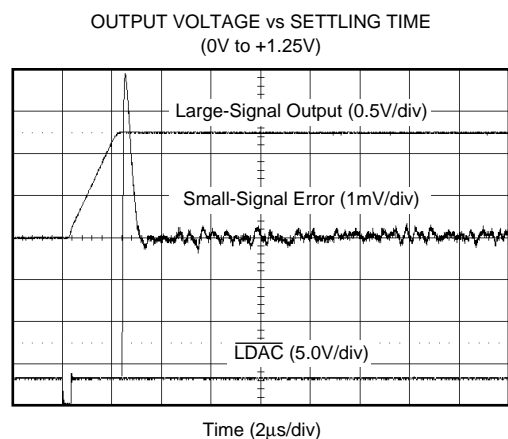
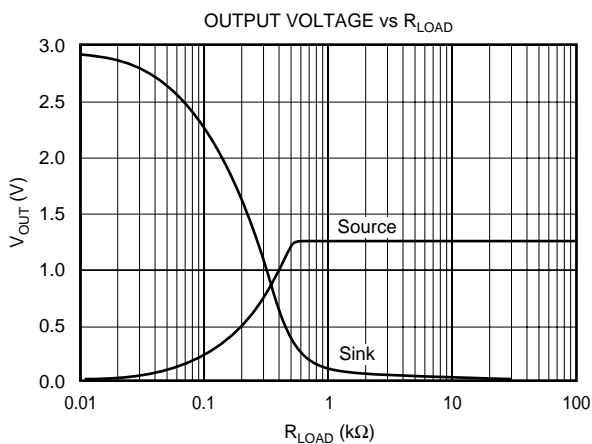
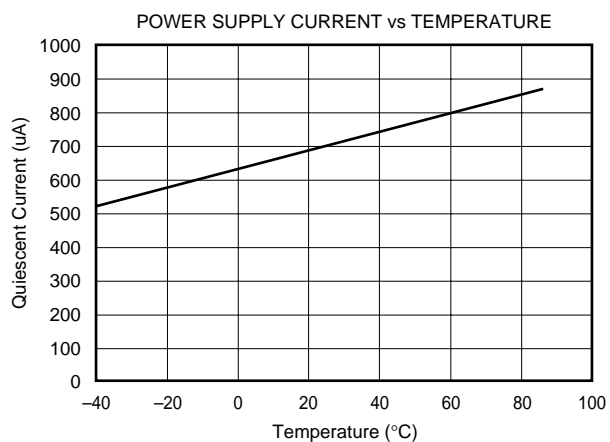
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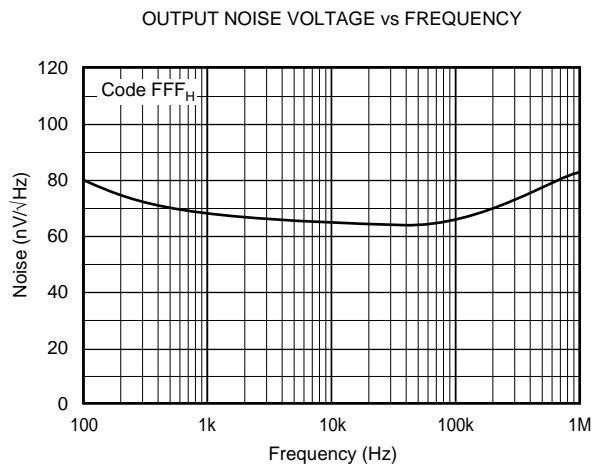
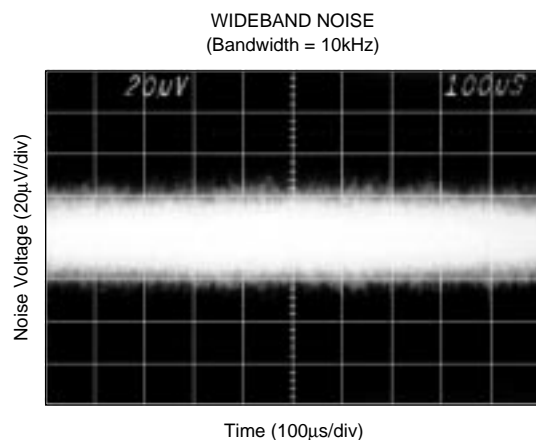
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TYPICAL PERFORMANCE CURVES

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THEORY OF OPERATION

The DAC7617 is a quad, serial input, 12-bit, voltage output DAC. The architecture is a classic R-2R ladder configuration followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network and output op amp, but all share the reference voltage inputs. The minimum voltage output (“zero-scale”) and maximum voltage output (“full-scale”) are set by external voltage references (V_{REFL} and V_{REFH} , respectively). The digital input is a 16-bit serial word that contains the 12-bit DAC code and a 2-bit address code that selects one of the four DACs (the two remaining bits are unused). The converter can be powered from a single +3V supply. Each device offers a reset function which immediately sets all DAC output voltages and internal registers to either zero-scale (code 000_H) or mid-scale (code 800_H). The reset code is selected by the state of the RESETSEL pin (LOW = 000_H, HIGH = 800_H). See Figure 1 for the basic operation of the DAC7617.

ANALOG OUTPUTS

The output of the DAC7617 can swing to ground. Note that the settling time of the output op amp will be longer with voltages very near ground. Additionally, care must be taken when measuring the zero-scale error. If the output amplifier has a negative offset, the output voltage may not change for the first few digital input codes (000_H, 001_H, 002_H, etc.) since the output voltage cannot swing below ground.

The behavior of the output amplifier can be critical in some applications. Under short-circuit conditions (DAC output shorted to V_{DD}), the output amplifier can sink a great deal more current than it can source. See the Specifications Table for more details concerning short-circuit current.

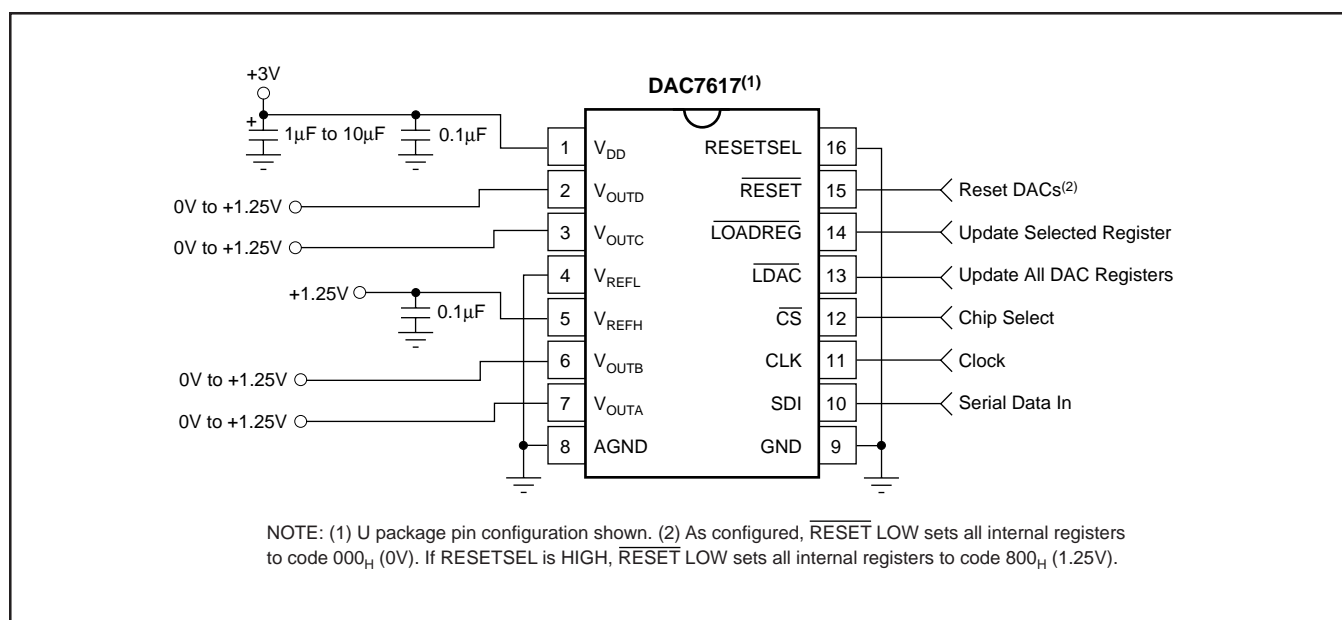


FIGURE 1. Basic Single-Supply Operation of the DAC7617.

REFERENCE INPUTS

The minimum output of each DAC is equal to V_{REFL} plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to $V_{REFH} - 1\text{LSB}$ plus a similar offset voltage.

The current into the reference inputs depends on the DAC output voltages and can vary from a few microamps to approximately 0.4 milliamp. Bypassing the reference voltage or voltages with a $0.1\mu\text{F}$ capacitor placed as close as possible to the DAC7617 package is strongly recommended.

DIGITAL INTERFACE

Figure 2 and Table I provide the basic timing for the DAC7617. The interface consists of a serial clock (CLK), serial data (SDI), a load register signal ($\overline{\text{LOADREG}}$), and a “load all DAC registers” signal ($\overline{\text{LDAC}}$). In addition, a chip select ($\overline{\text{CS}}$) input is available to enable serial communication when there are multiple serial devices. An asynchronous reset input ($\overline{\text{RESET}}$) is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state.

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|------------|---|-----|-----|-----|---------------|
| t_{DS} | Data Valid to CLK Rising | 25 | | | ns |
| t_{DH} | Data Held Valid after CLK Rises | 20 | | | ns |
| t_{CH} | CLK HIGH | 30 | | | ns |
| t_{CL} | CLK LOW | 50 | | | ns |
| t_{CSS} | $\overline{\text{CS}}$ LOW to CLK Rising | 55 | | | ns |
| t_{CSH} | CLK HIGH to $\overline{\text{CS}}$ Rising | 15 | | | ns |
| t_{LD1} | $\overline{\text{LOADREG}}$ HIGH to CLK Rising | 40 | | | ns |
| t_{LD2} | CLK Rising to $\overline{\text{LOADREG}}$ LOW | 15 | | | ns |
| t_{LDRW} | $\overline{\text{LOADREG}}$ LOW Time | 45 | | | ns |
| t_{LDDW} | $\overline{\text{LDAC}}$ LOW Time | 45 | | | ns |
| t_{RSSH} | $\overline{\text{RESETSEL}}$ Valid to $\overline{\text{RESET}}$ LOW | 25 | | | ns |
| t_{RSTW} | $\overline{\text{RESET}}$ LOW Time | 70 | | | ns |
| t_S | Settling Time | 10 | | | μs |

TABLE I. Timing Specifications ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$).

The DAC code and address are provided via a 16-bit serial interface, as shown in Figure 2. The first two bits select the input register that will be updated when $\overline{\text{LOADREG}}$ goes LOW (see Table II). The next two bits are not used. The last 12 bits are the DAC code which is provided, most significant bit first.

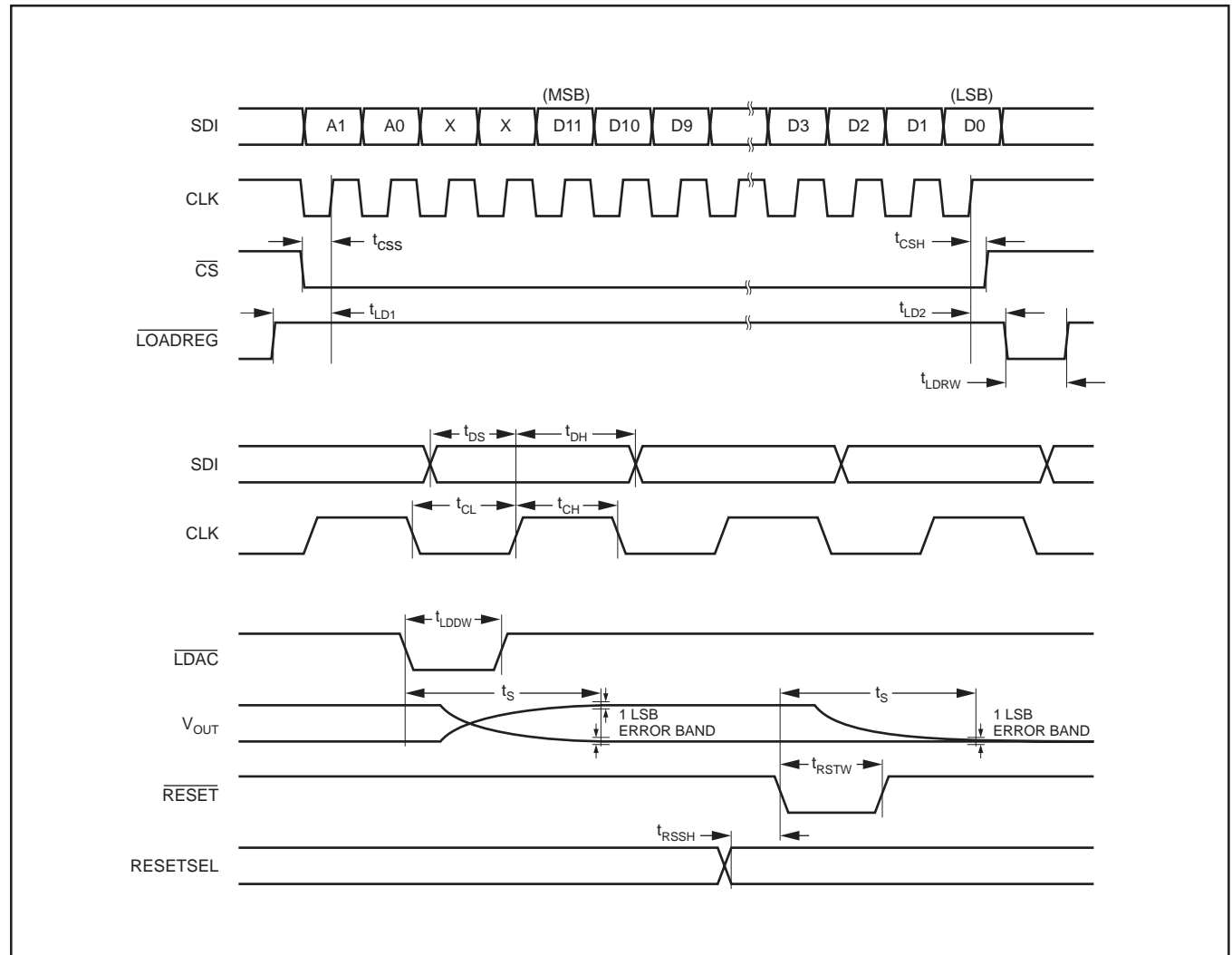


FIGURE 2. DAC7617 Timing.

| A1 | A0 | LOADREG | LDAC | RESET | SELECTED INPUT REGISTER | STATE OF SELECTED INPUT REGISTER | STATE OF ALL DAC REGISTERS |
|------------------|----|---------|------------------|-------|-------------------------|----------------------------------|----------------------------|
| L ⁽¹⁾ | L | L | H ⁽²⁾ | H | A | Transparent | Latched |
| L | H | L | H | H | B | Transparent | Latched |
| H | L | L | H | H | C | Transparent | Latched |
| H | H | L | H | H | D | Transparent | Latched |
| X ⁽³⁾ | X | H | L | H | NONE | (All Latched) | Transparent |
| X | X | H | H | H | NONE | (All Latched) | Latched |
| X | X | X | X | L | ALL | Reset ⁽⁴⁾ | Reset ⁽⁴⁾ |

NOTES: (1) L = Logic LOW. (2) H = Logic HIGH. (3) X = Don't Care. (4) Resets to either 000H or 800_H, per the RESETSEL state (LOW = 000_H, HIGH = 800_H). When RESET rises, all registers that are in their latched state retain the reset value.

TABLE II. Control Logic Truth Table.

| CS ⁽¹⁾ | CLK ⁽¹⁾ | LOADREG | RESET | SERIAL SHIFT REGISTER |
|-------------------|--------------------|------------------|------------------|-----------------------|
| H ⁽²⁾ | X ⁽³⁾ | H | H | No Change |
| L ⁽⁴⁾ | L | H | H | No Change |
| L | ↑ ⁽⁵⁾ | H | H | Advanced One Bit |
| ↑ | L | H | H | Advanced One Bit |
| H ⁽⁶⁾ | X | L ⁽⁷⁾ | H | No Change |
| H ⁽⁶⁾ | X | H | L ⁽⁸⁾ | No Change |

NOTES: (1) CS and CLK are interchangeable. (2) H = Logic HIGH. (3) X = Don't Care. (4) L = Logic LOW (5) = Positive Logic Transition. (6) A HIGH value is suggested in order to avoid a "false clock" from advancing the shift register and changing the shift register. (7) If data is clocked into the serial register while LOADREG is LOW, the selected input register will change as the shift register bits "flow" through A1 and A0. This will corrupt the data in each input register that has been erroneously selected. (8) RESET LOW causes no change in the contents of the serial shift register.

TABLE III. Serial Shift Register Truth Table.

Note that CS and CLK are combined with an OR gate and the output controls the serial-to-parallel shift register internal to the DAC7617 (see the block diagram on the front of this data sheet). These two inputs are completely interchangeable. In addition, care must be taken with the state of CLK when CS rises at the end of a serial transfer. If CLK is LOW when CS rises, the OR gate will provide a rising edge to the shift register, shifting the internal data one additional bit. The result will be incorrect data and possible selection of the wrong input register.

If both CS and CLK are used, then CS should rise only when CLK is HIGH. If not, then either CS or CLK can be used to operate the shift register. See Table III for more information.

The digital data into the DAC7617 is double-buffered. This allows new data to be entered for each DAC without disturbing the analog outputs. When the new settings have been entered into the device, all of the DAC outputs can be updated simultaneously. The transfer from the input registers to the DAC registers is accomplished with a HIGH to LOW transition on the LDAC input. It is possible to keep this pin LOW and update each DAC via LOADREG because the DAC registers become transparent when LDAC is LOW. However, as each new data word is entered into the device, the corresponding output will update immediately when LOADREG is taken LOW.

Digital Input Coding

The DAC7617 input data is in Straight Binary format. The output voltage is given by the following equation:

$$V_{\text{OUT}} = V_{\text{REFL}} + \frac{(V_{\text{REFH}} - V_{\text{REFL}}) \cdot N}{4096}$$

where N is the digital input code (in decimal). This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. As the DAC7617 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to keep digital noise from appearing at the converter output.

Due to the DAC7617's single ground pin, all return currents, including digital and analog return currents, must flow through the GND pin. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power entry point of the system (see Figure 3).

The power applied to V_{DD} should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} should be connected to a +3V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, the 1 μ F to 10 μ F and 0.1 μ F capacitors shown in Figure 3 are strongly recommended. In some situations, additional bypassing may be required, such as a 100 μ F electrolytic capacitor or even a π filter made up of inductors and capacitors—all designed to essentially low-pass filter the +3V supply, removing the high-frequency noise (see Figure 3).

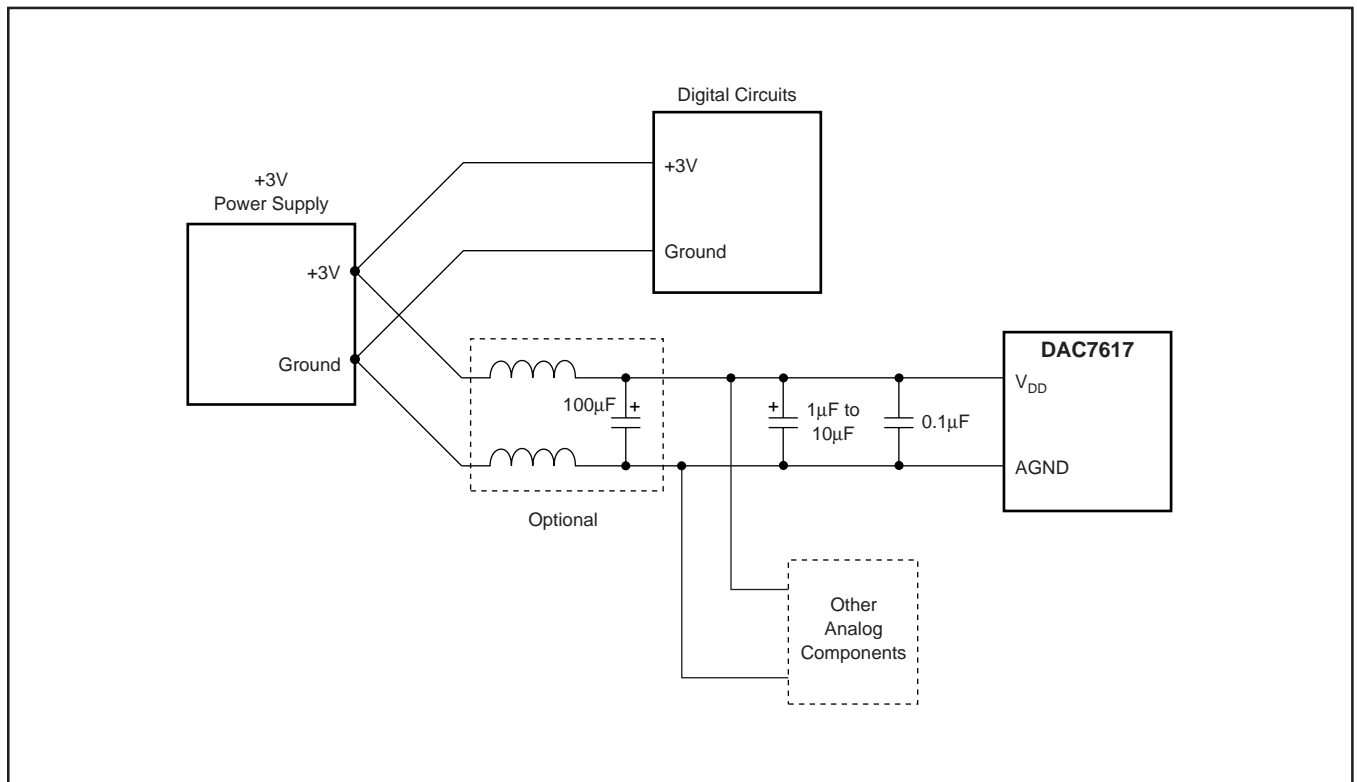


FIGURE 3. Suggested Power and Ground Connections for a DAC7617 Sharing a +3V Supply with a Digital System.

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