

2, 4 and 8-Channel Low Capacitance ESD Protection Array

Features

- 2, 4 and 8 channels of ESD protection
- Provides ESD protection to IEC61000-4-2 Level 4
 - $\pm 8\text{kV}$ contact discharge
 - $\pm 15\text{kV}$ air discharge
- Low loading capacitance of 0.8pF typical
- Minimal capacitance change with temperature and voltage
- Channel I/O to GND capacitance difference of 0.02pF typical is ideal for differential signals
- Channel I/O to I/O capacitance 0.15pF typical
- Zener diode protects supply rail and eliminates the need for external by-pass capacitors
- Each I/O pin can withstand over 1000 ESD strikes
- Available in 4, 6 and 10 bump Chip Scale Packages (CSP)
- *OptiGuard*™ coated for improved reliability at assembly
- Lead-free version available

Applications

- LCD and Camera data lines in wireless handsets that use high-speed serial interfaces.
- I/O port protection for mobile handsets, notebook computers, DSCs, MP3 players, PDAs, etc. including USB, 1394 and Serial ATA
- Wireless handsets
- Handheld PCs/PDAs
- LCD and camera modules

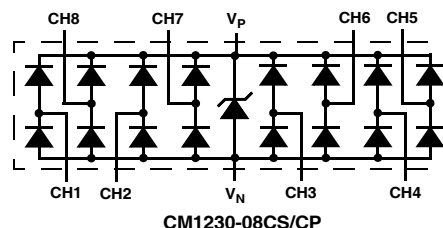
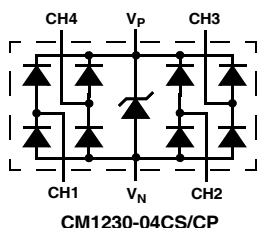
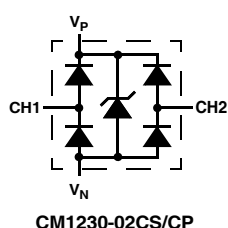
Product Description

The CM1230 is a family of 2, 4 and 8 channel, very low capacitance ESD protection diode arrays in CSP form factor. This device is ideal for protecting systems with high data and clock rates or for circuits that require low capacitive loading. Each channel consists of a pair of ESD diodes that act as clamp diodes that steer positive or negative ESD current pulses to either the positive or negative supply rail. A zener diode is integrated into the array between the positive and negative supply rails. The V_{CC} rail is thus protected from ESD strikes and eliminates the need for a bypass capacitor to absorb positive ESD strikes to ground. Each channel of the CM1230 can safely dissipate ESD strikes of $\pm 8\text{kV}$, meeting the Level 4 requirement of the IEC61000-4-2 international standard for contact discharges as well as $\pm 15\text{kV}$ air discharges per the IEC61000-4-2 specification. Using the MIL-STD-883 (Method 3015) specification for Human Body Model (HBM) ESD, the pins are protected for contact discharges at greater than $\pm 15\text{kV}$.

This device is particularly well-suited for next generation wireless handsets that implement high-speed serial interface solutions for the LCD display and camera interfaces. In these wireless handset designs, a tolerance above 1.5pF cannot be tolerated due to the high data rates that are transferred between the base-band chipset and the LCD driver/controller ICs because a higher capacitive loading will cause the rise and fall times to slow which in turn hampers the functionality of circuit and operation of the wireless handset.

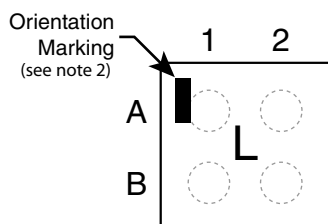
The CM1230 incorporates *OptiGuard*™ which results in improved reliability at assembly. The CM1230 is available in a space-saving, low profile Chip Scale Package with optional lead-free finishing.

Electrical Schematic



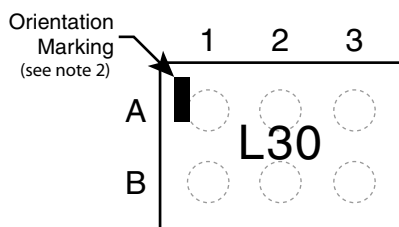
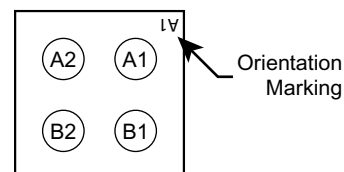
PACKAGE / PINOUT DIAGRAMS

TOP VIEW
(Bumps Down View)

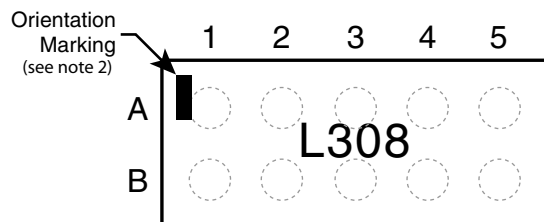
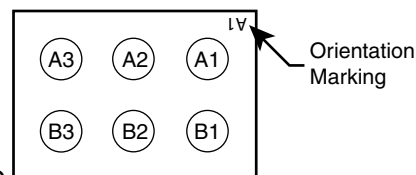


CM1230-02
4-Bump CSP Package

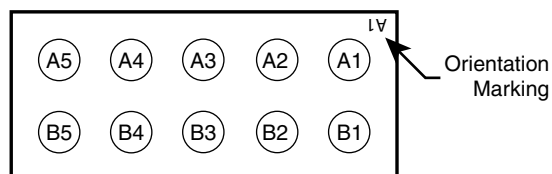
BOTTOM VIEW
(Bumps Up View)



CM1230-04
6-Bump CSP Package



CM1230-08
10-Bump CSP Package



Notes:

- 1) These drawings are not to scale.
- 2) Lead-free devices are specified by using a "+" character for the top side orientation mark.

Ordering Information

PART NUMBERING INFORMATION

# of Channels	Bumps	Package	Standard Finish		Lead-free Finish ²	
			Ordering Part Number ¹	Part Marking	Ordering Part Number ¹	Part Marking
2	4	CSP-4	CM1230-02CS	L	CM1230-02CP	L
4	6	CSP-6	CM1230-04CS	L30	CM1230-04CP	L30
8	10	CSP-10	CM1230-08CS	L308	CM1230-08CP	L308

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Note 2: Lead-free devices are specified by using a "+" character for the top side orientation mark.

Pin Descriptions

PIN DESCRIPTIONS			
2-CHANNEL, 4-BUMP CSP			
PIN	NAME	TYPE	DESCRIPTION
A1	V _N	GND	Negative voltage supply rail
B1	CH2	I/O	ESD Channel
A2	CH1	I/O	ESD Channel
B2	V _P	PWR	Positive voltage supply rail
4-CHANNEL, 6-BUMP CSP			
PIN	NAME	TYPE	DESCRIPTION
A1	CH1	I/O	ESD Channel
B1	CH2	I/O	ESD Channel
A2	V _P	PWR	Positive voltage supply rail
B2	V _N	GND	Negative voltage supply rail
A3	CH3	I/O	ESD Channel
B3	CH4	I/O	ESD Channel

PIN DESCRIPTIONS (CONT'D)			
8-CHANNEL, 10-BUMP CSP			
PIN	NAME	TYPE	DESCRIPTION
A1	CH1	I/O	ESD Channel
B1	CH2	I/O	ESD Channel
A2	CH3	I/O	ESD Channel
B2	CH4	I/O	ESD Channel
A3	V _P	PWR	Positive voltage supply rail
B3	V _N	GND	Negative voltage supply rail
A4	CH5	I/O	ESD Channel
B4	CH6	I/O	ESD Channel
A5	CH7	I/O	ESD Channel
B5	CH8	I/O	ESD Channel

Specifications

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNITS
Operating Supply Voltage ($V_P - V_N$)	6.0	V
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any channel input	($V_N - 0.5$) to ($V_P + 0.5$)	V

STANDARD OPERATING CONDITIONS

PARAMETER	RATING	UNITS
Operating Temperature Range	-40 to +85	°C

ELECTRICAL OPERATING CHARACTERISTICS^(SEE NOTE 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_P	Operating Supply Voltage ($V_P - V_N$)			3.3	5.5	V
I_P	Operating Supply Current	($V_P - V_N$)=3.3V			8.0	μA
V_F	Diode Forward Voltage Top Diode Bottom Diode	$I_F = 8\text{mA}$; $T_A = 25^\circ\text{C}$	0.60 0.60	0.80 0.80	0.95 0.95	V V
I_{LEAK}	Channel Leakage Current	$T_A = 25^\circ\text{C}$; $V_P = 5\text{V}$, $V_N = 0\text{V}$, $V_{IN} = 0\text{V}$ to 5V		±0.1	±1.0	μA
C_{IN}	Channel Input Capacitance	At 1 MHz, $V_P = 3.3\text{V}$, $V_N = 0\text{V}$, $V_{IN} = 1.65\text{V}$; Note 2 applies		0.8	1.20	pF
ΔC_{IN}	Channel Input Capacitance Matching	At 1 MHz, $V_P = 3.3\text{V}$, $V_N = 0\text{V}$, $V_{IN} = 1.65\text{V}$; Note 2 applies		0.02		pF
C_{MUTUAL}	Mutual Capacitance between signal pin and adjacent signal pin	At 1 MHz, $V_P = 3.3\text{V}$, $V_N = 0\text{V}$, $V_{IN} = 1.65\text{V}$; Note 2 applies		0.15		pF
V_{ESD}	In-system ESD Protection Peak Discharge Voltage at any channel input, in system a) Contact discharge per IEC 61000-4-2 standard b) Human Body Model, MIL- STD-883, Method 3015	Notes 2, 4 & 5; $T_A = 25^\circ\text{C}$ Notes 2, 3 & 5; $T_A = 25^\circ\text{C}$	±8 ±15			kV kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	$T_A = 25^\circ\text{C}$, $I_{PP} = 1\text{A}$, $t_P = 8/20\mu\text{S}$; Notes 2, & 5		+9.8 -1.8		V V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	$I_{PP} = 1\text{A}$, $t_P = 8/20\mu\text{S}$ Any I/O pin to Ground; Note 2 and 5		0.76 0.56		Ω Ω

Note 1: All parameters specified at $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise noted.

Note 2: These parameters guaranteed by design and characterization.

Note 3: Human Body Model per MIL-STD-883, Method 3015, $C_{Discharge} = 100\text{pF}$, $R_{Discharge} = 1.5\text{K}\Omega$, $V_P = 3.3\text{V}$, V_N grounded.

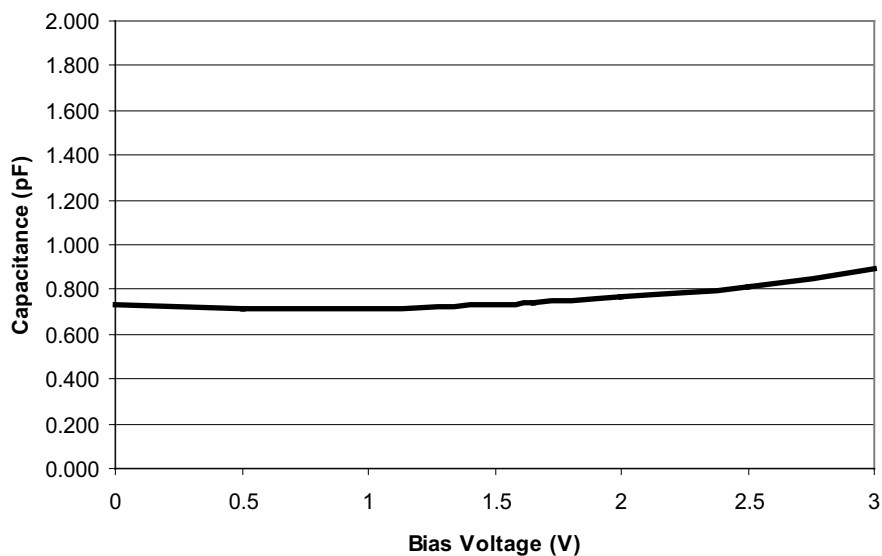
Note 4: Standard IEC 61000-4-2 with $C_{Discharge} = 150\text{pF}$, $R_{Discharge} = 330\Omega$, $V_P = 3.3\text{V}$, V_N grounded.

Note 5: These measurements performed with no external capacitor on V_P .

Note 6: Measured under pulsed conditions, pulse width = 0.7ms, maximum current = 1.5A.

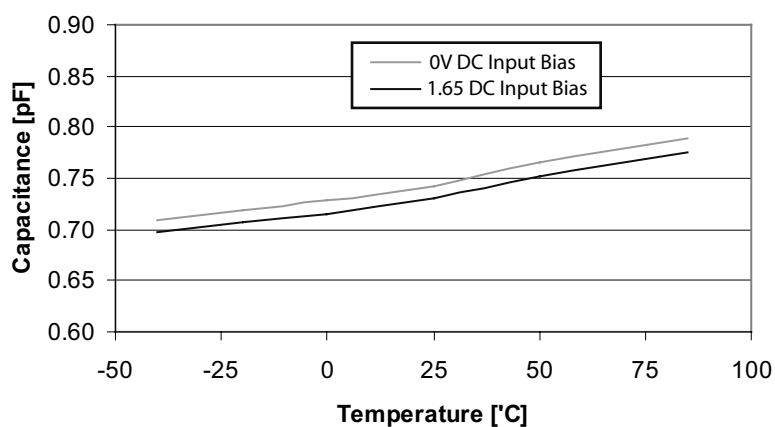
Performance Information

Input Channel Capacitance Performance Curves



Typical Variation of C_{IN} vs. V_{IN}

($f=1\text{MHz}$, $V_P = 3.3\text{V}$, $V_N = 0\text{V}$, $0.1\text{ }\mu\text{F}$ chip capacitor between V_P and V_N , $T_A = 25^\circ\text{C}$)

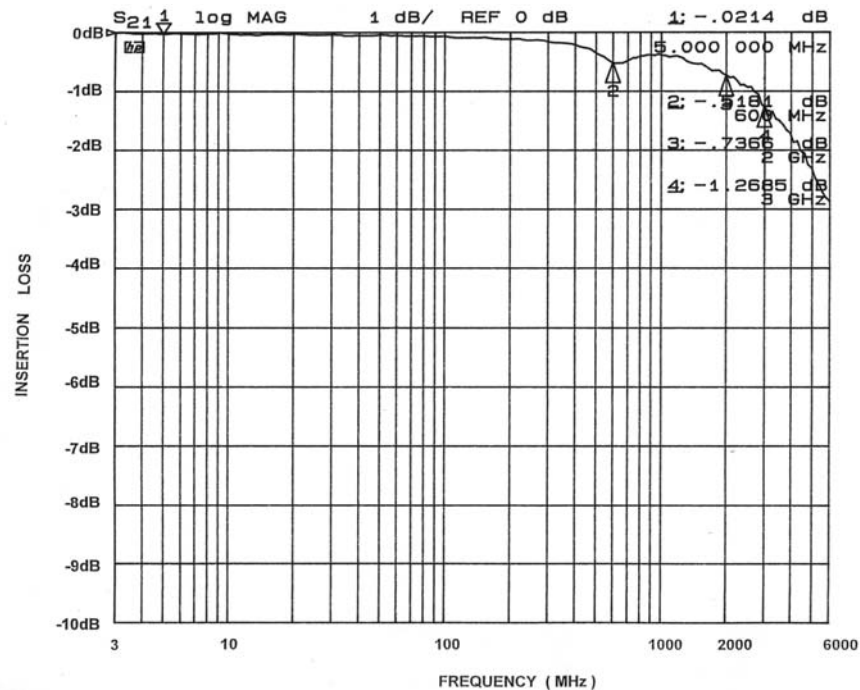


Typical Variation of C_{IN} vs. Temp

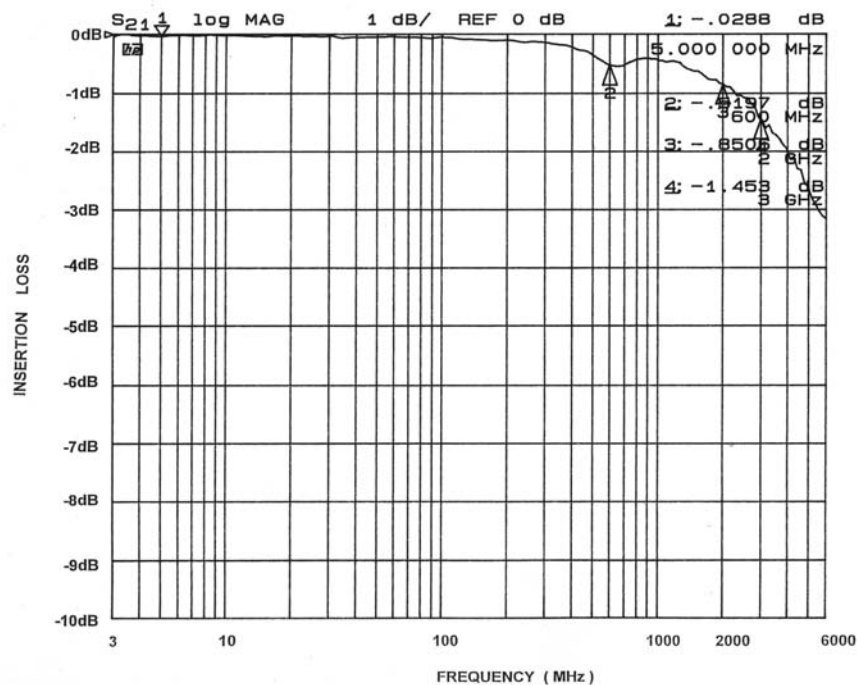
($f=1\text{MHz}$, $V_{IN}=30\text{mV}$, $V_P = 3.3\text{V}$, $V_N = 0\text{V}$, $0.1\text{ }\mu\text{F}$ chip capacitor between V_P and V_N)

Performance Information (Cont'd)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment)



Insertion Loss VS. Frequency (0V DC Bias, $V_p=3.3V$)



Insertion Loss VS. Frequency (2.5V DC Bias, $V_p=3.3V$)

Application Information

Refer to Application Note AP-217, "The Chip Scale Package", for a detailed description of Chip Scale Packages offered by California Micro Devices.

PRINTED CIRCUIT BOARD RECOMMENDATIONS

PARAMETER	VALUE
Pad Size on PCB	0.275mm
Pad Shape	Round
Pad Definition	Non-Solder Mask defined pads
Solder Mask Opening	0.325mm Round
Solder Stencil Thickness	0.125mm - 0.150mm
Solder Stencil Aperture Opening (laser cut, 5% tapered walls)	0.330mm Round
Solder Flux Ratio	50/50 by volume
Solder Paste Type	No Clean
Pad Protective Finish	OSP (Entek Cu Plus 106A)
Tolerance — Edge To Corner Ball	±50µm
Solder Ball Side Coplanarity	±20µm
Maximum Dwell Time Above Liquidous (183°C)	60 seconds
Maximum Soldering Temperature for a Eutectic Device using Eutectic Solder Paste	240°C
Maximum Soldering Temperature for a Lead-free Device using Lead-free Solder Paste	260°C

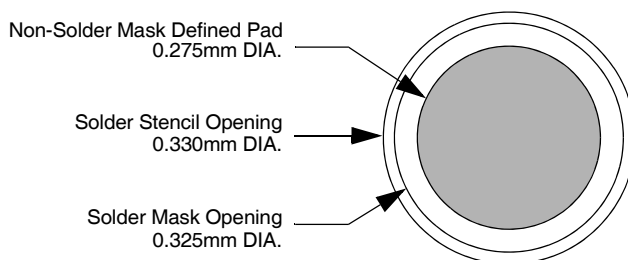


Figure 1. Recommended Non-Solder Mask Defined Pad Illustration

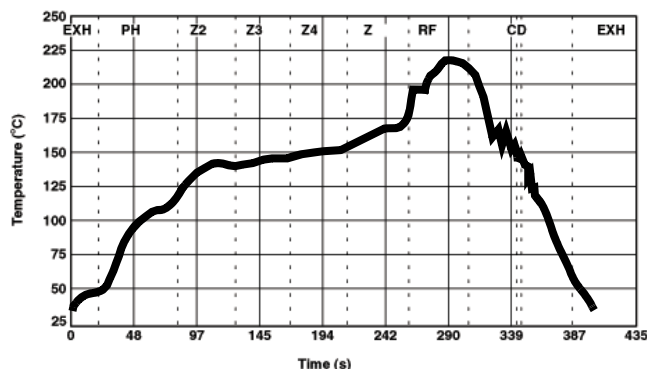


Figure 2. Eutectic (SnPb) Solder Ball Reflow Profile

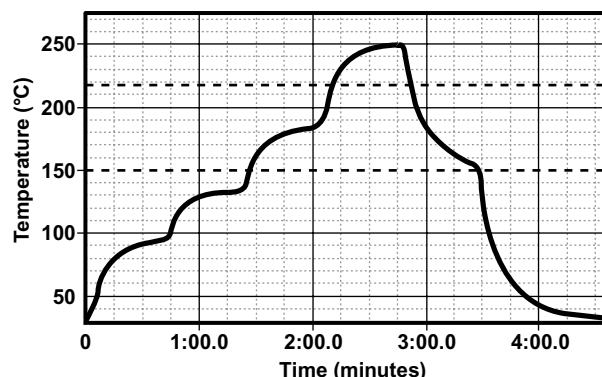


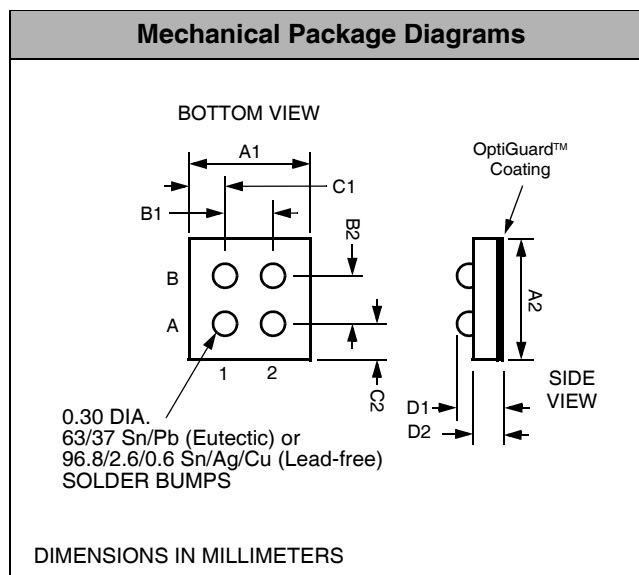
Figure 3. Lead-free (SnAgCu) Solder Ball Reflow Profile

Mechanical Details

CSP-4 Mechanical Specifications

The CM1230-02CS/CP is supplied in a 4 bump Chip Scale Package (CSP). Dimensions are shown below. For complete information on the CSP, see the California Micro Devices CSP Package Information document.

PACKAGE DIMENSIONS						
Package		Custom CSP				
Bumps		4				
Dim	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A1	0.915	0.960	1.005	0.0360	0.0378	0.0396
A2	0.915	0.960	1.005	0.0360	0.0378	0.0396
B1	0.495	0.500	0.505	0.0195	0.0197	0.0199
B2	0.495	0.500	0.505	0.0195	0.0197	0.0199
C1	0.180	0.230	0.280	0.0071	0.0091	0.0110
C2	0.180	0.230	0.280	0.0071	0.0091	0.0110
D1	0.575	0.644	0.714	0.0226	0.0254	0.0281
D2	0.368	0.419	0.470	0.0145	0.0165	0.0185
# per tape and reel		3500 pieces				
Controlling dimension: millimeters						



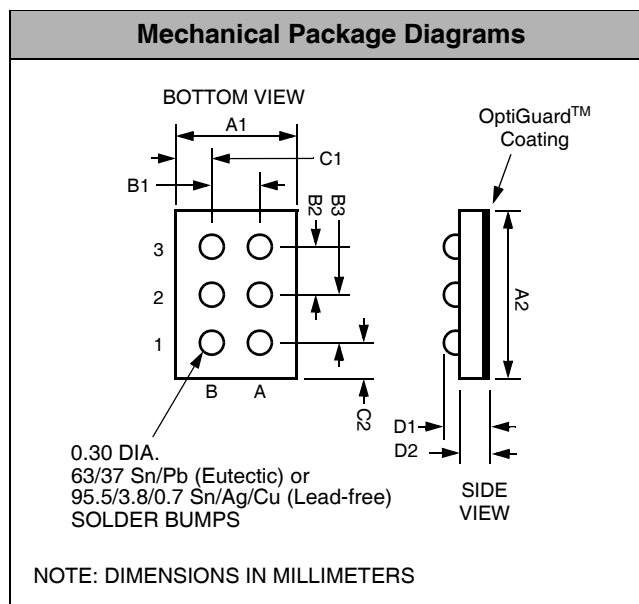
**Package Dimensions for
CM1230-02 Chip Scale Package**

Mechanical Details (cont'd)

CSP-6 Mechanical Specifications

The CM1230-04CS/CP is supplied in a 6 bump Chip Scale Package (CSP). Dimensions are shown below. For complete information on the CSP, see the California Micro Devices CSP Package Information document.

PACKAGE DIMENSIONS						
Package		Custom CSP				
Bumps		6				
Dim	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A1	0.915	0.960	1.005	0.0360	0.0378	0.0396
A2	1.415	1.460	1.505	0.0557	0.0575	0.0593
B1	0.495	0.500	0.505	0.0195	0.0197	0.0199
B2	0.495	0.500	0.505	0.0195	0.0197	0.0199
C1	0.180	0.230	0.280	0.0071	0.0091	0.0110
C2	0.180	0.230	0.280	0.0071	0.0091	0.0110
D1	0.575	0.644	0.714	0.0226	0.0254	0.0281
D2	0.368	0.419	0.470	0.0145	0.0165	0.0185
# per tape and reel		3500 pieces				
Controlling dimension: millimeters						



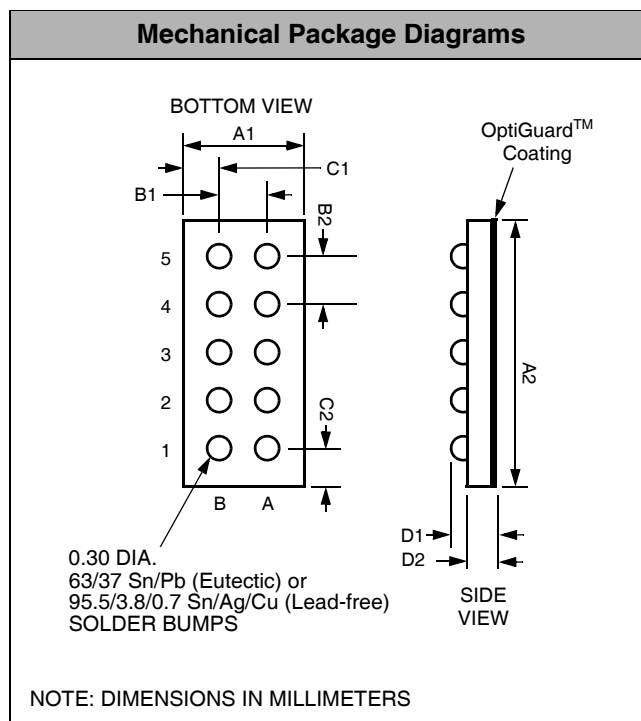
**Package Dimensions for
CM1230-04 Chip Scale Package**

Mechanical Details (cont'd)

CSP-10 Mechanical Specifications

The CM1230-08CS/CP is supplied in a 10 bump Chip Scale Package (CSP). Dimensions are shown below. For complete information on the CSP, see the California Micro Devices CSP Package Information document.

PACKAGE DIMENSIONS						
Package		Custom CSP				
Bumps		10				
Dim	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A1	0.915	0.960	1.005	0.0360	0.0378	0.0396
A2	2.415	2.460	2.505	0.0951	0.0969	0.0986
B1	0.495	0.500	0.505	0.0195	0.0197	0.0199
B2	0.495	0.500	0.505	0.0195	0.0197	0.0199
C1	0.180	0.230	0.280	0.0071	0.0091	0.0110
C2	0.180	0.230	0.280	0.0071	0.0091	0.0110
D1	0.575	0.644	0.714	0.0226	0.0254	0.0281
D2	0.368	0.419	0.470	0.0145	0.0165	0.0185
# per tape and reel		3500 pieces				
Controlling dimension: millimeters						



**Package Dimensions for
CM1230-08 Chip Scale Package**

CSP Tape and Reel Specifications

PART NUMBER	CHIP SIZE (mm)	POCKET SIZE (mm) $B_0 \times A_0 \times K_0$	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	P_0	P_1
CM1230-02	0.96 x 0.96 x 0.644	1.14 x 1.00 x 0.70	8mm	178mm (7")	3500	4mm	4mm
CM1230-04	1.46 x 0.96 x 0.644	1.72 x 1.17 x 0.73	8mm	178mm (7")	3500	4mm	4mm
CM1230-08	2.46 x 0.96 x 0.644	2.62 x 1.12 x 0.76	8mm	178mm (7")	3500	4mm	4mm

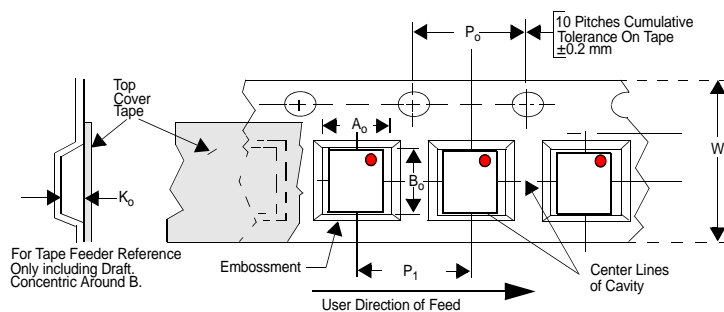


Figure 4. Tape and Reel Mechanical Data