

MICROPOWER RRO Operational Amplifier

Features

- Tiny SOT23-5 Package
- Guaranteed specs at 1.8V, 2.2V, 2.7V, 3V and 5V
- Very Low Supply current typically 150 μ A @3V
- Rail-to-Rail Output
- Typical Total Harmonic Distortion of 0.02% at 3V
- 2.7MHz Typical Gain Bandwidth Product
- 2V/ μ s Typical Slew Rate

Applications

- Mobile Communications
- Cellular Phones
- Portable Equipment
- Notebooks and PDAs

Product Description

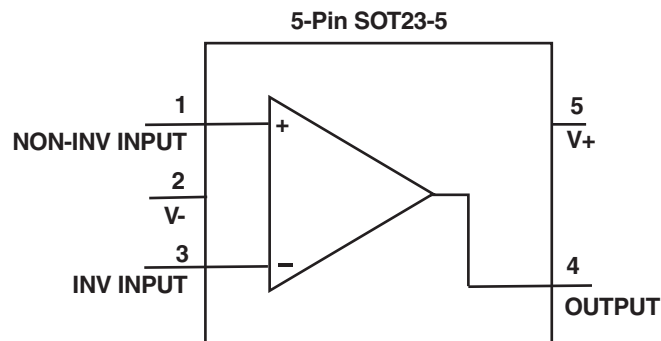
The CMV1030 is a high performance CMOS operational amplifier available in a small SOT23-5 package. Operating with very low supply current, it is ideal for battery operated applications where power, space and weight are critical.

With 2.7MHz Gain Bandwidth Product, 2V/ μ s Slew Rate, and a typical current consumption of only 150 μ A, the

CMV1030 provides excellent power-performance ratio for power sensitive applications.

Ideal for use in personal electronics such as cellular handsets, pagers, cordless telephones and other products with limited space and battery power.

PIN DIAGRAM



STANDARD PART ORDERING INFORMATION

Package		Ordering Part Number	
Pins	Style	Tape & Reel	Part Marking
5	SOT23-5	CMV1030Y/R	1030

ABSOLUTE MAXIMUM RATINGS (NOTE 1)		
Parameter	Rating	Unit
ESD Protection (HBM, Note 2)	2000	V
Differential Input Voltage	+/- Supply Voltage	V
Voltage at input/output Pin	(V+) +0.3, (V-) -0.3	V
Temperature: Storage	-65 to 150	°C
Operating Junction (Note 4)	125	
Lead (Soldering, 10s)	260	
Supply Voltage (V+ to V-)	7.5	V
Current at Input Pin	5	mA
Current at Output Pin (Note 3)	15	mA
Current at Power Supply Pins	15	mA

OPERATING CONDITIONS (unless specified otherwise)		
Parameter	Rating	Unit
Supply Voltage	1.8 to 7	V
Junction Temperature	-40 to 85	°C
Thermal Resistance	325	°C / W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating conditions indicate ratings for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Operating Characteristics.

Note 2: Human Body Model, 1.5K Ω in series with 100pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short ckt operation at elevated ambient temperatures can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly to a PC board.

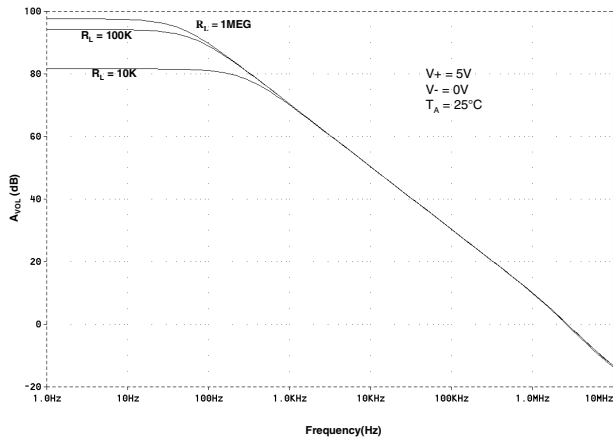
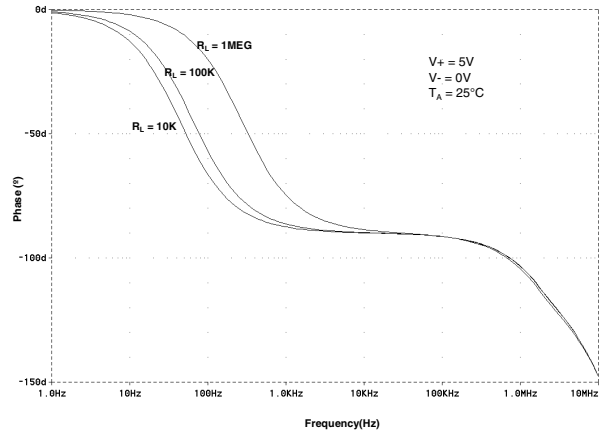
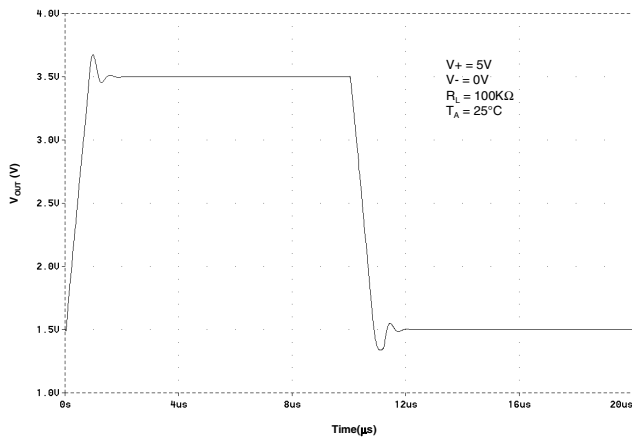
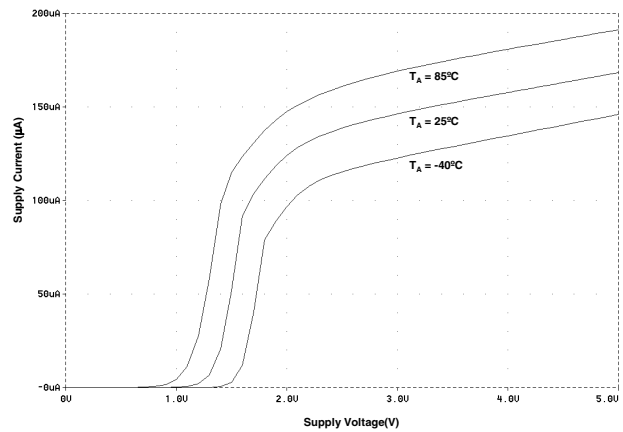
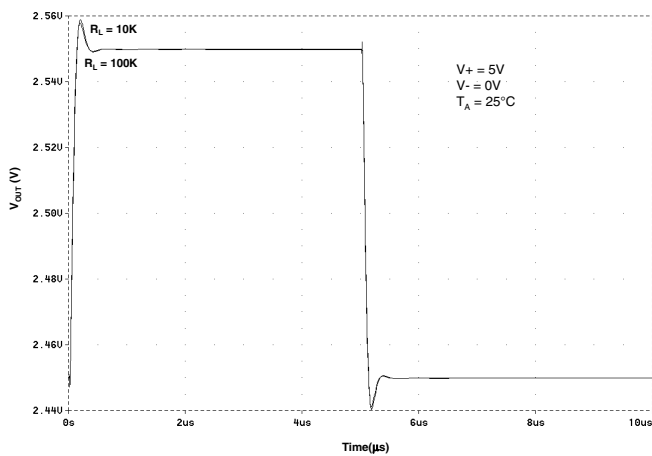
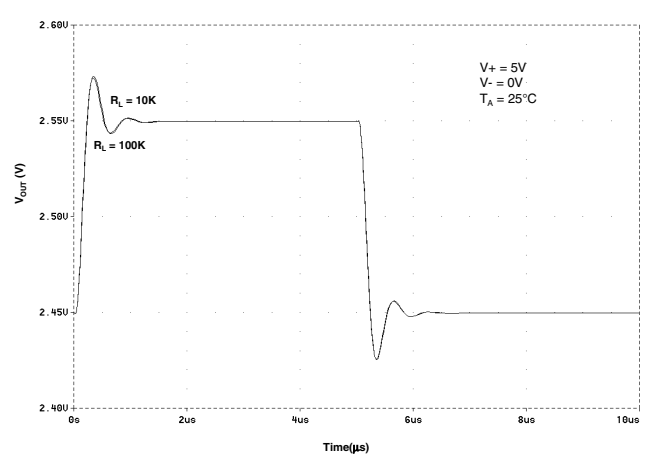
1.8V ELECTRICAL OPERATING CHARACTERISTICS (Unless otherwise specified T _j = 25°C, V ₊ = 1.8V, V ₋ = 0V, R _L > 1MΩ)					
Symbol	Parameter	Conditions	Typ	Limit	Unit
V _{OS}	Input Offset Voltage	V _{OUT} = 0.9V		9	mV
I _B	Input Bias Current		1		pA
I _{OS}	Input Offset Current		0.5		pA
R _{IN}	Input Resistance		1		TΩ
I _S	Supply Current		120	240	μA
GBW	Gain Bandwidth Product		2		MHz
A _V	Large Signal Voltage Gain	V _{OUT} = 0.2V to 1.6V	80	60	dB
SR	Slew Rate	A _V = -1, R _L = 100K	1.4	0.35	V/μs
PSRR	Power Supply Rejection Ratio	V ₊ = 0.9V tp 1.2V V ₋ = -0.9V to -1.2V V _{CM} = 0V	70	50	dB
CMRR	Common Mode Rejection Ratio	0V < V _{CM} < 1.8V	60	40	dB
V _{CM}	Common Mode Input Range		0 1.1		V
THD	Total Harmonic Distortion	A _V = -1, f = 1KHz, V _{OUT} = 1V p-p R _L = 100K	0.026		%
I _{SC}	Output Short Circuit Current	Source/Sink	5		mA
V _O	Output Swing from either rail	R _L = 10K	20	150	mV

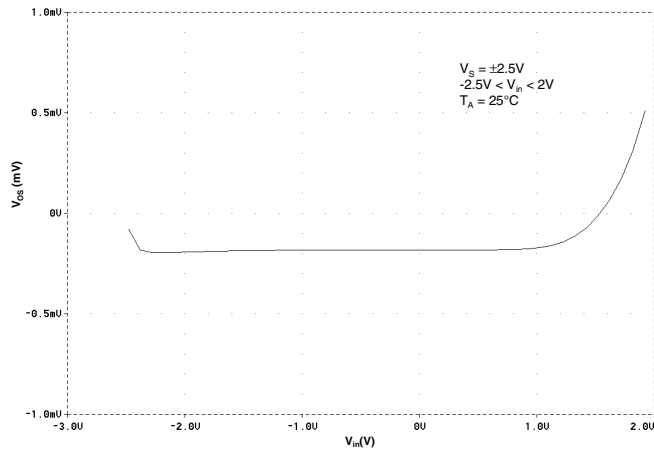
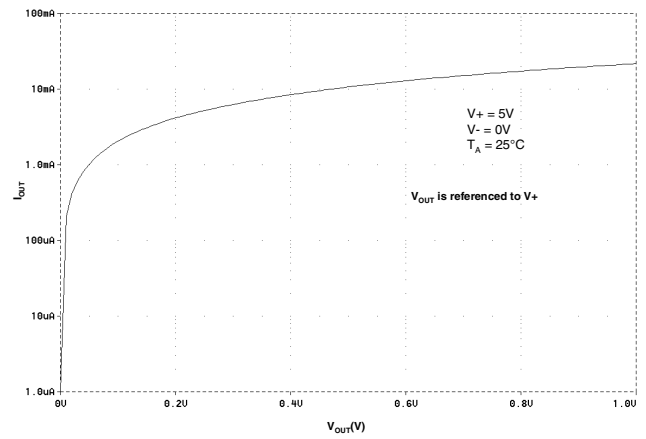
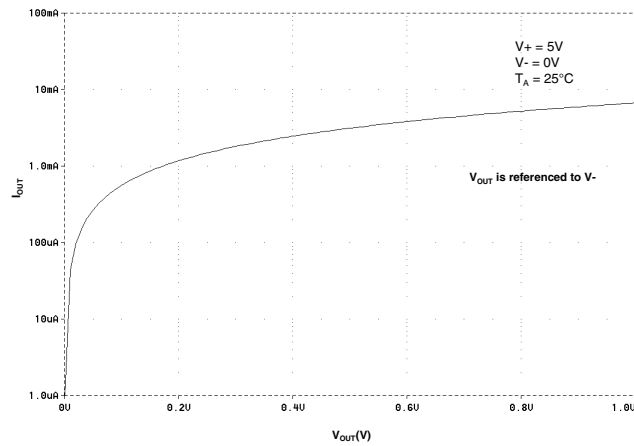
2.2V ELECTRICAL OPERATING CHARACTERISTICS (Unless otherwise specified T _j = 25°C, V ₊ = 2.2V, V ₋ = 0V, R _L > 1MΩ)					
Symbol	Parameter	Conditions	Typ	Limit	Unit
V _{OS}	Input Offset Voltage	V _{OUT} = 1.1V		9	mV
I _B	Input Bias Current		1		pA
I _{OS}	Input Offset Current		0.5		pA
R _{IN}	Input Resistance		1		TΩ
I _S	Supply Current		135	270	μA
GBW	Gain Bandwidth Product		2.4		MHz
A _V	Large Signal Voltage Gain	V _{OUT} = 0.2V to 2V	80	60	dB
SR	Slew Rate	A _V = -1, R _L = 100K	1.8	0.45	V/μs
PSRR	Power Supply Rejection Ratio	V ₊ = 1.1V tp 1.4V V ₋ = -1.1V to -1.4V V _{CM} = 0V	70	50	dB
CMRR	Common Mode Rejection Ratio	0V < V _{CM} < 1.2V	60	40	dB
V _{CM}	Common Mode Input Range		0 1.5		V
THD	Total Harmonic Distortion	A _V = -1, f = 1KHz, V _{OUT} = 1.4Vp-p R _L = 100K	0.02		%
I _{SC}	Output Short Circuit Current	Source/Sink	7		mA
V _O	Output Swing from either rail	R _L = 10K	20	150	mV

2.7V ELECTRICAL OPERATING CHARACTERISTICS (Unless otherwise specified $T_j = 25^\circ\text{C}$, $V_+ = 2.7\text{V}$, $V_- = 0\text{V}$, $R_L > 1\text{M}\Omega$)					
Symbol	Parameter	Conditions	Typ	Limit	Unit
V_{OS}	Input Offset Voltage	$V_{OUT} = 1.35\text{V}$		6	mV
I_B	Input Bias Current		1		pA
I_{OS}	Input Offset Current		0.5		pA
R_{IN}	Input Resistance		1		$\text{T}\Omega$
I_S	Supply Current		150	300	μA
GBW	Gain Bandwidth Product		2.7		MHz
A_V	Large Signal Voltage Gain	$V_{OUT} = 0.2\text{V to } 2.5\text{V}$	85	65	dB
SR	Slew Rate	$A_V = -1$, $R_L = 100\text{K}$	2	0.5	$\text{V}/\mu\text{s}$
PSRR	Power Supply Rejection Ratio	$V_+ = 1.35\text{V to } 1.65\text{V}$ $V_- = -1.35\text{V to } 1.65\text{V}$ $V_{CM} = 0\text{V}$	70	50	dB
CMRR	Common Mode Rejection Ratio	$0\text{V} < V_{CM} < 1.7\text{V}$	60	45	dB
V_{CM}	Common Mode Input Range		0 2		V
THD	Total Harmonic Distortion	$A_V = -1$, $f = 1\text{KHz}$, $V_{OUT} = 1.9\text{Vp-p}$ $R_L = 100\text{K}$	0.02		%
I_{SC}	Output Short Circuit Current	Source/Sink	12		mA
V_O	Output Swing from either rail	$R_L = 10\text{K}$	20	150	mV

3V ELECTRICAL OPERATING CHARACTERISTICS (Unless otherwise specified $T_j = 25^\circ\text{C}$, $V_+ = 3\text{V}$, $V_- = 0\text{V}$, $R_L > 1\text{M}\Omega$)					
Symbol	Parameter	Conditions	Typ	Limit	Unit
V_{OS}	Input Offset Voltage	$V_{OUT} = 1.5\text{V}$		5	mV
I_B	Input Bias Current		1		pA
I_{OS}	Input Offset Current		0.5		pA
R_{IN}	Input Resistance		1		$\text{T}\Omega$
I_S	Supply Current		150	300	μA
GBW	Gain Bandwidth Product		2.7		MHz
A_V	Large Signal Voltage Gain	$V_{OUT} = 0.2\text{V to } 2.8\text{V}$	85	65	dB
SR	Slew Rate	$A_V = -1$, $R_L = 100\text{K}$	2	0.5	$\text{V}/\mu\text{s}$
PSRR	Power Supply Rejection Ratio	$V_+ = 1.5\text{V to } 1.8\text{V}$ $V_- = -1.5\text{V to } -1.8\text{V}$ $V_{CM} = 0\text{V}$	80	55	dB
CMRR	Common Mode Rejection Ratio	$0\text{V} < V_{CM} < 2\text{V}$	70	50	dB
V_{CM}	Common Mode Input Range		0 2.3		V
THD	Total Harmonic Distortion	$A_V = -1$, $f = 1\text{KHz}$, $V_{OUT} = 2\text{Vp-p}$ $R_L = 100\text{K}$	0.02		%
I_{SC}	Output Short Circuit Current	Source/Sink	15		mA
V_O	Output Swing from either rail	$R_L = 10\text{K}$	20	150	mV

5V ELECTRICAL OPERATING CHARACTERISTICS (Unless otherwise specified T_j = 25°C, V₊ = 5V, V₋ = 0V, R_L > 1MΩ)					
Symbol	Parameter	Conditions	Typ	Limit	Unit
V _{OS}	Input Offset Voltage	V _{OUT} = 1.5V		5	mV
I _B	Input Bias Current		1		pA
I _{OS}	Input Offset Current		0.5		pA
R _{IN}	Input Resistance		1		TΩ
I _S	Supply Current		100	200	μA
GBW	Gain Bandwidth Product		2.9		MHz
A _V	Large Signal Voltage Gain	V _{OUT} = 0.2V to 4.8V	90	70	dB
SR	Slew Rate	A _V = -1, R _L = 100K	2.3	0.575	V/μs
PSRR	Power Supply Rejection Ratio	V ₊ = 2.5V to 2.8V V ₋ = -2.5V to -2.8V V _{CM} = 0V	80	55	dB
CMRR	Common Mode Rejection Ratio	0V < V _{CM} < 4V	70	50	dB
V _{CM}	Common Mode Input Range		0 4.3		V
THD	Total Harmonic Distortion	A _V = -1, f = 1KHz, V _{OUT} = 4Vp-p R _L = 100K	0.02		%
I _{SC}	Output Short Circuit Current	Source/Sink	25		mA
V _O	Output Swing from either rail	R _L = 10K	20	150	mV

Open Loop Voltage Gain Response

Open Loop Phase Response

Large Signal Pulse Response

Supply Current Versus Supply Voltage

Non Inverting Small Signal Response

Inverting Small Signal Response


Common Mode Rejection Ratio

Current Sourcing Versus V_{OUT}

Current Sinking Versus V_{OUT}


Applications Information

1. Input Common Mode Range and Output Voltage Considerations

The CMV1030 is capable of accommodating an input common mode voltage equal to one volt below the positive rail and all the way to the negative rail. It is also capable of output voltages equal to both power supply rails. Voltages that exceed the supply voltages will not cause phase inversion of the output, however, ESD diode clamps are provided at the inputs that can be damaged if static currents in excess of $\pm 5\text{mA}$ are allowed to flow in them. This can occur when the magnitude of input voltage exceeds the rail by more than 0.3 volt. To preclude damage, an applications resistor, R_s , in series with the input is recommended as illustrated in Figure 1 whose value for R_s is given by:

$$R_s > \frac{V_{IN} - (V+ + 0.3 \text{ V})}{5\text{mA}}$$

For $V+$ (or $V-$) equal to 2.2 volts and V_{IN} equal to 10 volts, R_s should be chosen for a value of $2.5\text{K}\Omega$ or greater.

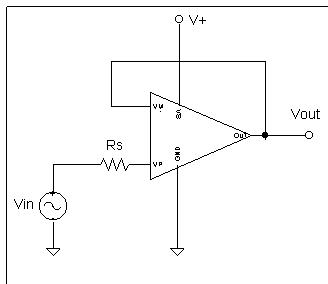


Figure 1.

2. Output Current and Power Dissipation Considerations

The CMV1030 is capable of sinking and sourcing output currents in excess of 7mA at voltages very nearly equal to the rails. As such, it does not have any internal short circuit protection (which would in any event detract from its rail to rail capability). Although the power dissipation and junction temperature rise are small, a short analysis is worth investigating.

Obviously, the worst case from a power dissipation point of view is when the output is shorted to either ground in a single rail application or to the opposite supply voltage in split rail applications. Since device only draws $60\mu\text{A}$ supply current ($100\mu\text{A}$ maximum), its contribution to the junction temperature, T_J , is negligible. As an example, let us analyze a situation in which the CMV1030 is operated from a 5 volt supply and ground, the output is "programmed" to positive saturation, and the output pin

is indefinitely shorted to ground. In general:

$$P_{DISS} = (V+ - V_{OUT}) * I_{OUT} + I_S * V+$$

Where: P_{DISS} = Power dissipated by the chip

$V+$ = Supply voltage

V_{OUT} = The output voltage

I_S = Supply Current

The contribution to power dissipation due to supply current is $200\mu\text{W}$ and is indeed negligible as stated above.

The primary contribution to power dissipation occurs in the output stage. $V+ - V_{OUT}$ would equal $5\text{V} - 0\text{V} = 5\text{V}$, and power dissipation would be equal to 35mW .

$$T_J = T_A + \theta_{JA} * P_{DISS}$$

Where: T_A = The ambient temperature

θ_{JA} = The thermal impedance of the package junction to ambient

The SOT23 exhibits a θ_{JA} equal to 325°C/W . Thus for our example the junction rise would be about 11.4 which is clearly not a destructive situation even under an ambient temperature of 85°C .

3. Input Impedance Considerations

The CMV1030 exhibits an input impedance typically in excess of $1\text{ Tera } \Omega$ (1×10^{12} ohms) making it very appropriate for applications involving high source impedance such as photodiodes and high output impedance transducers or long time constant integrators. High source impedances usually dictate large feedback resistors. But, the output capacitance of the source in parallel with the input capacitance of the CMV1030 (which is typically 3pF) create a parasitic pole with the feedback resistor which erodes the phase margin of the amplifier. The usual fix is to bypass, R_F , as shown in Figure 2 with a small capacitor to cancel the input pole. The usual formula for calculating C_F always results in a value larger than that is required:

$$\frac{1}{2\pi R_s C_s} \geq \frac{1}{2\pi R_F C_F}$$

Since the parasitic capacitance can change between the breadboard and the production printed circuit board, we favor the use of a "gimmick", a technique perfected by TV technicians in the 1950's. A gimmick is made by taking two lengths (typically about a foot) of small gauge wire such as AWG 24, twisting them together, and then after baring all ends soldering the gimmick across R_F . With the circuit operating, C_F is "adjusted" by clipping short lengths of the gimmick off until the compensation is nominal. Then simply remove the gimmick, take it to an impedance bridge, and select the capacitor accord-

ingly.

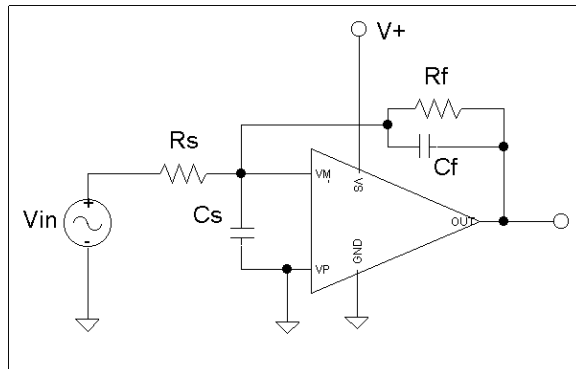


Figure 2.

4. Capacitive Load Considerations

The CMV1030 is capable of driving capacitive loads in excess of 100pF without oscillation. However, significant peaking will result. Probably the easiest way minimize this problem is to use an isolation resistor as shown in Figure 3.

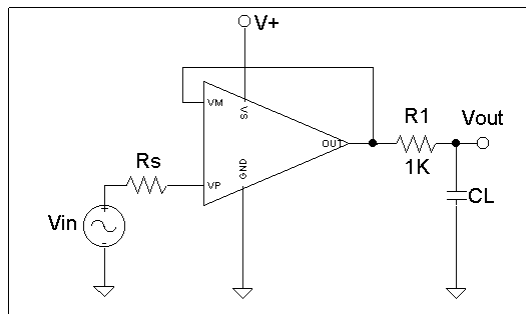


Figure 3

5. Power Supply Decoupling

The CMV1030 is not prone to oscillation without the use of power supply decoupling capacitors, however to minimize hum and noise pick-up, it is recommended that the rails be bypassed with 0.01μF capacitors.

6. Typical Applications

Operational amplifiers have been used for years to generate frequency stable oscillators, but the circuit

shown in Figure 4 provides a stable frequency operating from a single supply voltage and drawing a mere 40μA. For $(R_1 + R_2) \div R_1 = 0.473$, the period, T, of the oscillator is given by:

$$T = 2 R_F C_1$$

Where: R_F is the feedback resistor
 C_1 is the capacitor

The period is easily adjusted by varying R_F . R_3 ensures that the circuit will start on a single rail by forcing A_1 's output to the positive rail. R_4 's value is not critical but should be a factor of 10 greater than the parallel combination of R_1 and R_2 . The circuit lends itself to a variety of applications such as battery operated toys where a stable frequency is required and low supply current is a must to maintain battery life.

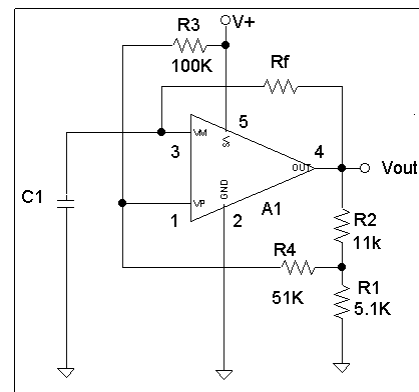


Figure 4

Personal Computers including laptops are available with sophisticated and high quality audio capabilities. Battery conservation is a key issue with laptop computers, and the circuit in Figure 5 utilizes the low supply current of the CMV1030, its rail to rail output voltage swing, and its high output current drive to provide the interface to the microphone input. A_1 is used to provide the common mode bias for A_2 by buffering the V_{REF} output (typically 2.2 volts) of the Codec and to supply bias to the microphone. R_1 should be selected for the appropriate bias for the microphone. R_3 and C_2 provide low pass filtering for noise, and the closed loop gain of A_2 is adjusted by the ratio of R_5 to R_4 .

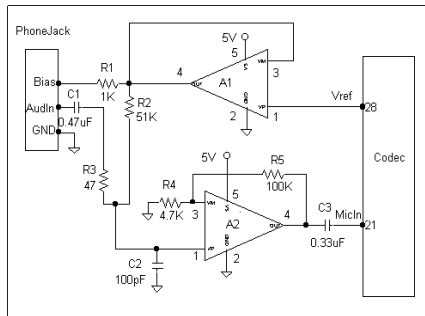


Figure 5