



Microcircuits

CMOS PCM Transmit/Receive Filters

Features

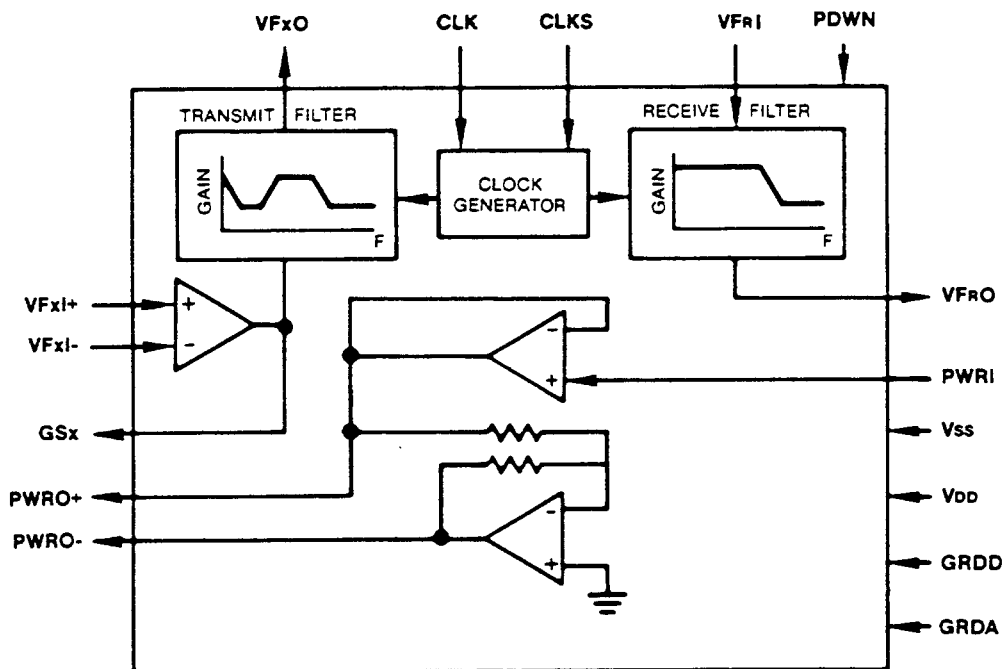
- Monolithic device includes both transmit and receive filters
- Compatible with Bell D3/D4 and CCITT G.712
- Transmit filter rejects 50/60Hz
- Receive filter includes Sin x/x correction
- External gain adjustment of both transmit and receive filters
- Direct interface with transformer or electronic 2-to-4 wire converters
- Low power consumption:
 - 20mW typical without power amps
 - 30mW typical with power amps
 - 0.4 mW Power Down Mode
- Anti-aliasing pre-filters on both transmit and receive filters
- Pin-for-pin compatible with Intel 2912

General Description

The CMD G8912B is a monolithic device containing both receive and transmit filters required for the analog termination of a PCM line or trunk. The transmit filter performs the 50-/60 Hz power line frequency rejection and the antialiasing function needed for an 8KHz sampling system. The receive filter has a pre-filter to eliminate aliasable codec noise, a low pass transfer characteristic and provides the Sin x/x correction required after D/A signal conversion by a suitable codec.

The G8912B is fabricated using CMD double-poly CMOS technology. Switched capacitors are used for the filter design. The G8912B interfaces directly with an electronic or transformer 2-to-4 wire converter. When interfacing with an electronic converter, the on-chip power amplifiers may be deactivated, thus reducing power dissipation.

Block Diagram



**Absolute Maximum Ratings:** (Note 1)

Parameter	Symbol	Value
V _{DD} With Respect to V _{SS}	V _{DC}	-0.3V to +14V
Input/Output Voltages With Respect to V _{SS}	V _{DC}	-0.3V to V _{DD}
All Output Currents	I _{DD} /I _{SS}	±50 mA
Operating Temperature	T _A	-40°C to +85°C
Storage Temperature	T _S	-65°C to +150°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated values.

Notes:

- Exceeding these ratings may result in permanent damage. Functional operation under these conditions is not implied.

DC and Operating Characteristics: GRDA = GRDD = 0V unless otherwise noted, V_{DD} = +5V, V_{SS} = -5V, T_A = 0°C to 70°C

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Operating Supply Voltages	V _{SS}	-5.25	-5	-4.75	V	Ref. to GRDA
	V _{DD}	4.75	5	5.25	V	
V _{DD} Standby Current	I _{DD0}		40	100	μA	PDWN = V _{DD}
V _{SS} Standby Current	I _{SS0}		10	100	μA	
V _{DD} Operating Current	I _{DD1}		2.0	4.0	mA	PWRI = V _{SS}
V _{SS} Operating Current	I _{SS1}		2.0	4.0	mA	Power Amps Inactive
V _{DD2} Operating Current	I _{DD2}		3.0	6.4	mA	With Power Amps
V _{SS2} Operating Current	I _{SS2}		3.0	6.4	mA	(Outputs Unloaded)
Input Load Current, CLK	I _{LIC}	-10	1	+10	μA	V _{IN} = 0 to V _{DD}
Input Load Current, CLKS	I _{LIS}	-10	1	+10	μA	V _{IN} = V _{SS} to V _{DD}
Input Load Current, PDWN	I _{LIP}	-100	-1	+100	μA	V _{IN} = 0 to V _{DD}
Input Low Voltage, CLK, PDWN	V _{IL}	0		0.8	V	
Input Low Voltage, CLKS	V _{ILS}	V _{SS}		V _{SS} + 0.5	V	
Input High Voltage, CLK, PDWN	V _{IH}	2.2		V _{DD}	V	
Input High Voltage, CLKS	V _{IHS}	V _{DD} - 0.5		V _{DD}	V	
Input Intermediate Voltage, CLKS	V _{IS}	-1.0		1.0	V	

Transmit Filter Gain Setting Amplifier

Input Leakage Current, VFxl +, VFxl-	I _{bxl}	-100		100	nA	V _{SS} < V _{IN} < V _{DD}
Input Resistance, VFxl +, VFxl-	R _{ixl}	10			MΩ	
Input Offset Voltage, VFxl +, VFxl-	V _{OSxl}	-25		+25	mV	
Power Supply Rejection, GSx	PSRR ₁	50	70		dB	
Common Mode Rejection, VFxl +, VFxl-	CMRR	55	65		dB	-2.5V ≤ V _{IN} ≤ +2.5V
DC Open Loop Voltage Gain, GSx	A _{VOL}	60	70		dB	
Open Loop Unity Gain Bandwidth, GSx	f _c		1.0		MHz	
Output Voltage Swing, GSx	V _{Oxl}	±2.5	±3.5		V	R _L ≥ 10 KΩ
Load Capacitance, GSx	CL _{xl}			50	pF	
Minimum Load Resistance, GSx	R _{Lxl}	10			KΩ	
Common-Mode Range, VFxl	V _{CM}	-2.5		+2.5	V	

Transmit Filter

Output Resistance, VFxO	R _{ox}		1	3	Ω	
Output DC Offset, VFxO	V _{OSx}	-150		+150	mV	VFxl + Connected to GRDA, Input Op Amp at unity gain
Power Supply Rejection of V _{DD} at 1KHz VFxO	PSRR ₂	33	38		dB	
Power Supply Rejection of V _{SS} at 1KHz VFxO	PSRR ₃	30	35		dB	
Load Capacitance, VFxO	CL _x			50	pF	
Minimum Load Resistance	R _{Lx}	10			KΩ	
Output Voltage, 1KHz, VFxO	V _{ox}	±3.2	±3.8		V	R _L ≥ 10 KΩ



DC and Operating Characteristics (Cont'd):

Receive Filter

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Leakage Current, VFRI	IBR			100	nA	VSS < VIN < VDD
Input Resistance, VFRI	RIR	10			MΩ	
Output Resistance, VFRO	ROR		5	7	Ω	
Output DC Offset, VFRO	VOSR	-150		+150	mV	VFRI Connected to GRDA
Power Supply Rejection of VCC at 1KHz, VFRO	PSRR4	35	40		dB	
Power Supply Rejection of VBB at 1KHz, VFRO	PSRR5	35	40		dB	
Load Capacitance, VFRO	CLR			50	pF	
Minimum Load Resistance, VFRO	RLR	10			KΩ	
Output Voltage Swing, VFRO	VOR	±3.2	±3.8		V	RL = 10KΩ

Receive Filter Driver Amplifiers

Input Leakage Current, PWRI	IBRA			3	μA	VSS < VIN < VDD
Input Resistance, PWRI	RIRA	10			MΩ	
Output Resistance, PWRO+, PWRO-	RORA		1	2	Ω	Iout < 5mA -3.0V < Vout < 3.0V
Output DC Offset, PWRO+, PWRO-	VOSRA	-50		-50	mV	PWRI Connected to GRDA
Load Capacitance, PWRO+, PWRO-	CLRA			100	pF	
Output Voltage Swing Across RL, PWRO-, PWRO-, Single Ended Connection	VORA1	±3.2			V	RL = 10KΩ
		±2.9			V	RL = 600Ω
		±2.5			V	RL = 300Ω
Differential Output Voltage Swing, PWRO-, PWRO-, Balanced Output Connection	VORA2	±6.4			V	RL = 20KΩ
		±5.8			V	RL = 1200Ω
		±5.0			V	RL = 600Ω

AC Characteristics: GRDA = GRDD = 0V unless otherwise noted, VDD = +5V, VSS = -5V, TA = 0°C to 70°C

Clock Input Frequency: CLK = 1.536MHz ± 0.1%, CLKS = VSS

CLK = 1.544MHz ± 0.1%, CLKS = GRDD

CLK = 2.048MHz ± 0.1%, CLKS = VDD

Transmit Filter

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Gain Relative to Gain at 1KHz	GRx					0dBmO Input Signal Gain Setting Op Amp at Unity Gain
Below 50Hz				-10	dB	
50Hz				-20	dB	
60Hz				-26	dB	
200Hz		-1.5		-0.125	dB	0dBmO Signal = 1.1 VRMS Input at VFxI+
300Hz to 3000Hz		-0.125		-0.125	dB	
3300Hz		-0.35		0.03	dB	
3400Hz		-0.8		-0.1	dB	
4000Hz				-14	dB	
4600Hz and Above				-32	dB	
Absolute Passband Gain at 1KHz, VFxO	GAX	2.9	3.0	3.1	dB	
Gain Variation with Temperature at 1KHz	GAXT		0.0004		dB/°C	0dBmO Signal Level
Gain Variation with Supplies at 1KHz	GAXS		0.01		dB/V	0dBmO Signal Level, Supplies ± 5%
Cross Talk, Receive to Transmit, Measured at VFxO $20 \log \left[\frac{VFxO}{VFRO} \right]$	CTRT		-85	-70	dB	VFRI = 2.20 VRMS, Freq. = 200Hz -3.4KHz; VFxI+, VFxI- Connected to GSx, GSx Connected through 10KΩ to GRDA
Total C Message Noise at Output, VFxO	NCS1		2	5	dBmC	Gain Setting Op Amp at Unity Gain
Total C Message Noise at Output, VFxO	Ncx2		3	6	dBmC	Gain Setting Op Amp at 20dB Gain

**AC Characteristics: (Cont'd)****Transmit Filter (cont.)**

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Differential Envelope Delay, VFxO 1KHz to 2.6KHz	Dox			70	μs	
Absolute Delay at 1KHz VFxO	DAX			185	μs	
Single Frequency Distortion Products	DPx1		-55	-48	dB	0dBm Input Signal at 1KHz
Single Frequency Distortion Products at Maximum Signal Level of + 3dBmO at VFxO	DPx2		-50	-48	dB	Gain Setting Op Amp at 20dB Gain. The -3dBmO signal at VFxO is 2.26 VRMS
Gaintracking Relative to GAX	GAXX	-0.1 -0.05 -0.1		+0.1 +0.05 +0.1	dB dB dB	Input Signal at 1KHz +3 to -2 dBmO +2 to -40 dBmO -40 to -50 dBmO

Receive Filter

Gain Relative to Gain at 1KHz with Sin x/x Correction	GRR					0dBmO Input Signal
Below 200Hz				0.125	dB	0dBmO Signal $\cong 1.6 \text{ VRMSX}$ $\left[\frac{\sin \frac{\pi F}{8000}}{\frac{\pi F}{8000}} \right]$ Input at VFRI
200Hz		-0.125		0.125	dB	
300Hz to 3000Hz		-0.125		0.125	dB	
3300Hz		-0.35		0.03	dB	
3400Hz		-0.8		-0.1	dB	
4000Hz				-14	dB	
4600Hz and Above				-30	dB	
Absolute Passband Gain at 1KHz, VFRO	GAR	-0.1	0	+0.1	dB	
Gain Variation with Temperature at 1KHz	GART		0.0004		dB/°C	0dBmO Signal Level
Gain Variation with Supplies at 1KHz	GARS		0.01		dB/V	0dBmO Signal Level, Supplies $\pm 5\%$
Cross Talk, Transmit to Receive, Measured at VFRO	CTTR		-80	-70	dB	VFxO = 2.26 VRMS, Freq. = 300Hz -3.4KHz, VFRI Connected to GRDA
Total C Messages Noise at Output, VFRO	NCR		3	5	dBrncO	VFRO Output or PWRO - and PWRO - Connected with Unity Gain
Differential Envelope Delay, VFRO 1KHz to 2.6KHz	DDR			85	μs	
Absolute Delay at 1KHz VFRO	DAR			110	μs	
Single Frequency Distortion Products	DPR1		-55	-48	dB	0dBm Input Signal at 1KHz
Single Frequency Distortion Products at Maximum Signal Level of + 3dBmO at VFRO	DPR2		-50	-48	dB	+3dBmO Signal Level of 2.26 VRMS, 1KHz Output at VFRO
Gaintracking Relative to GAR	GARR	-0.1 -0.05 -0.1		+0.1 -0.05 +0.1	dB dB dB	Input Signal at 1KHz +3 to +2 dBmO +2 to -40 dBmO -40 to -55 dBmO



Functional Description

Transmit Filter Input Stage

The input stage provides gain adjustment in the passband. The input operational amplifier has a common mode range of ± 3.2 volts, a DC offset of less than 25mV, a voltage gain of typically 2000 and a unity gain bandwidth of 1.0 MHz. It can be connected to provide a gain of 20dB without degrading the noise performance of the filter. The load impedance connected to the amplifier output must be greater than 10K Ω . The input signal on lead VFxl+ can be either AC or DC coupled. The input Op Amp can also be used in the inverting mode or differential amplifier mode. The remaining portion of the transmit filter provides a gain of +3dB in the pass band.

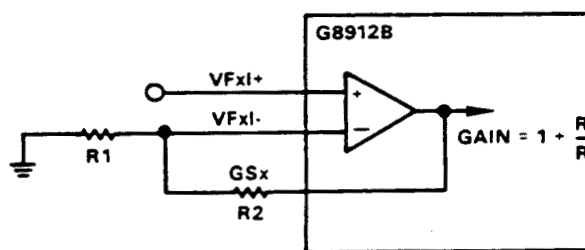


Fig. 1 Transmit Filter Gain Adjustment

50 Hz/60Hz Notch—Transmit Filter

The transmit filter has a notch section to reject 50Hz and 60Hz components of the input signal. A minimum attenuation of 26dB is provided at 60Hz. At 50Hz, the minimum attenuation is 20dB. The gain at 200Hz is between -0.125dB and -1.5dB. (All gain figures are relative to the gain at 1KHz.)

An active RC low pass anti-aliasing filter is included on chip immediately in front of the 50Hz/60Hz notch section. This filter provides greater than 35dB attenuation at 64KHz. As a result no external anti-aliasing components are required to provide the necessary anti-aliasing function for the switched capacitor sections of the transmit filter which operate at an internal sampling rate of 128KHz.

Transmit Filter Transfer Characteristics

The transmit section of filter provides a passband flatness and stopband attenuation which exceeds the Bell D3 and D4 specifications and the CCITT G.712 recommendations. The transmit filter transfer characteristics and specifications are shown in Fig. 2.

Transmit Filter Output Stage

The voltage range of the output signal on the VFxO lead is ± 3.2 volts. The DC offset is less than 150mV. The output stage includes an active RC post-filter to attenuate clock noise.

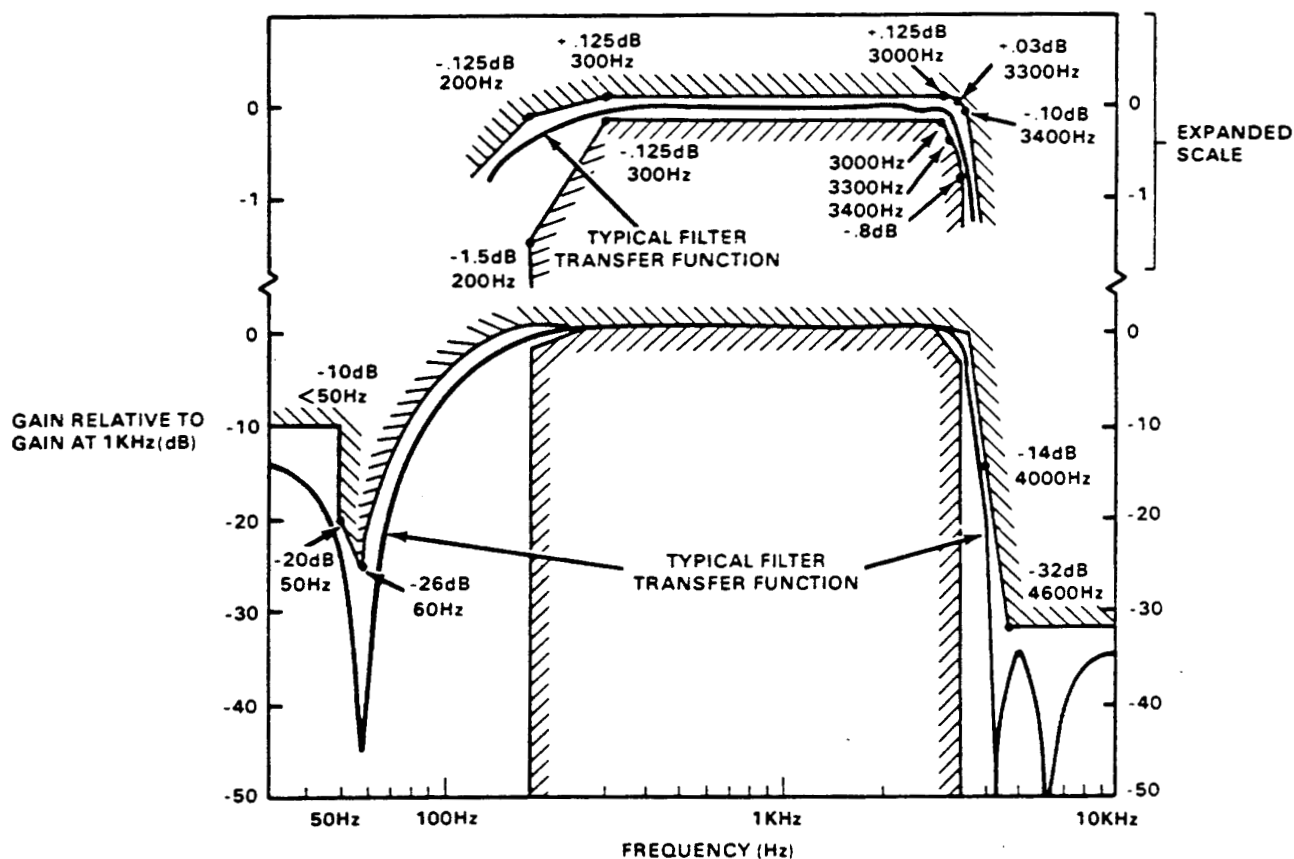


Fig. 2 Transmit Filter Transfer Characteristics

**Receive Filter Anti-Aliasing Prefilter**

An active RC low pass anti-aliasing filter is included on chip immediately preceding the receive filter section. This filter provides greater than 32dB rejection at 255KHz which is 1KHz below the receive filter effective sampling rate of 256KHz. This filter removes out-of-band noise generated by the codec which can be aliased in band by the filter. This results in significantly reduced harmonic distortion in the receive channel.

Receive Filter Transfer Characteristics

The receive section of the filter provides a passband flatness and stopband rejection which exceeds the Bell D3/D4 specifications and the CCITT G.712 recommendations, when used with a decoder which contains a sample/hold amplifier at its output. The filter contains the required compensation for the $\sin x/x$ response of such decoders. The receive filter transfer characteristics and specifications, including the $\sin x/x$ response of the decoder are shown in Fig. 3.

Receive Filter Output

The VFRO lead is capable of driving high impedance electronic hybrids. The gain of the receive section from VFRI TO VFRO is:

$$\text{Gain} = \frac{\left[\frac{\pi f}{8000} \right]}{\sin \left[\frac{\pi f}{8000} \right]}$$

which when multiplied by the output response of a suitable Codec results in a 0dB gain in the passband. The filter gain can be adjusted downward by a resistor voltage divider connected as shown in Fig. 4. The total resistive load R_T on VFRO should not be less than 10K Ω . The output stage includes an active RC post filter to attenuate clock noise.

Receive Filter Output Driver Amplifier Stage

A balanced power amplifier is provided in order to drive low-impedance loads in a bridged configuration. The receive filter output VFRO is connected through gain setting resistors R1 and R2 to the amplifier input PWRI. The series combination of RS and the hybrid transformer must present a minimum AC load resistance of 600 Ω to the amplifier in the bridged configuration. A typical connection of the output driver amplifiers is shown in Fig. 5. These amplifiers can also be used with loads connected to ground.

When the power amplifier is not needed it may be deactivated to save power. This is accomplished by tying the PWRI pin to VSS.

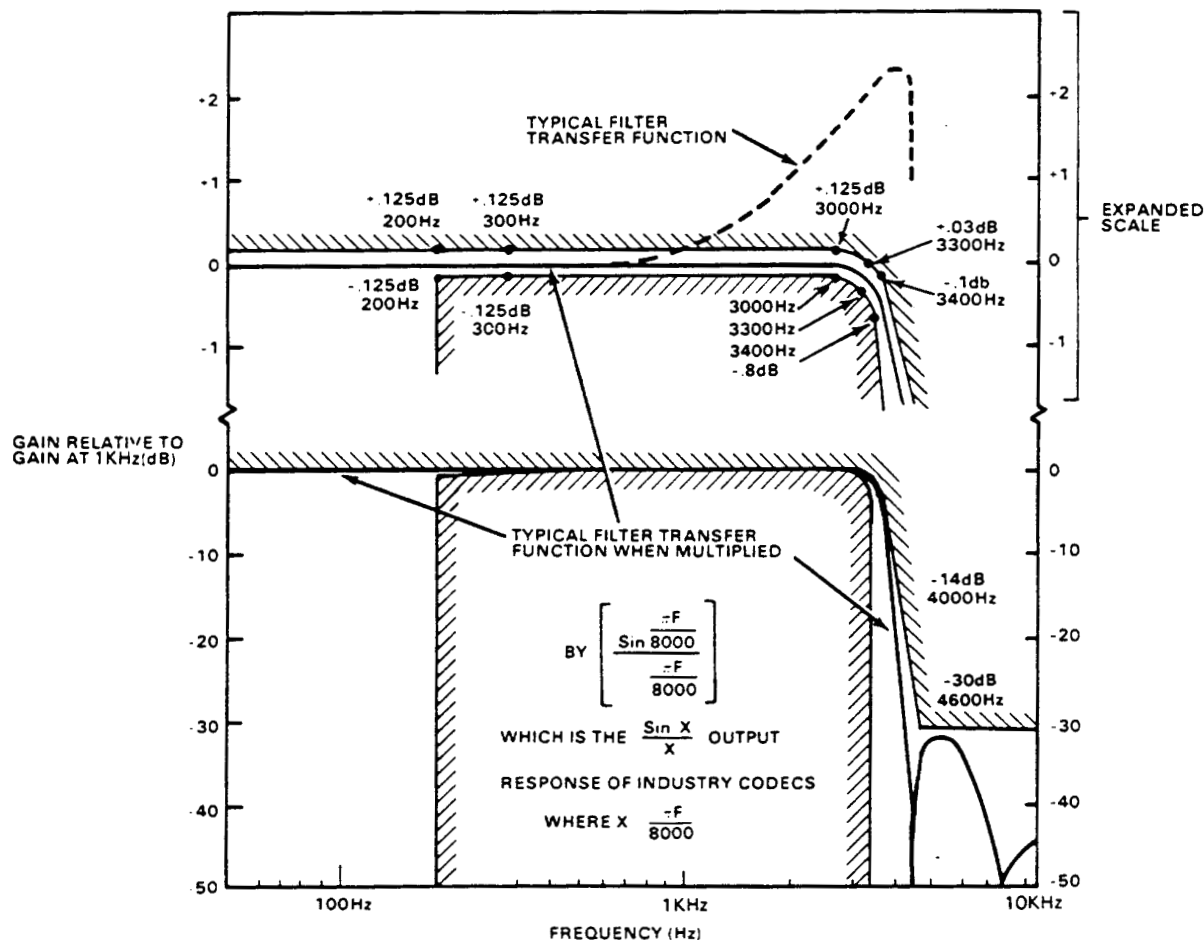


Fig. 3 Receive Filter Transfer Characteristics



$$R_T = R_1 + \frac{R_2 Z}{R_2 + Z} \geq 10K\Omega$$

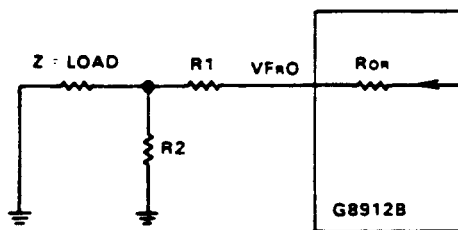


Fig. 4 Receive Filter Output Gain Adjustment

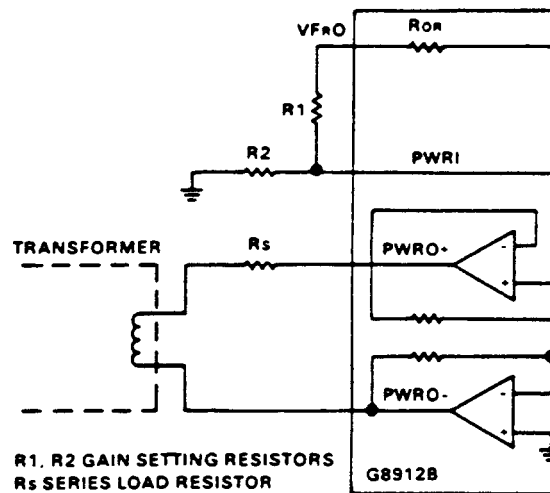


Fig. 5 Typical Connection of Output Driver Amplifier

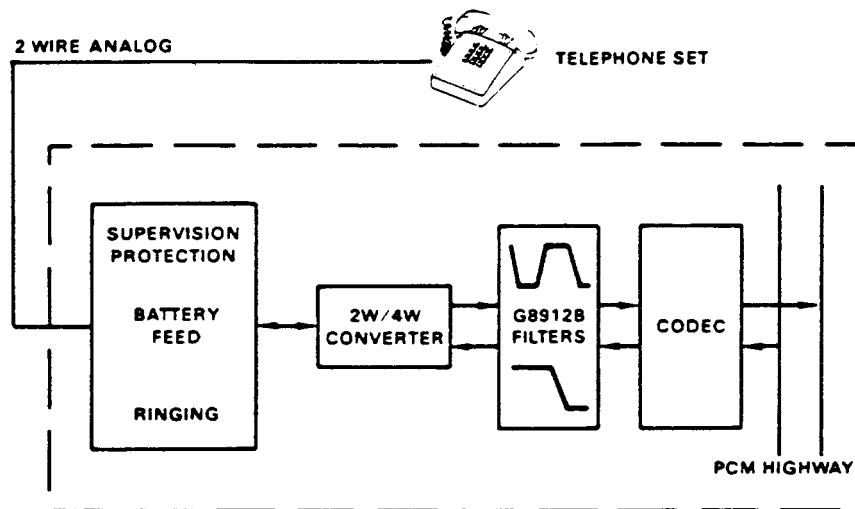


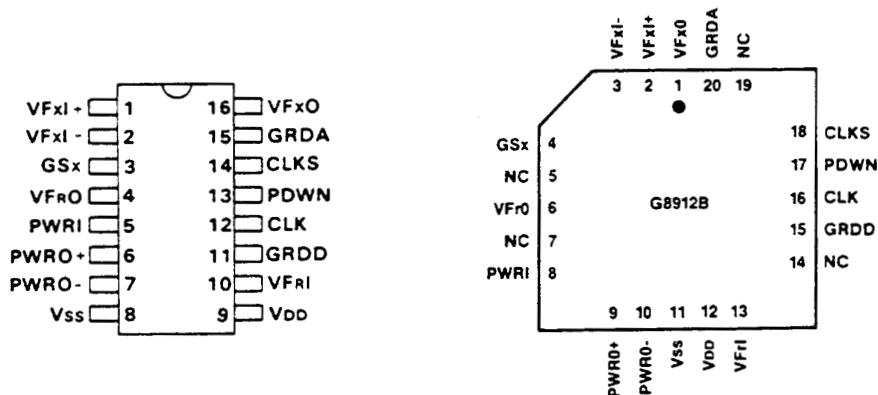
Fig. 6 Typical Line Termination



Pin Function Table

Name	Description
VFXI -	Analog input of the transmit filter from the 2 wire transmit output of a 2-to-4 wire converter
VFXI-	Inverting input of the gain adjustment op. amp on the transmit filter
GSX	Op. amp output used for gain setting of the transmit filter
VFR0	Analog output of the receive filter providing a direct interface to electronic 2-to-4 wire converter.
PWRI	Input to the power driver amplifiers. When tied to Vss these amplifiers are powered down
PWRO+ PWRO-	Power amplifier outputs capable of directly driving transformer 2-to-4 wire converters
Vss	Negative supply voltage (-5V)
VDD	Positive supply voltage (+5V)
VFRI	Analog input of the receive filter.
GRDD	Digital ground for internal clock generator.
CLK	Clock input. High impedance input. TTL-compatible voltage levels.
PDWN	Control input active high for the standby power down mode. Internal pull up to 5V. TTL-compatible voltage levels
CLKS	Clock frequency select. CLK Input 1.536MHz 1.544MHz 2.048MHz CLKS Connection Vss (-5V) GRDD VDD (+5V)
GRDA	Analog ground for receive and transmit filters. Not internally connected to GRDD
VFXO	Analog output of transmit filter

Pin Configuration



Ordering Information

Description	G	8912B	D	I
C—Special G—Standard				
Product Identification Number				
Package				
P—Plastic E—Leaded Chip Carrier				
C—Ceramic L—Leadless Chip Carrier				
D—Cerdip X—Dice				
Temperature/Processing				
None— 0°C to +70°C, ± 5% P.S. Tol.				
I— -40°C to +85°C, ± 5% P.S. Tol.				