

FEATURES

- Normally ON Configuration
- Low Interelectrode Capacitances
- High-Speed Switching
- Wide Dynamic Range

APPLICATIONS

- High-Speed Analog Switches
- Wide-Band Dual Differential Amplifiers
- Dual Cascode Amplifiers
- High Intercept Point Double Balanced Mixers

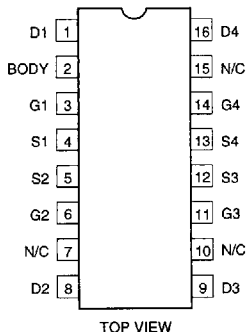
DESCRIPTION

The SD5501 is manufactured utilizing Calogic's proprietary high speed, low capacitance DMOS process featuring an N-Channel depletion-mode design. This "normally-ON" device is well suited for high speed instrumentation and communication systems where multiple channels are required for fast switching or dual amplification. Available in a 16-pin plastic dual in-line plastic package or chip form.

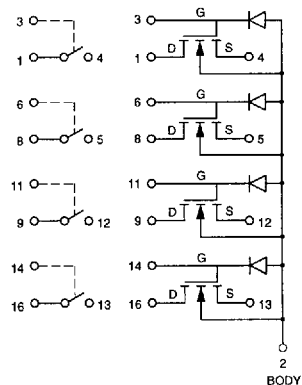
ORDERING INFORMATION

Part	Package	Temperature Range
SD5501N	Plastic	-55°C to +125°C
XSD5501	Sorted Chips in Carriers	-55°C to +125°C

PIN CONFIGURATION



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V _{DS}	Drain-Source Voltage	+30 Vdc	P _D	Total Package Power Dissipation (at or below T _A = +25°C)	640 mW
V _{SD}	Source-Drain Voltage	+0.5 Vdc		Linear Derating Factor	10.7 mW/°C
V _{DB}	Drain-Body Voltage	+30 Vdc	P _D	Single Device Power Dissipation (at or below T _A = +25°C)	300 mW
V _{SB}	Source-Body Voltage	+15 Vdc		Linear Derating Factor	5.0 mW/°C
V _{GS}	Gate-Source Voltage	+25 Vdc	T _J	Operating Junction Temperature Range	-55 to +85°C
V _{GB}	Gate-Body Voltage	+25 Vdc	T _S	Storage Temperature Range	-55 to +150°C
V _{GD}	Gate-Drain Voltage	-0.3 Vdc			
I _D	Continuous Drain Current	50 mA			

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
STATIC							
B _{VDS}	Drain-Source Breakdown Voltage	20			V	I _D = 10 nA, V _{GS} = V _{BS} = -5.6V	
B _{VSD}	Source-Drain Breakdown Voltage	10				I _S = 10 nA, V _{GD} = V _{BD} = -5.6V	
B _{VDB}	Drain-Body Breakdown Voltage	25				I _D = 10nA, V _{GB} = 0, Source Open	
B _{VSB}	Source-Body Breakdown Voltage	15				I _S = 10μA, V _{GB} = 0, Drain Open	
I _{GSS(fwd)}	Forward Gate Leakage Current			1.0	nA	V _{GS} = 25V, V _{DS} = V _{BS} = 0	
I _G	Gate Operating Current		-3.0	-100	pA	V _{DG} = 15V, I _D = 5.0 mA, V _{BS} = -5.6V	T _A = +125°C
			-0.7	-10	nA		
V _{GS (off)}	Gate - Source Cutoff Voltage	-1.0		-5.0	V	V _{DS} = 10V, I _D = 1.0μA, V _{BS} = 5.6V	
V _{GS (on)}	Gate-Source On Voltage	-0.3		-3.0		V _{DG} = 10V, I _D = 5mA, V _{SB} = -5.6V	
I _{DSX}	Zero Gate Voltage Drain Current	7.0		40	mA	V _{DS} = 10V, V _{GS} = 0, V _{BS} = -5.6V	T _A = +125°C
		5.0					
r _{DS (ON)}	Drain-Source On Resistance		100	150	ohms	I _D = 1.0mA, V _{GS} = 0, V _{BS} = -5.6V	
DYNAMIC							
g _{fs}	Common-Source Forward Transconductance ⁽¹⁾	6.0	7.5	12	mS	V _{DG} = 10V I _D = 5.0mA V _{BS} = -5.6V	f = 1 KHz
g _{os}	Common-Source Output Conductance		200	350	μS		f = 1 MHz
C _{iss}	Common-Source Input Capacitance		3.5		pF		
C _{oss}	Common-Source Output Capacitance		1.2				
C _{rss}	Common-Source Reverse Transfer Capacitance		0.3				
C _{i(gs + sb)}	Source Node Capacitance		4.5				
MATCHING							
V _{GSM}	Gate Source Voltage Match			50	mV	V _{DG} = 10V, I _D = 5.0 mA, V _{BS} = -5.6V	
r _{DS(on)}	Drain-Source On Resistance Match			10%		I _D = 1.0 mA, V _{GS} = 0, V _{BS} = 5.6V	
I _{DSM}	Zero Gate Voltage Drain Current Match			10%		V _{DG} = 10V, I _D = 5.0 mA, V _{BS} = -5.6V	f = 1 KHz
g _{fsm}	Transconductance Match ^{(1), (2)}			10%			

Note 1: Pulse Test, 80 sec, 1% Duty Cycle

Note 2: Match of 4 channels