

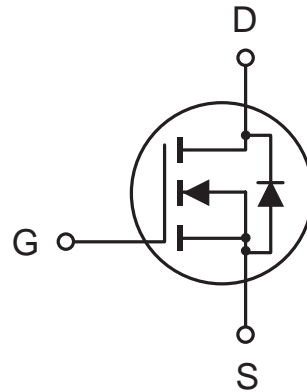
# CED603AL/CEU603AL

March 1998

## N-Channel Logic Level Enhancement Mode Field Effect Transistor

### FEATURES

- 30V , 20A ,  $R_{DS(ON)}=22m\Omega$  @  $V_{GS}=10V$ .  
 $R_{DS(ON)}=40m\Omega$  @  $V_{GS}=4.5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- TO-251 & TO-252 package.



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### ABSOLUTE MAXIMUM RATINGS ( $T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous @ $T_J=125^\circ\text{C}$ -Pulsed	$I_D$	20	A
	$I_{DM}$	77	A
Drain-Source Diode Forward Current	$I_S$	20	A
Maximum Power Dissipation @ $T_c=25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	50	W
		0.3	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$

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## ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V			1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V			±100	nA
ON CHARACTERISTICS <sup>a</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1	1.6	3	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =20A		18	22	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 10A		28	40	mΩ
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 10V	60			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 25A		35		S
DYNAMIC CHARACTERISTICS <sup>b</sup>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DD</sub> =15V, V <sub>GS</sub> = 0V f = 1.0MHz		770		pF
Output Capacitance	C <sub>OSS</sub>			330		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			100		pF
SWITCHING CHARACTERISTICS <sup>b</sup>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> = 15V, I <sub>D</sub> =20A, V <sub>GS</sub> = 10V, R <sub>GEN</sub> = 24Ω		15	30	ns
Rise Time	t <sub>r</sub>			55	110	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			95	150	ns
Fall time	t <sub>f</sub>			100	130	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 24V, I <sub>D</sub> = 20A, V <sub>GS</sub> =10V		20	26	nC
Gate-Source Charge	Q <sub>gs</sub>			3		nC
Gate-Drain Charge	Q <sub>gd</sub>			5		nC

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## ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>a</sup></b>						
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = 25A		0.95	1.3	V

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### Notes

a. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.

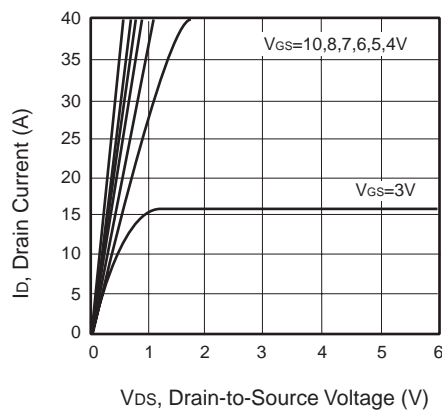


Figure 1. Output Characteristics

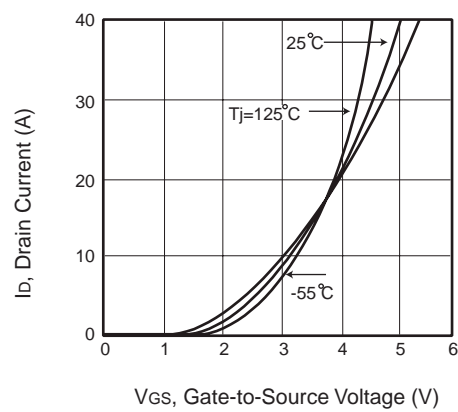


Figure 2. Transfer Characteristics

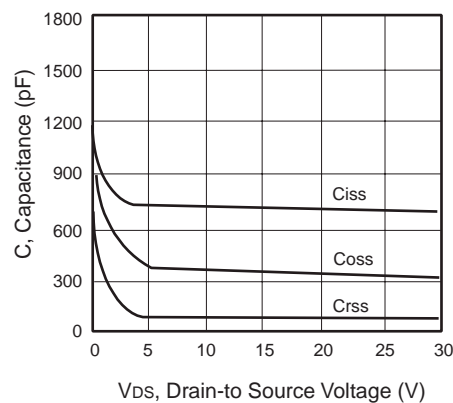


Figure 3. Capacitance

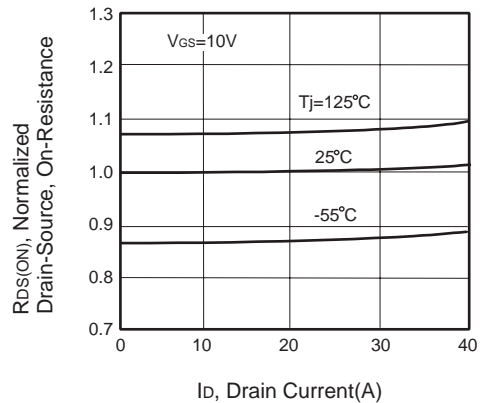
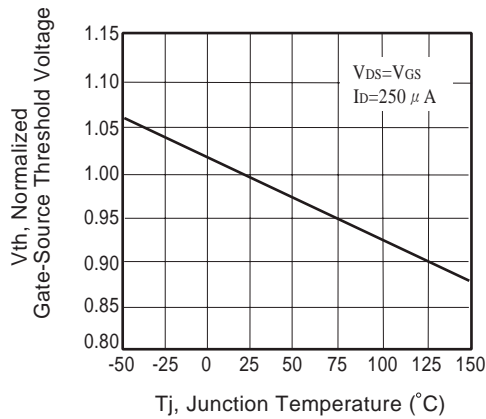


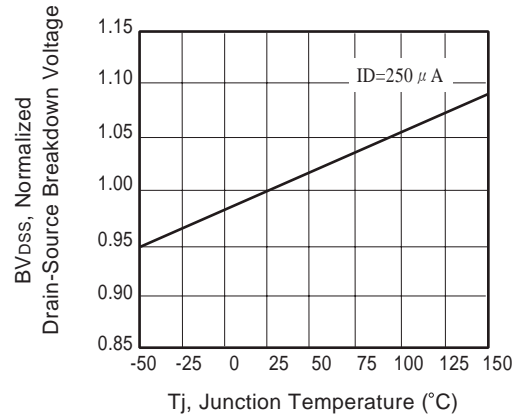
Figure 4. On-Resistance Variation with Drain Current and Temperature

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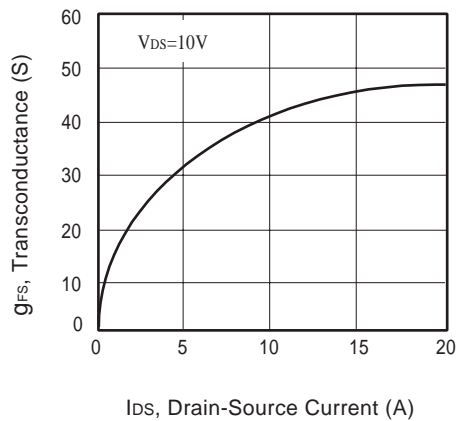
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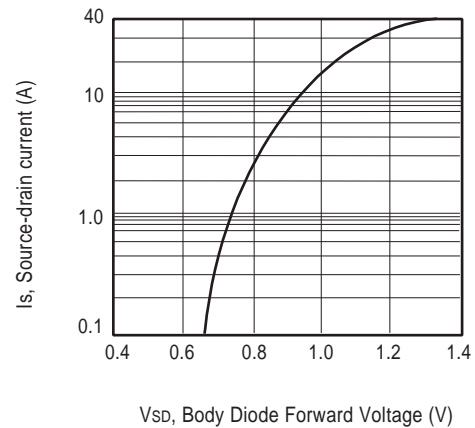
**Figure 5. Gate Threshold Variation with Temperature**



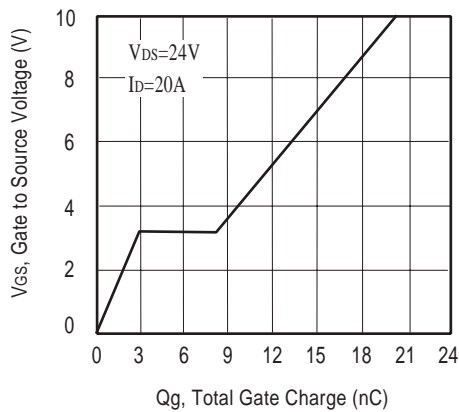
**Figure 6. Breakdown Voltage Variation with Temperature**



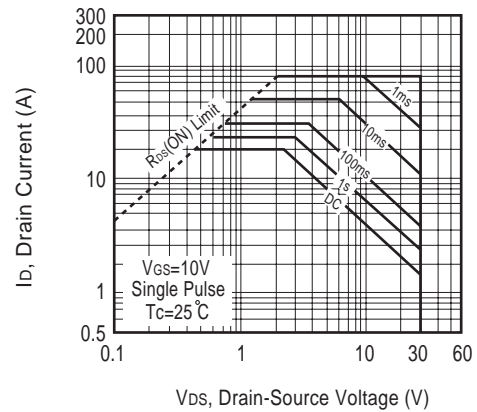
**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**



**Figure 9. Gate Charge**



**Figure 10. Maximum Safe Operating Area**

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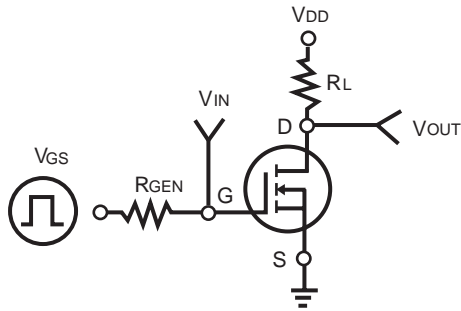


Figure 11. Switching Test Circuit

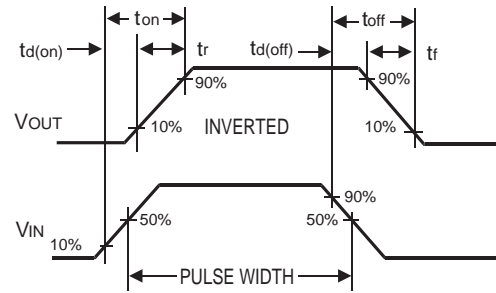


Figure 12. Switching Waveforms

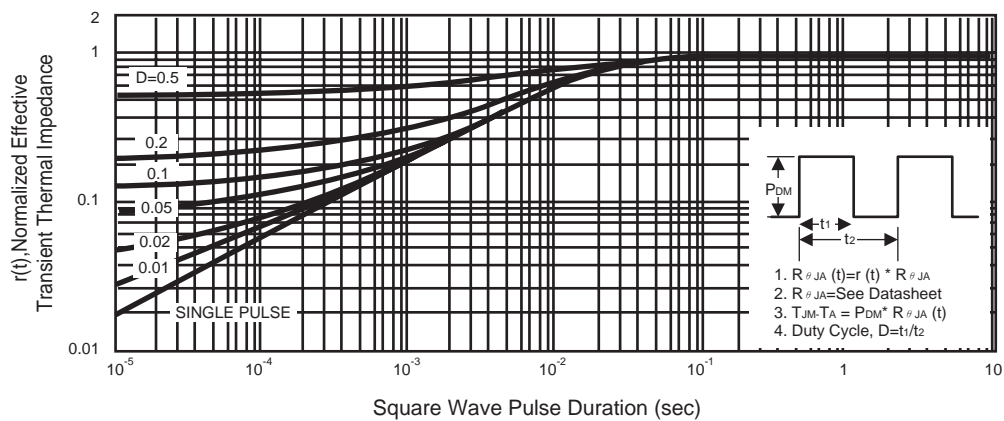


Figure 13. Normalized Thermal Transient Impedance Curve