



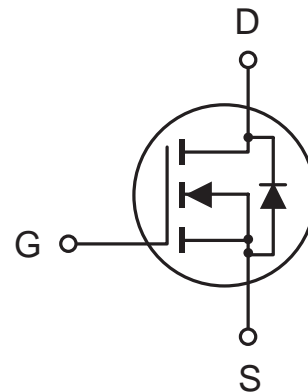
CED71A3/CEU71A3

Dec. 2002

N-Channel Logic Level Enhancement Mode Field Effect Transistor

FEATURES

- 30V , 65A , $R_{DS(ON)}=10m\Omega$ @ $V_{GS}=10V$.
 $R_{DS(ON)}=14m\Omega$ @ $V_{GS}=5.0V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- TO-252 & TO-251 package.



6

ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous -Pulsed	I_D	65	A
	I_{DM}	100	A
Drain-Source Diode Forward Current	I_S	65	A
Maximum Power Dissipation @ $T_c=25^\circ\text{C}$ Derate above 25°C	P_D	69	W
		0.56	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.8	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	40	$^\circ\text{C/W}$

CED71A3/CEU71A3

ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

6

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V			1	μA
Gate-Body Leakage	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V			±100	nA
ON CHARACTERISTICS ^a						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1		3	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 15A		8.5	10	mΩ
		V _{GS} = 5.0V, I _D = 13A		11.5	14	mΩ
On-State Drain Current	I _{D(ON)}	V _{GS} = 10V, V _{DS} = 5V	65			A
Forward Transconductance	g _{FS}	V _{DS} = 5V, I _D = 12A		26		S
DYNAMIC CHARACTERISTICS ^b						
Input Capacitance	C _{ISS}	V _{DS} =15V, V _{GS} = 0V f =1.0MHz		2152		pF
Output Capacitance	C _{OSS}			965		pF
Reverse Transfer Capacitance	C _{RSS}			234		pF
SWITCHING CHARACTERISTICS ^b						
Turn-On Delay Time	t _{D(ON)}	V _{DD} = 15V, I _D =1A, V _{GS} = 10V, R _{GEN} =6Ω		30	60	ns
Rise Time	t _r			63	110	ns
Turn-Off Delay Time	t _{D(OFF)}			73	130	ns
Fall Time	t _f			59	100	ns
Total Gate Charge	Q _g	V _{DS} =10V, I _D = 15A, V _{GS} =10V		55	67	nC
Gate-Source Charge	Q _{gs}			9		nC
Gate-Drain Charge	Q _{gd}			18		nC

CED71A3/CEU71A3

ELECTRICAL CHARACTERISTICS ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS ^a						
Diode Forward Voltage	V_{SD}	$V_{GS} = 0\text{V}, I_S = 2.3\text{A}$		0.9	1.3	V

6

Notes

a. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

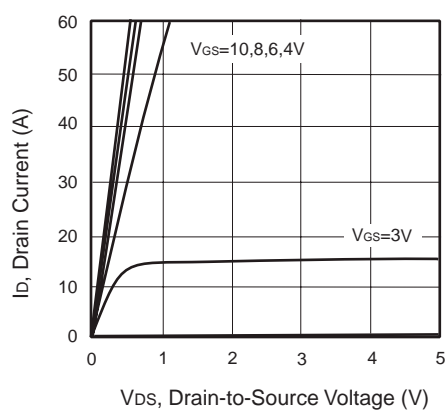


Figure 1. Output Characteristics

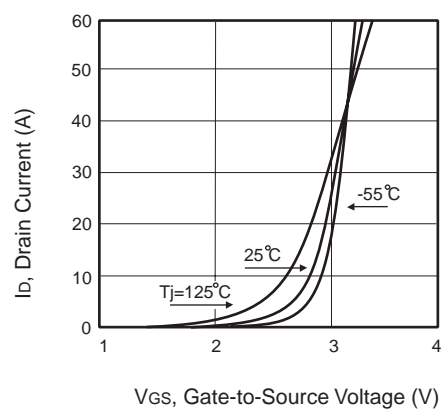


Figure 2. Transfer Characteristics

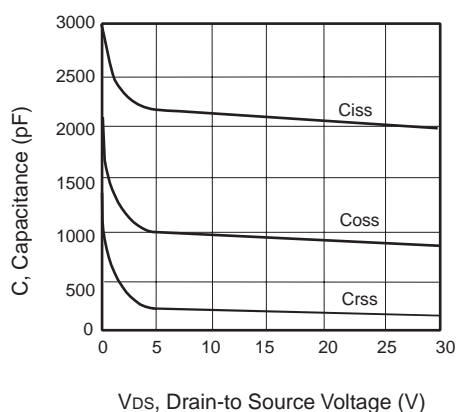


Figure 3. Capacitance

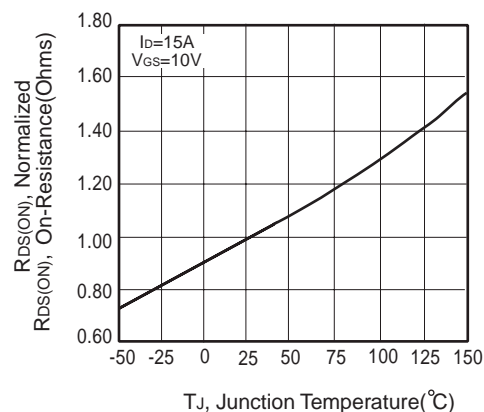


Figure 4. On-Resistance Variation with Temperature

CED71A3/CEU71A3

6

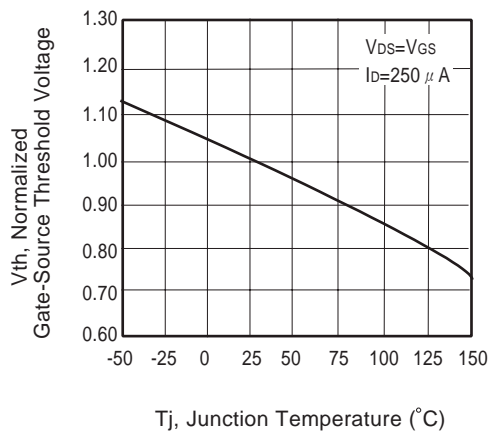


Figure 5. Gate Threshold Variation with Temperature

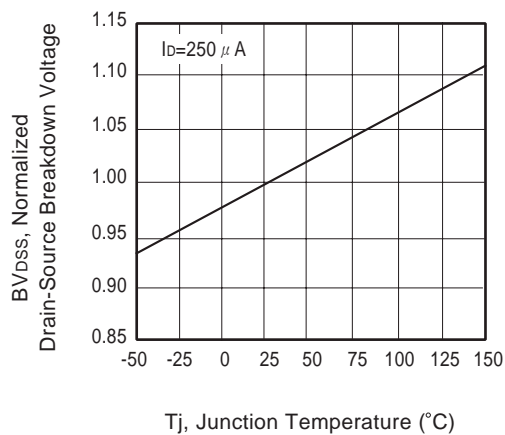


Figure 6. Breakdown Voltage Variation with Temperature

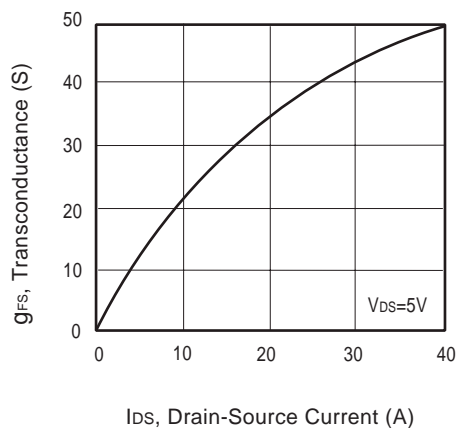


Figure 7. Transconductance Variation with Drain Current

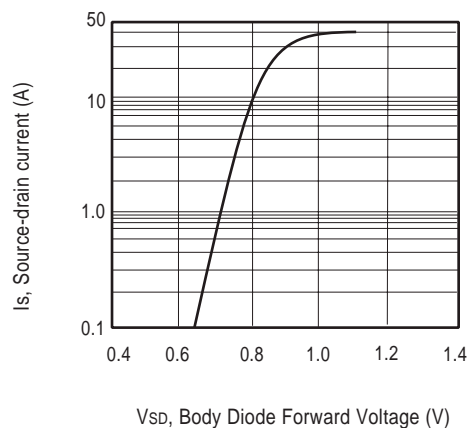


Figure 8. Body Diode Forward Voltage Variation with Source Current

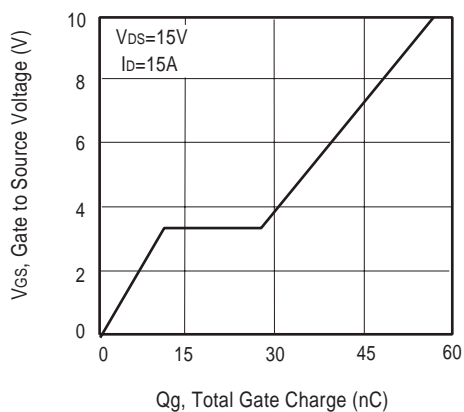


Figure 9. Gate Charge

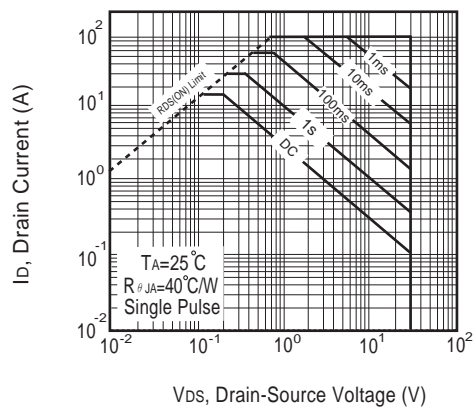


Figure 10. Maximum Safe Operating Area

CED71A3/CEU71A3

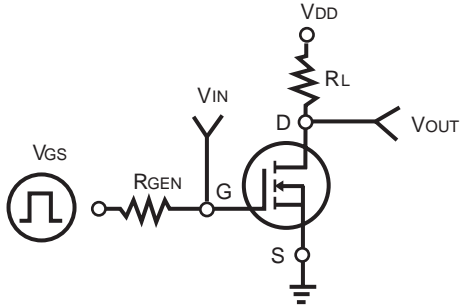


Figure 11. Switching Test Circuit

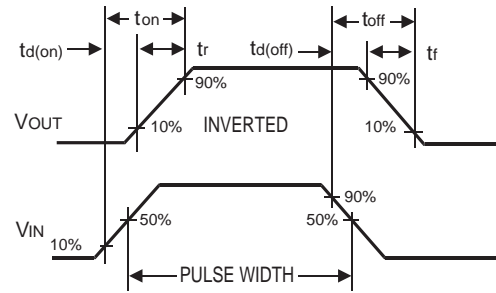


Figure 12. Switching Waveforms

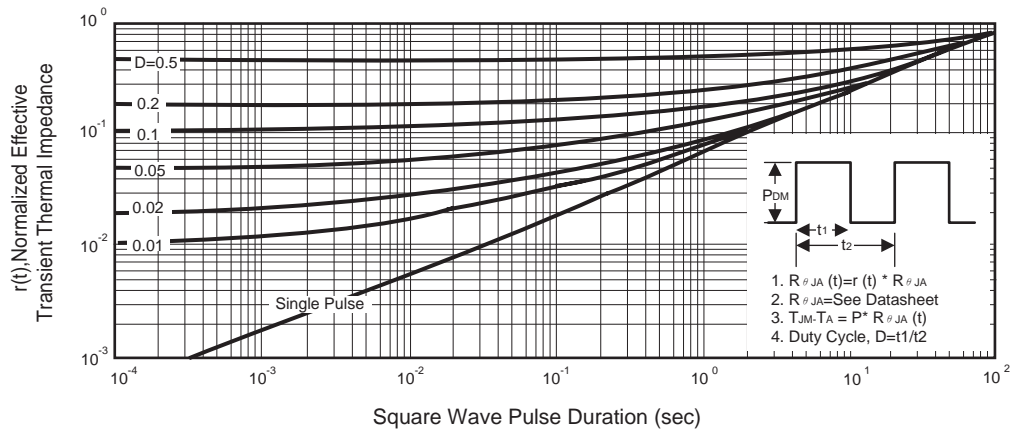


Figure 13. Normalized Thermal Transient Impedance Curve