

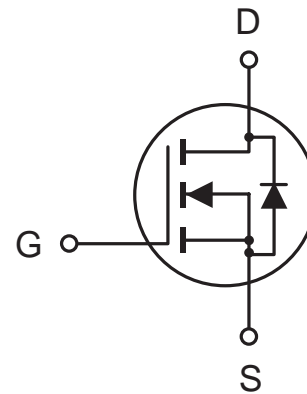
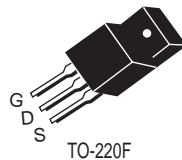
# CEF07N8

PRELIMINARY

## N-Channel Logic Level Enhancement Mode Field Effect Transistor

### FEATURES

- 800V , 4A ,  $R_{DS(ON)}=2\Omega$  @  $V_{GS}=10V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- TO-220F full-pak for through hole



6

### ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	VDS	800	V
Gate-Source Voltage	VGS	± 30	V
Drain Current-Continuous -Pulsed	ID	4	A
	IDM	12	A
Drain-Source Diode Forward Current	IS	4	A
Maximum Power Dissipation @Tc=25°C Derate above 25°C	PD	50	W
		0.4	W/°C
Operating and Storage Temperature Range	TJ, TSTG	-55 to 150	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	65	°C/W

# CEF07N8

## ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

6

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE AVALANCHE RATING<sup>a</sup></b>						
Single Pulse Drain-Source Avalanche Energy	E <sub>AS</sub>	V <sub>DD</sub> = 50V, L = 30.6mH R <sub>G</sub> = 25Ω		500		mJ
Maximum Drain-Source Avalanche Current	I <sub>AS</sub>			7		A
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	800			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 800V, V <sub>GS</sub> = 0V			50	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±30V, V <sub>DS</sub> = 0V			±100	nA
<b>ON CHARACTERISTICS<sup>a</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2		4	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 4A		1.8	2.0	Ω
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 10V	4			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 50V, I <sub>D</sub> = 4A		3		S
<b>SWITCHING CHARACTERISTICS<sup>b</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> = 400V, I <sub>D</sub> = 6A, V <sub>GS</sub> = 10V R <sub>GEN</sub> = 25Ω		32	45	ns
Rise Time	t <sub>r</sub>			68	95	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			194	230	ns
Fall Time	t <sub>f</sub>			70	98	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 640V, I <sub>D</sub> = 6A, V <sub>GS</sub> = 10V		70	85	nC
Gate-Source Charge	Q <sub>gs</sub>			8		nC
Gate-Drain Charge	Q <sub>gd</sub>			36		nC

# CEF07N8

## ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS <sup>b</sup>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> = 0V f =1.0MHz		1500		pF
Output Capacitance	C <sub>OSS</sub>			125		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			50		pF
DRAIN-SOURCE DIODE CHARACTERISTICS <sup>a</sup>						
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> =4A			1.5	V

### Notes

a.Pulse Test:Pulse Width≤300 μs, Duty Cycle ≤2%.

b.Guaranteed by design, not subject to production testing.

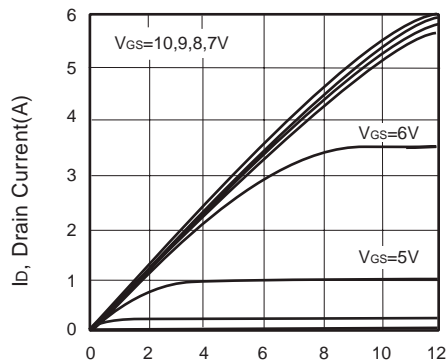


Figure 1. Output Characteristics

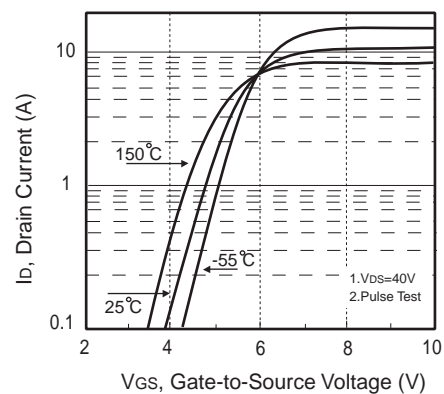


Figure 2. Transfer Characteristics

# CEF07N8

6

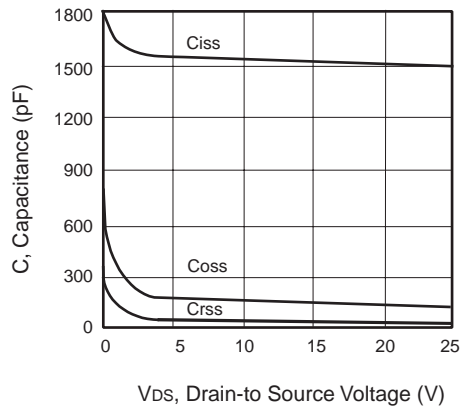


Figure 3. Capacitance

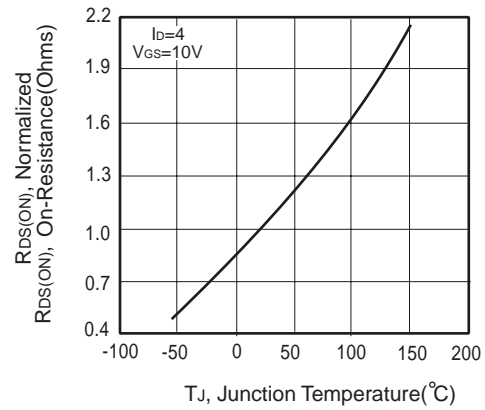


Figure 4. On-Resistance Variation with Temperature

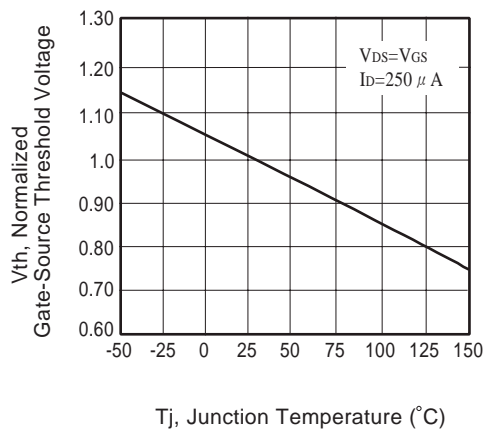


Figure 5. Gate Threshold Variation with Temperature

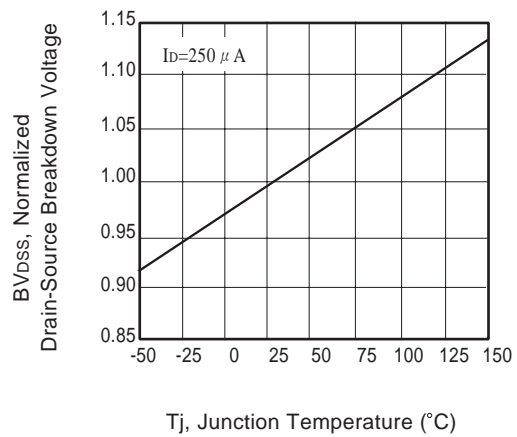


Figure 6. Breakdown Voltage Variation with Temperature

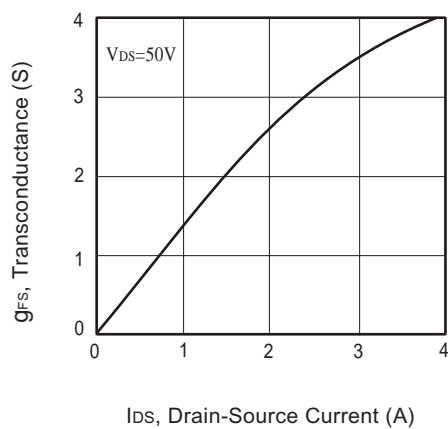


Figure 7. Transconductance Variation with Drain Current

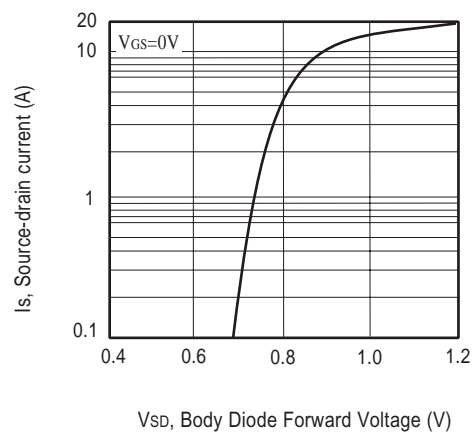


Figure 8. Body Diode Forward Voltage Variation with Source Current

# CEF07N8

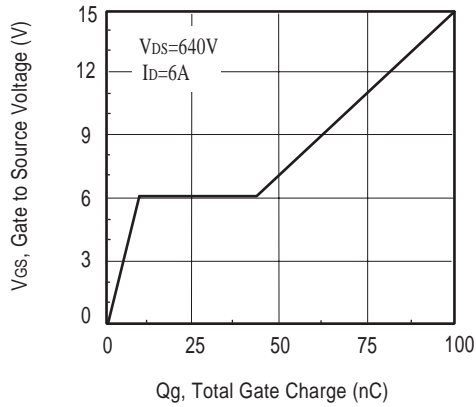


Figure 9. Gate Charge

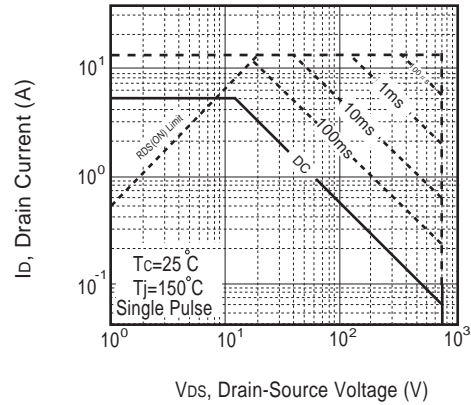


Figure 10. Maximum Safe Operating Area

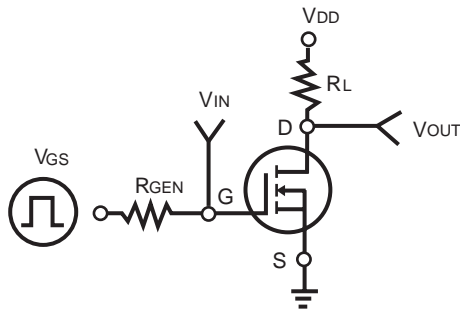


Figure 11. Switching Test Circuit

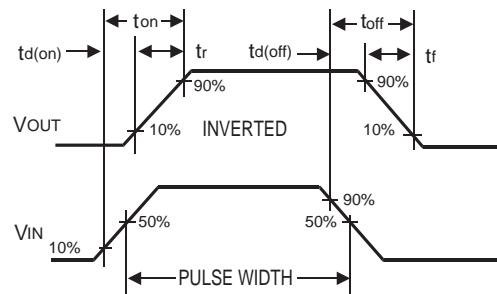


Figure 12. Switching Waveforms

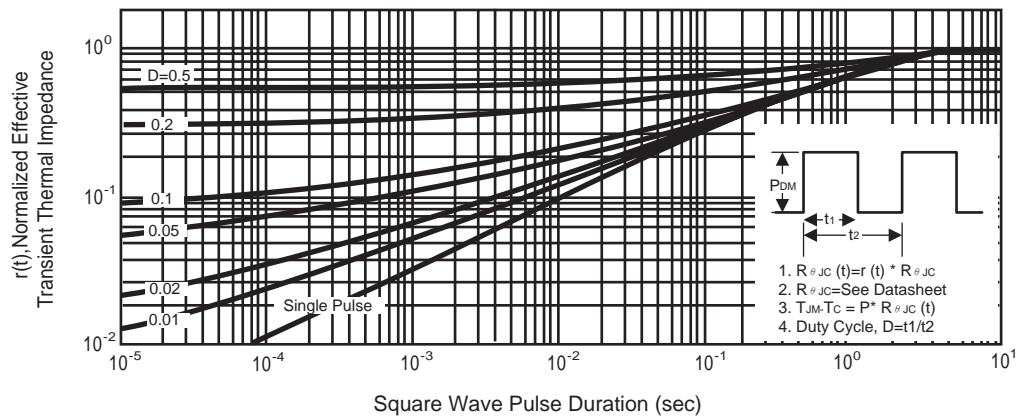


Figure 13. Normalized Thermal Transient Impedance Curve