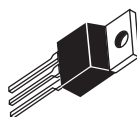


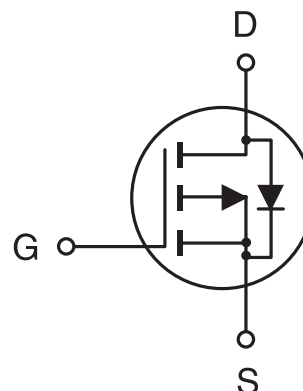
## Single P-Channel Enhancement Mode MOSFET

### FEATURES

- -30V , -4.9A ,  $R_{DS(ON)}=70m\Omega$  @  $V_{GS}=-10V$   
 $R_{DS(ON)}=120m\Omega$  @  $V_{GS}=-4.5V$
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- TO-220 package for through hole.



CEP SERIES  
TO-220



### ABSOLUTE MAXIMUM RATINGS ( $T_c=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous @ $T_J=125^{\circ}\text{C}$ -Pulsed	$I_D$	$\pm 4.9$	A
	$I_{DM}$	$\pm 30$	A
Drain-Source Diode Forward Current	$I_S$	-1.7	A
Maximum Power Dissipation	$P_D$	50	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^{\circ}\text{C}$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^{\circ}\text{C/W}$
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## ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =-250μA	-30	-35		V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V			-1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =20V, V <sub>DS</sub> =0V			100	nA
ON CHARACTERISTICS <sup>a</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = -250μA	-1	-1.6	-3	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-4.9A		50	70	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-2.0A		100	120	mΩ
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> =-5V, V <sub>GS</sub> =-10V	-20			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-15V, I <sub>D</sub> =-4.9A	5			S
DYNAMIC CHARACTERISTICS <sup>b</sup>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V f =1.0MHz		840	1200	pF
Output Capacitance	C <sub>OSS</sub>			420	600	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			140	200	pF
SWITCHING CHARACTERISTICS <sup>b</sup>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> = -15V, I <sub>D</sub> = -1A, V <sub>GEN</sub> = -10V, R <sub>GEN</sub> = 6Ω R <sub>L</sub> = 15Ω		8	15	ns
Rise Time	t <sub>r</sub>			11	20	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			23	40	ns
Fall time	t <sub>f</sub>			14	25	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -15V, I <sub>D</sub> = -4.9A, V <sub>GS</sub> = -10V		16	25	nC
Gate-Source Charge	Q <sub>gs</sub>			5		nC
Gate-Drain Charge	Q <sub>gd</sub>			2		nC

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## ELECTRICAL CHARACTERISTICS ( $T_c=25^\circ\text{C}$ unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>a</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0\text{V}$ , $I_S = -1.7\text{A}$		-0.79	-1.2	V

### Notes

a. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

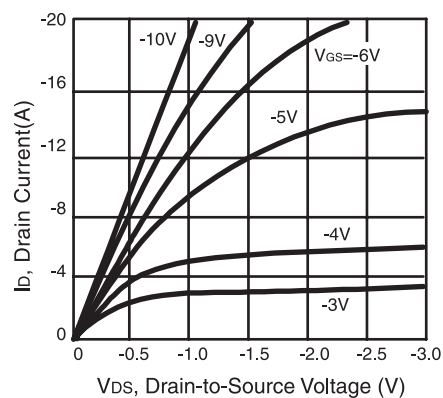


Figure 1. Output Characteristics

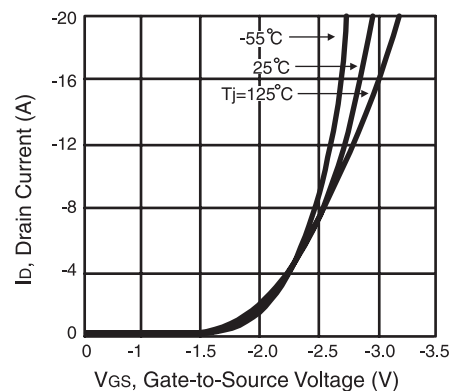


Figure 2. Transfer Characteristics

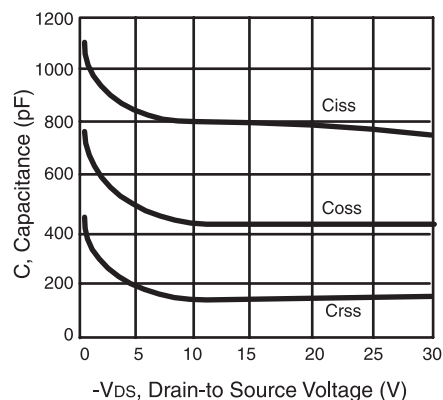


Figure 3. Capacitance

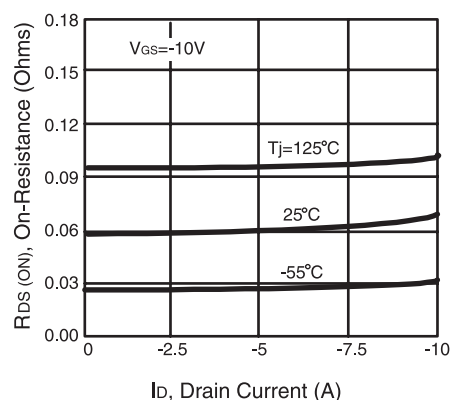
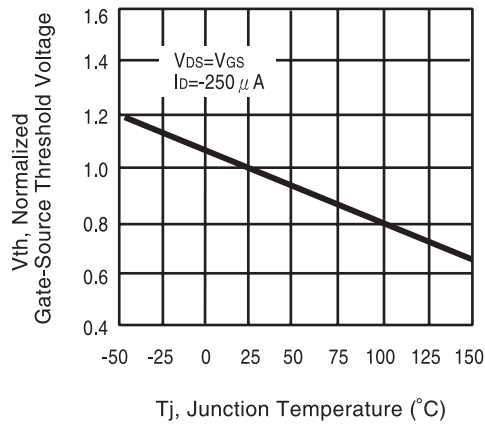
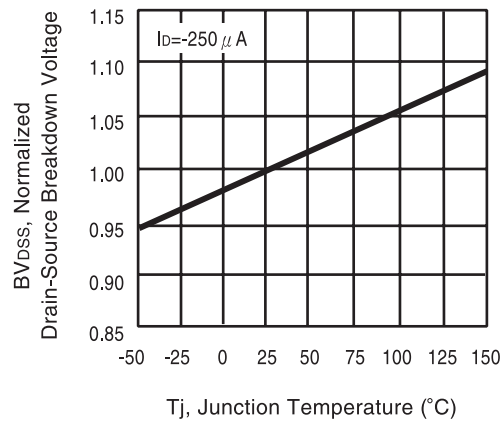


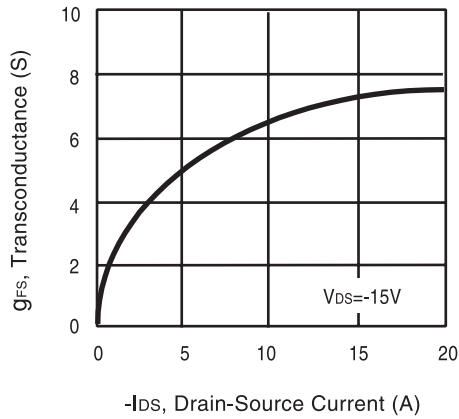
Figure 4. On-Resistance Variation with Drain Current and Temperature



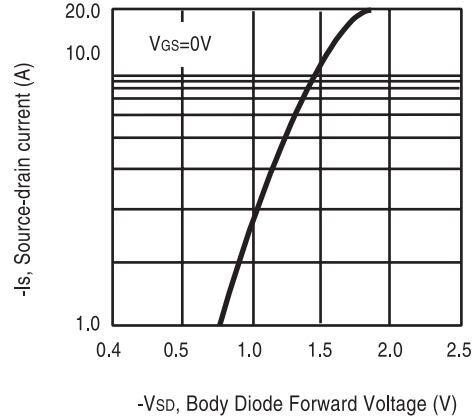
**Figure 5. Gate Threshold Variation with Temperature**



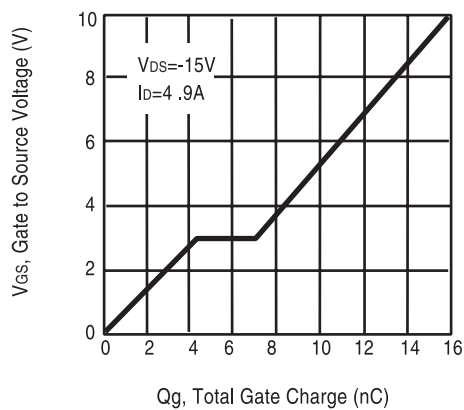
**Figure 6. Breakdown Voltage Variation with Temperature**



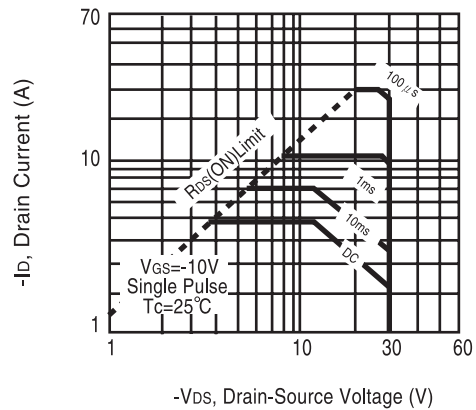
**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**



**Figure 9. Gate Charge**



**Figure 10. Maximum Safe Operating Area**

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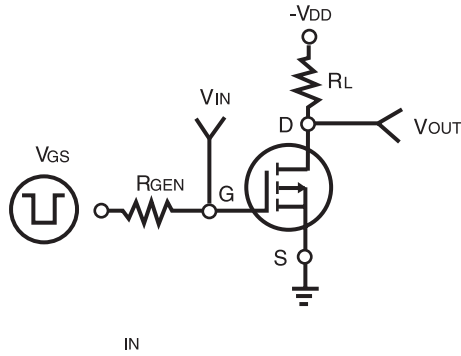


Figure 11. Switching Test Circuit

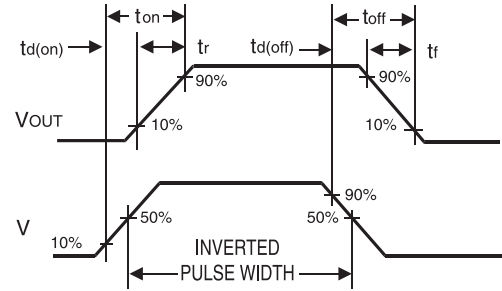


Figure 12. Switching Waveforms

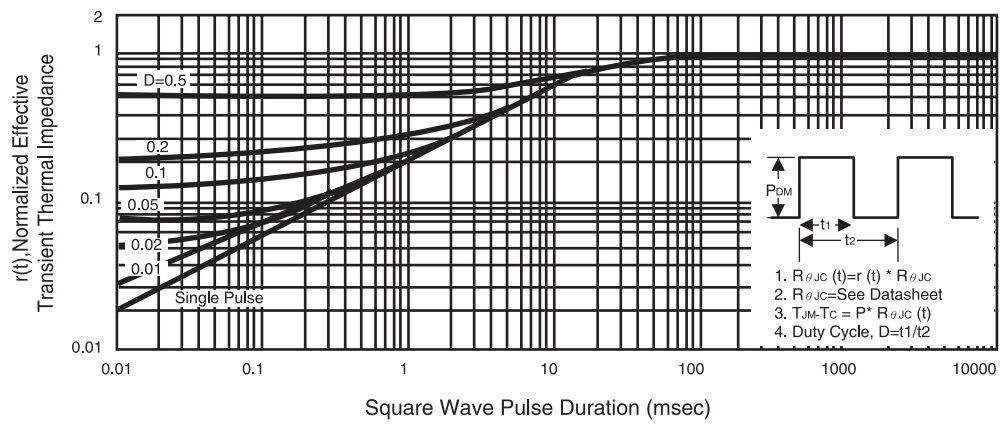


Figure 13. Normalized Thermal Transient Impedance Curve