
CC1020**Single Chip Low Power RF Transceiver for Narrow Band Systems**

Applications

- *Narrowband low power UHF wireless data transmitters and receivers*
- *402 / 426 / 429 / 433 / 868 and 915 MHz ISM/SRD band systems*
- *AMR – Automatic Meter Reading*
- *Wireless alarm and security systems*
- *Home automation*
- *Low power telemetry*

Product Description

CC1020 is a true single-chip UHF transceiver designed for very low power and very low voltage wireless applications. The circuit is mainly intended for the ISM (Industrial, Scientific and Medical) and SRD (Short Range Device) frequency bands at 402, 426, 429, 433, 868 and 915 MHz, but can easily be programmed for multi-channel operation at other frequencies in the 402 - 470 and 804 - 940 MHz range.

The **CC1020** is especially suited for narrow-band systems, e.g. with channel widths of 12.5 or 25 kHz complying with ARIB STD T-67 and EN 300 220.

The **CC1020** main operating parameters can be programmed via an easily interfaced serial bus, thus making **CC1020** a very flexible and easy to use transceiver.

In a typical system **CC1020** will be used together with a microcontroller and a few external passive components.

CC1020 is based on Chipcon's SmartRF[®]-02 technology in 0.35 μ m CMOS.

**Features**

- True single chip UHF RF transceiver
- Frequency range 402 MHz - 470 MHz and 804 MHz - 940 MHz
- High sensitivity (up to -121 dBm for a 12.5 kHz channel)
- Programmable output power
- Low current consumption (RX: 17 mA)
- Low supply voltage (2.3 V to 3.6 V)
- No external IF filter needed
- Low-IF receiver
- Very few external components required
- Small size (QFN 32 package)
- Digital RSSI and carrier sense indicator
- Single port antenna connection
- Data rate up to 153.6 kBaud
- OOK/ASK, FSK and GFSK data modulation
- Integrated bit synchronizer
- Image rejection mixer
- Programmable frequency and AFC make crystal temperature drift compensation possible without TCXO
- Suitable for frequency hopping systems
- Complies with EN 300 220, FCC CFR47 part 15, and ARIB STD T-67
- Development kit available
- Easy-to-use software for generating the **CC1020** configuration data

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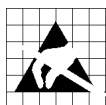
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Absolute Maximum Ratings

Parameter	Min.	Max.	Units	Condition
Supply voltage, VDD	-0.3	5.0	V	
Voltage on any pin	-0.3	VDD+0.3, max 5.0	V	
Input RF level		10	dBm	
Storage temperature range	-50	150	°C	
Reflow soldering temperature		260	°C	T = 10 s

The absolute maximum ratings given above should under no circumstances be violated. Stress exceeding one or more of

the limiting values may cause permanent damage to the device.



Caution! ESD sensitive device.
Precaution should be used when handling the device in order to prevent permanent damage.

Electrical Specifications

T_c = 25°C, AVDD = DVDD = 3.0 V if nothing else stated. Crystal frequency = 14.7456 MHz.
All measurements were performed using the test circuit shown in Figure 3.

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Overall					
RF Frequency Range	402 804		470 940	MHz MHz	Programmable in <300 Hz steps Programmable in <600 Hz steps
Operating ambient temperature range	-40		85	°C	
Supply voltage	2.3	3.0	3.6	V	Note: The same supply voltage should be used for digital (DVDD) and analogue (AVDD) power.
Transmit Section					
Transmit data rate	0.45		153.6	kBaud	Data rate is programmable. See "Data rate programming" on page 27 for details. NRZ or Manchester encoding can be used. 153.6 kBaud equals 153.6 kbps using NRZ coding. See page 21. Minimum data rate for OOK/ASK is 2.4 kBaud
Binary FSK frequency separation	0 0		108 216	kHz kHz	in 402 - 470 MHz range in 804 - 940 MHz range The frequency separation is programmable in 250 Hz steps. 108/216 kHz is the maximum guaranteed separation at 1.84 MHz reference frequency. Larger separations can be achieved at higher reference frequencies.
Output power 433 MHz 868 MHz	-20 -20		10 5	dBm dBm	Delivered to 50 Ω load. The output power is programmable.

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Output power tolerance		-4 3		dB dB	At maximum output power At 2.3 V, +85°C At 3.6 V, -40°C
Harmonics 2 nd harmonic, 433 MHz, +10 dBm 3 rd harmonic, 433 MHz, +10 dBm 2 nd harmonic, 868 MHz, +5 dBm 3 rd harmonic, 868 MHz, +5 dBm		-60 -65 -54 -60		dBc dBc dBc dBc	An external LC Filter is used to suppress harmonics.
Adjacent channel power (GFSK) 12.5 kHz channel width, 426 MHz 25 kHz channel width, 868 MHz		-46 -51		dBc dBc	ACP is measured in a ± 4.25 and ± 8.5 kHz bandwidth at 12.5 and 25 kHz offsets for 12.5 and 25 kHz channel widths respectively. Modulation for 12.5/25 kHz channel width: 2.4/4.8 kBaud NRZ PN9 sequence, $\pm 2.0/2.4$ kHz frequency deviation.
Occupied bandwidth (99.5%,GFSK) 12.5 kHz channel width, 426 MHz 25 kHz channel width, 868 MHz		7 9		kHz kHz	Bandwidth for 99.5% of total average power. Modulation for 12.5/25 kHz channel width: 2.4/4.8 kBaud NRZ PN9 sequence, $\pm 2.0/2.4$ kHz frequency deviation.
Spurious emission 47-74, 87.5-118, 174-230, 470-862 MHz 9 kHz – 1 GHz 1 – 4 GHz			-54 -36 -30	dBm dBm dBm	10/5 dBm at 433/868 MHz Modulation is 2.4 kBaud, Manchester coded data, ± 2.0 kHz frequency deviation. An external LC filter must be used to reduce out-of-band spurs. Complying with EN 300 220, FCC CFR47 part 15 and ARIB STD T-67.
Optimum load impedance 434 MHz 868 MHz 915 MHz		57 + j106 36 + j74 57 + j76		Ω Ω Ω	Transmit mode, series equivalent. For matching details see "Input/ output matching" on page 53.
Optimum load admittance 434 MHz 868 MHz 915 MHz		250 Ω 50 nH 180 Ω 17 nH 160 Ω 20 nH			Transmit mode, parallel equivalent. For matching details see "Input/ output matching" on page 53.

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Receive Section					
Receiver Sensitivity, 433 MHz, FSK 12.5 kHz channel width, optimized selectivity. ± 2.0 kHz freq. deviation		-117		dBm	Sensitivity is measured with PN9 sequence at $BER = 10^{-3}$ 12.5 kHz channel width: 2.4 kBaud, Manchester coded data. 25 kHz channel width: 4.8 kBaud, NRZ coded data, ± 2.4 kHz frequency deviation. 500 kHz channel width: 153.6 kBaud, NRZ, ± 76.8 kHz frequency deviation. See Table 6, page 38 for typical sensitivity figures at other data rates.
12.5 kHz channel width, optimized sensitivity. ± 2.4 kHz freq. deviation		-121		dBm	
25 kHz channel width		-115		dBm	
500 kHz channel width		-97		dBm	
Receiver Sensitivity, 868 MHz, FSK 12.5 kHz channel width		-116		dBm	
25 kHz channel width		-112		dBm	
500 kHz channel width		-94		dBm	
Receiver sensitivity, 433 MHz, ASK 2.4 kBaud 153.6 kBaud		-116 -81		dBm dBm	
Receiver sensitivity, 868 MHz, ASK 4.8 kBaud 153.6 kBaud		-107 -87		dBm dBm	Manchester coded data. See Table 8 for typical sensitivity figures at other data rates.
Saturation (maximum input level) FSK/ASK 2.4 kBaud, 433 MHz 153.6 kBaud, 433 MHz		7 9		dBm dBm	FSK: Manchester/NRZ coded data, ASK: Manchester coded data $BER = 10^{-3}$
4.8 kBaud, 868 MHz 153.6 kBaud, 868 MHz		10 10		dBm dBm	
System noise bandwidth	9.6		307.2	kHz	Channel filter 6 dB bandwidth is programmable from 9.6 kHz to 307.2 kHz. See page 26 for details.
Noise figure, cascaded 433/868 MHz		5		dB	
Input IP3 Out-of-band (+10/20 MHz), 434 MHz 12.5 kHz channel width		-23 -18 -16		dBm dBm dBm	LNA2 maximum gain LNA2 medium gain LNA2 minimum gain
Out-of-band (+10/20 MHz), 868 MHz 25 kHz channel width		-18 -15 -13		dBm dBm dBm	LNA2 maximum gain LNA2 medium gain LNA2 minimum gain
Co-channel rejection, FSK/ASK 12.5 kHz channel width, 433 MHz 25 kHz channel width, 868 MHz		-11 -11		dB dB	Wanted signal 3 dB above the sensitivity level, FM jammer (1 kHz sine, ± 2.5 kHz deviation) at operating frequency, $BER = 10^{-3}$

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Adjacent channel rejection (ACR) 12.5 kHz channel width, 433 MHz 25 kHz channel width, 868 MHz		30 32		dB dB	Wanted signal 3 dB above the sensitivity level, FM jammer (1 kHz sine, ± 2.5 kHz deviation) at adjacent channel, BER = 10^{-3}
Image channel rejection 433/868 MHz No I/Q gain and phase calibration I/Q gain and phase calibrated		26/31 49/52		dB dB	Wanted signal 3 dB above the sensitivity level, CW jammer at image frequency, BER = 10^{-3} .
Selectivity* 12.5 kHz channel width, 433 MHz 25 kHz channel width, 868 MHz (*Close-in spurious response rejection)		41 39		dB dB	Wanted signal 3 dB above the sensitivity level. CW jammer is swept in 12.5 kHz/25 kHz steps within ± 1 MHz from wanted channel. BER = 10^{-3} . Adjacent channel and image channel are excluded.
Blocking / Desensitization* 433/868 MHz ± 1 MHz ± 2 MHz ± 5 MHz ± 10 MHz (*Out-of-band spurious response rejection)		50/60 64/71 64/71 75/78		dB dB dB dB	Wanted signal 3 dB above the sensitivity level, CW jammer at $\pm 1, 2, 5$ and 10 MHz offset, BER = 10^{-3} . Complying with EN 300 220, class 2 receiver requirements.
Image frequency suppression, 433/868 MHz No I/Q gain and phase calibration I/Q gain and phase calibrated		36/41 59/62		dB dB	Ratio between sensitivity for a signal at the image frequency to the sensitivity in the wanted channel. Image frequency is RF – 2 IF. The signal source is a 2.4 kBaud, Manchester coded data, ± 2.0 kHz frequency deviation, signal level for BER = 10^{-3}
Spurious reception			40	dB	Ratio between sensitivity for an unwanted frequency to the sensitivity in the wanted channel. The signal source is a 2.4 kBaud, Manchester coded data, ± 2.0 kHz frequency deviation, swept over all frequencies 100 MHz – 2 GHz. Signal level for BER = 10^{-3}
Intermodulation rejection 12.5 kHz channel width 25 kHz channel width		TBD TBD		dB dB	Wanted signal 3 dB above the sensitivity level, two CW jammers at +2Ch and +4Ch where Ch is channel width 12.5 kHz or 25 kHz, BER = 10^{-2}
LO leakage			-47	dBm	LO is at 1608 – 1880 MHz
Spurious emission 9 kHz – 1 GHz 1 – 4 GHz			-57 -47	dBm dBm	Complying with EN 300 220, FCC CFR47 part 15 and ARIB STD T-67.
Input impedance 434 MHz 868 MHz		58 - j10 54 - j22		Ω Ω	Receive mode, series equivalent For matching details see "Input/output matching" on page 53.
Matched input impedance, S11 434 MHz 868 MHz		-14 -12		dB dB	Using application circuit matching network. For details see "Input/output matching" on page 53.

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Matched input impedance 433 MHz 868 MHz		39 - j14 32 - j10		Ω Ω	Using application circuit matching network. For details see "Input/output matching" on page 53.
Bit synchronization offset			0.8	%	The maximum bit rate offset tolerated by the bit synchronization circuit for 6 dB degradation (synchronous modes only)
Data latency NRZ, UART mode Manchester mode		4 8		Baud Baud	Time from clocking the data on the transmitter DIO pin until data is available on receiver DIO pin
RSSI / Carrier Sense					
Carrier sense programmable range		40		dB	Accuracy is as for RSSI, see below.
Adjacent channel carrier sense rejection 12.5 kHz channel width 25 kHz channel width		38 38		dB dB	At carrier sense level -110 dBm, FM jammer (1 kHz sine, ± 2.5 kHz deviation) at adjacent channel
Spurious carrier sense rejection		40		dB	At carrier sense level -110 dBm, 100 MHz – 2 GHz. Adjacent channel and image channel are excluded.
RSSI dynamic range		63		dB	12.5 and 25 kHz channel width
RSSI accuracy		± 3		dB	See page 32 for details
RSSI linearity		± 1		dB	
RSSI attach time 2.4 kBaud, 12.5 kHz channel width 4.8 kBaud, 25 kHz channel width 153.6 kBaud, 500 kHz channel width		3.8 1.9 140		ms ms μ s	Shorter RSSI attach times can be traded for lower RSSI accuracy. See page 36 for more details. Shorter RSSI attach time can also be traded for reduced sensitivity and selectivity by increasing the receiver channel bandwidth.
IF Section					
Intermediate frequency (IF)		307.2		kHz	See "IF frequency" on page 27 for more details.
Digital channel filter bandwidth	9.6		307.2	kHz	Channel filter 6 dB bandwidth is programmable from 9.6 kHz to 307.2 kHz. See page 26 for details.
AFC resolution		150		Hz	At 2.4 kBaud Given as Baud rate/16. See page 30 for more details.

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Frequency Synthesizer Section					
Crystal Oscillator Frequency	4.9152		19.6608	MHz	Recommended frequency is 14.7456 MHz. See page 52 for details.
Reference frequency accuracy requirement		+/- 5.7 +/- 2.8		ppm ppm	433 MHz (EN 300 220) 868 MHz (EN 300 220) Must be less than $\pm 5.7 / \pm 2.8$ ppm to comply with EN 300 220 25 kHz channel width at 433/868 MHz.
		+/- 4		ppm	Must be less than ± 4 ppm to comply with Japanese 12.5 kHz channel width regulations (ARIB STD T-67). NOTE: The reference frequency accuracy (initial tolerance) and drift (aging and temperature dependency) will determine the frequency accuracy of the transmitted signal. Crystal oscillator temperature compensation can be done using the fine step PLL frequency programmability and the AFC feature, see page 41.
Crystal operation		Parallel			C4 and C5 are loading capacitors, see page 52
Crystal load capacitance	12	22	30	pF	4-6 MHz, 22 pF recommended
	12	16	30	pF	6-8 MHz, 16 pF recommended
	12	16	16	pF	8-20 MHz, 16 pF recommended
Crystal oscillator start-up time		1.55		ms	4.9152 MHz, 12 pF load
		1.0		ms	7.3728 MHz, 12 pF load
		0.90		ms	9.8304 MHz, 12 pF load
		0.95		ms	14.7456 MHz, 16 pF load
		0.60		ms	17.2032 MHz, 12 pF load
		0.63		ms	19.6608 MHz, 12 pF load
External clock signal drive, sine wave		300		mVpp	The external clock signal must be connected to XOSC_Q1 using a DC block (10 nF). Set XOSC_BYPASS = 0 in the INTERFACE register when using an external clock signal with low amplitude or a crystal. A full-swing digital external clock can also be used, with no DC block capacitor. In that case, set XOSC_BYPASS = 1. See page 52 for further details.

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Phase noise, 402 – 470 MHz 12.5 kHz channel width		-90 -95 -100 -107 -112		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz	Unmodulated carrier At 12.5 kHz offset from carrier At 25 kHz offset from carrier At 50 kHz offset from carrier At 100 kHz offset from carrier At 1 MHz offset from carrier Measured using loop filter components given in Table 3. The phase noise will be higher for larger PLL loop filter bandwidth.
Phase noise, 804 - 940 MHz 25 kHz channel width		-85 -95 -101 -109 -125		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz	Unmodulated carrier At 12.5 kHz offset from carrier At 25 kHz offset from carrier At 50 kHz offset from carrier At 100 kHz offset from carrier At 1 MHz offset from carrier Measured using loop filter components given in Table 3. The phase noise will be higher for larger PLL loop filter bandwidth.
PLL loop bandwidth 12.5 kHz channel width, 433 MHz 25 kHz channel width, 868 MHz		2.7 8.3		kHz kHz	After PLL and VCO calibration. The PLL loop bandwidth is programmable.
PLL lock time (RX / TX turn time) 12.5 kHz channel width, 433 MHz 25 kHz channel width, 868 MHz 500 kHz channel width		900 640 14		us us us	307.2 kHz frequency step to RF frequency within $\pm 10\%$ of channel width. Depends on loop filter component values and <i>PLL_BW</i> register setting. See page 48 for more details.
PLL turn-on time. From power down mode with crystal oscillator running. 12.5 kHz channel width, 433 MHz 25 kHz channel width, 868 MHz 500 kHz channel width		3.2 2.5 700		ms ms us	Time from writing to registers to RF frequency within $\pm 10\%$ of channel width. Depends on loop filter component values and <i>PLL_BW</i> register setting. See page 47 for more details.
Digital Inputs/Outputs					
Logic "0" input voltage	0		0.3* VDD	V	
Logic "1" input voltage	0.7* VDD		VDD	V	
Logic "0" output voltage	0		0.4	V	Output current –2.0 mA, 3.0 V supply voltage
Logic "1" output voltage	2.5		VDD	V	Output current 2.0 mA, 3.0 V supply voltage
Logic "0" input current	NA		–1	μA	Input signal equals GND. PSEL has an internal pull-up resistor and during configuration the current will be –350 μA.
Logic "1" input current	NA		1	μA	Input signal equals VDD
DIO setup time	20			ns	TX mode, minimum time DIO must be ready before the positive edge of DCLK

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
DIO hold time	10			ns	TX mode, minimum time DIO must be held after the positive edge of DCLK
Serial interface (PCLK, PDI, PDO and PSEL) timing specification					See Table 4 on page 20
Pin drive, LNA_EN, PA_EN		0.90 0.87 0.81 0.69		mA mA mA mA	Source current 0 V on LNA_EN, PA_EN pin 0.5 V on LNA_EN, PA_EN pin 1.0 V on LNA_EN, PA_EN pin 1.5 V on LNA_EN, PA_EN pin Sink current 3.0 V on LNA_EN, PA_EN pin 2.5 V on LNA_EN, PA_EN pin 2.0 V on LNA_EN, PA_EN pin 1.5 V on LNA_EN, PA_EN pin See Figure 40 for more details.
Current Consumption					
Power Down mode		0.2	1	μA	Oscillator core off
Current Consumption, receive mode 433/868 MHz		17.3/17.9		mA	25 kHz channel width. Lower current can be achieved at other settings.
Current Consumption, transmit mode 433/868 MHz: P = -20 dBm P = -5 dBm P = 0 dBm P = 5 dBm P = 10 dBm (433 MHz only)		10.3/13.7 12.1/18.1 13.7/21.9 16.8/33 23.7		mA mA mA mA mA	The output power is delivered to a 50 Ω load, see also page 51
Current Consumption, crystal oscillator		77		μA	14.7456 MHz, 16 pF load crystal
Current Consumption, crystal oscillator and bias		500		μA	14.7456 MHz, 16 pF load crystal
Current Consumption, crystal oscillator, bias and synthesizer		11.5		mA	14.7456 MHz, 16 pF load crystal

Pin Assignment

Table 1 shows an overview of the **CC1020** pins.

The package for the **CC1020** is a QFN32 type (see page 80 for details).

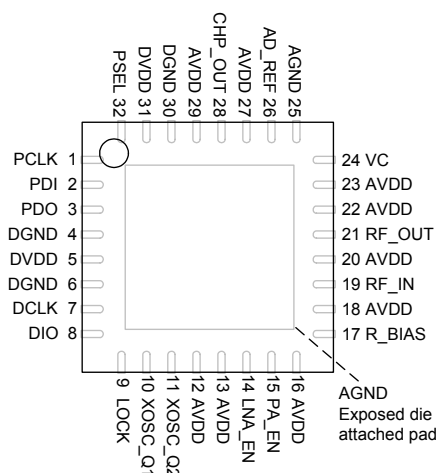


Figure 1. **CC1020** package (top view)

Pin no.	Pin name	Pin type	Description
-	AGND	Ground (analogue)	Exposed die attached pad. Must be soldered to solid ground plane as this is the ground connection for all analogue modules. See page 58 for more details.
1	PCLK	Digital input	Programming clock for SPI configuration interface
2	PDI	Digital input	Programming data input for SPI configuration interface
3	PDO	Digital output	Programming data output for SPI configuration interface
4	DGND	Ground (digital)	Ground connection (0 V) for digital modules and digital I/O
5	DVDD	Power (digital)	Power supply (3 V typical) for digital modules and digital I/O
6	DGND	Ground (digital)	Ground connection (0 V) for digital modules (substrate)
7	DCLK	Digital output	Clock for data in both receive and transmit mode. Can be used as receive data output in asynchronous mode
8	DIO	Digital input/output	Data input in transmit mode; data output in receive mode Can also be used to start power-up sequencing in receive
9	LOCK	Digital output	PLL Lock indicator, active low. Output is asserted (low) when PLL is in lock. The pin can also be used as a general digital output, or as receive data output in synchronous NRZ/Manchester mode
10	XOSC_Q1	Analogue input	Crystal oscillator or external clock input
11	XOSC_Q2	Analogue output	Crystal oscillator
12	AVDD	Power (analogue)	Power supply (3 V typical) for crystal oscillator
13	AVDD	Power (analogue)	Power supply (3 V typical) for the IF VGA
14	LNA_EN	Digital output	General digital output. Can be used for controlling an external LNA, if higher sensitivity is needed.
15	PA_EN	Digital output	General digital output. Can be used for controlling an external PA, if higher output power is needed.
16	AVDD	Power (analogue)	Power supply (3 V typical) for global bias generator and IF anti-alias filter
17	R_BIAS	Analogue output	Connection for external precision bias resistor (82 k Ω , \pm 1%)
18	AVDD	Power (analogue)	Power supply (3 V typical) for LNA input stage
19	RF_IN	RF Input	RF signal input from antenna (external AC-coupling)
20	AVDD	Power (analogue)	Power supply (3 V typical) for LNA
21	RF_OUT	RF output	RF signal output to antenna
22	AVDD	Power (analogue)	Power supply (3 V typical) for LO buffers, mixers, prescaler, and first PA stage
23	AVDD	Power (analogue)	Power supply (3 V typical) for VCO
24	VC	Analogue input	VCO control voltage input from external loop filter
25	AGND	Ground (analogue)	Ground connection (0 V) for analogue modules (guard)

Pin no.	Pin name	Pin type	Description
26	AD_REF	Power (analogue)	3 V reference input for ADC
27	AVDD	Power (analogue)	Power supply (3 V typical) for charge pump and phase detector
28	CHP_OUT	Analogue output	PLL charge pump output to external loop filter
29	AVDD	Power (analogue)	Power supply (3 V typical) for ADC
30	DGND	Ground (digital)	Ground connection (0 V) for digital modules (guard)
31	DVDD	Power (digital)	Power supply connection (3 V typical) for digital modules
32	PSEL	Digital input	Programming chip select, active low, for configuration interface. Internal pull-up resistor.

Table 1. Pin assignment overview**Note:**

DCLK, DIO and LOCK are high-impedance (3-state) in power down (*BIAS_PD* = 1 in the *MAIN* register).

The exposed die attached pad **must** be soldered to solid ground plane as this is the main ground connection for the chip.

Circuit Description

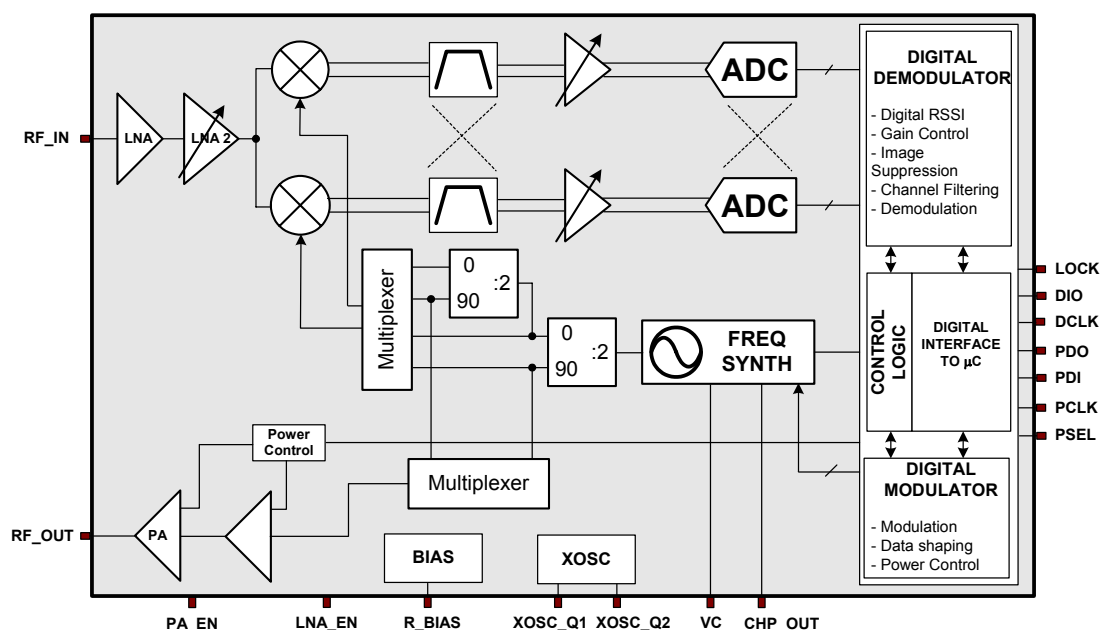


Figure 2. CC1020 simplified block diagram

A simplified block diagram of **CC1020** is shown in Figure 2. Only signal pins are shown.

CC1020 features a low-IF receiver. The received RF signal is amplified by the low-noise amplifier (LNA and LNA2) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF, the I/Q signal is complex filtered and amplified, and then digitized by the ADCs. Automatic gain control, fine channel filtering, demodulation and bit synchronization is performed digitally. **CC1020** outputs the digital demodulated data on the DIO pin. A synchronized data clock is available at the DCLK pin. RSSI is available in digital format and can be read via the serial interface. The RSSI also features a programmable carrier sense indicator.

In transmit mode, the synthesized RF frequency is fed directly to the power amplifier (PA). The RF output is frequency

shift keyed (FSK) by the digital bit stream that is fed to the pin DIO. Optionally, a Gaussian filter can be used to get Gaussian FSK (GFSK). The internal match circuitry makes the antenna interface easy.

The frequency synthesizer includes a completely on-chip LC VCO and a 90 degrees phase splitter for generating the LO_I and LO_Q signals to the down-conversion mixers in receive mode. The VCO operates in the frequency range 1.608-1.880 GHz. The pin CHP_OUT is the charge pump output and $\overline{\text{VC}}$ is the control node of the on-chip VCO. The loop filter is external, and placed between these pins. A crystal is to be connected to XOSC_Q1 and XOSC_Q2. A lock signal is available from the PLL.

The 4-wire SPI serial interface is used for configuration.

Application Circuit

Very few external components are required for the operation of **CC1020**. The recommended application circuit is shown in Figure 3. The external components are described in Table 2 and typical values are given in Table 3.

Input / output matching

L1 and C1 is the input match for the receiver. L1 is also a DC choke for biasing. L2 and C3 are used to match the transmitter to 50 Ω . Internal circuitry makes it possible to connect the input and output together and match the **CC1020** to 50 Ω in both RX and TX mode. However, it is recommended to use an external T/R switch for optimal performance. See "Input/output matching" on page 53 and Application Note *AN022 Crystal Frequency Selection* for more details. Component values for the matching network are easily calculated using the SmartRF® Studio software.

Bias resistor

The precision bias resistor R1 is used to set an accurate bias current.

PLL loop filter

The loop filter consists of two resistors (R2 and R3) and three capacitors (C6-C8). C7 and C8 may be omitted in applications

where high loop bandwidth is desired. The values shown in Table 3 can be used for data rates up to 4.8 kBaud. Component values for higher data rates are easily calculated using the SmartRF® Studio software.

Crystal

An external crystal with two loading capacitors (C4 and C5) is used for the crystal oscillator. See page 52 for details.

Additional filtering

Additional external components (e.g. RF LC or SAW filter) may be used in order to improve the performance in specific applications. See also "Optional LC filter" on page 55 for further information.

Power supply decoupling and filtering

Power supply decoupling and filtering must be used (not shown in the application circuit). The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the optimum performance for narrowband applications. Chipcon provides a reference design that should be followed very closely.

Ref	Description
C1	LNA input match and DC block, see page 53
C3	PA output match and DC block, see page 53
C4	Crystal load capacitor, see page 52
C5	Crystal load capacitor, see page 52
C6	PLL loop filter capacitor
C7	PLL loop filter capacitor (may be omitted for highest loop bandwidth)
C8	PLL loop filter capacitor (may be omitted for highest loop bandwidth)
L1	LNA match and DC bias (ground), see page 53
L2	PA match and DC bias (supply voltage), see page 53
R1	Precision resistor for current reference generator
R2	PLL loop filter resistor
R3	PLL loop filter resistor
XTAL	Crystal, see page 52

Table 2. Overview of external components (excluding supply decoupling capacitors)

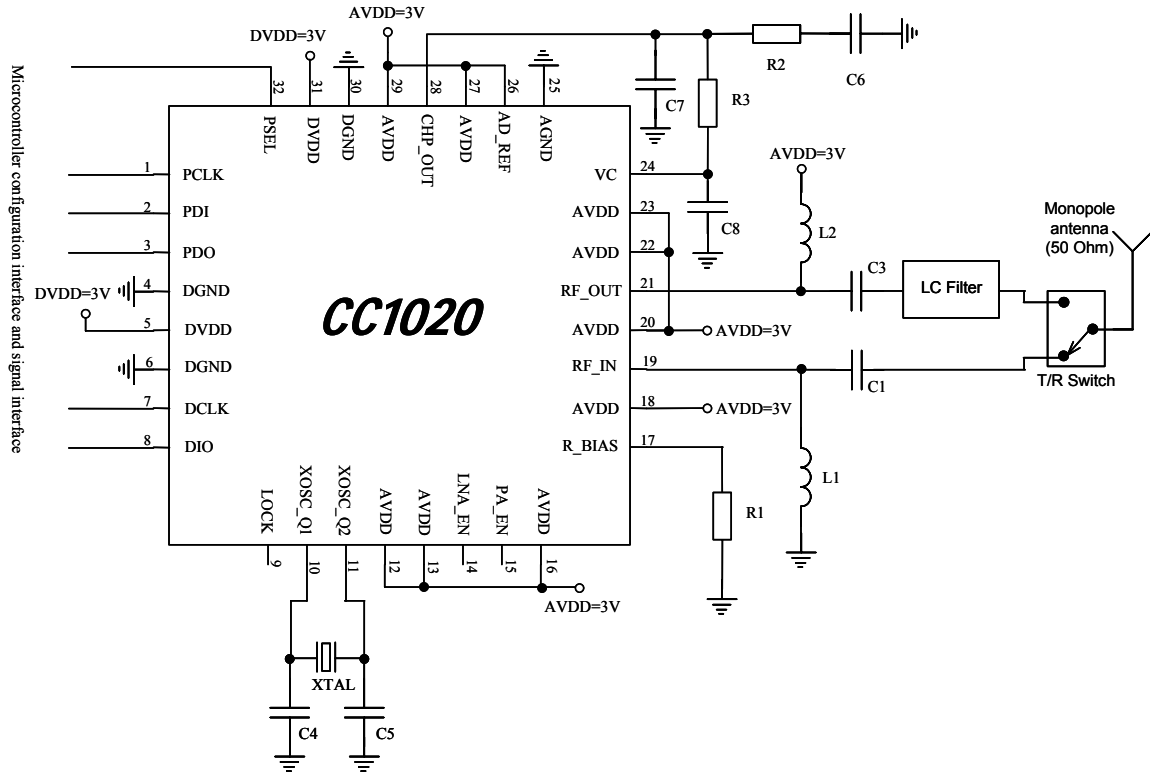


Figure 3. Typical application and test circuit (power supply decoupling not shown)

Item	433 MHz	868 MHz	915 MHz
C1	10 pF, 5%, C0G, 0603	10 pF, 5%, C0G, 0603	10 pF, 5%, C0G, 0603
C3	3.9 pF, 5%, C0G, 0603	10 pF, 5%, C0G, 0603	10 pF, 5%, C0G, 0603
C4	18 pF, 5%, C0G, 0603	18 pF, 5%, C0G, 0603	18 pF, 5%, C0G, 0603
C5	18 pF, 5%, C0G, 0603	18 pF, 5%, C0G, 0603	18 pF, 5%, C0G, 0603
C6	220 nF, 10%, X7R, 0603	100 nF, 10%, X7R, 0603	100 nF, 10%, X7R, 0603
C7	8.2 nF, 10%, X7R, 0603	3.9 nF, 10%, X7R, 0603	3.9 nF, 10%, X7R, 0603
C8	2.2 nF, 10%, X7R, 0603	1.0 nF, 10%, X7R, 0603	1.0 nF, 10%, X7R, 0603
L1	33 nH, 5%, 0603 (Coilcraft 0603CS-33NXJBC)	18 nH, 5%, 0603 (Coilcraft 0603CS-18NXJBC)	18 nH, 5%, 0603 (Coilcraft 0603CS-18NXJBC)
L2	15 nH, 5%, 0603 (Coilcraft 0603CS-15NXJBC)	3.6 nH, 5%, 0603 (Coilcraft 0603CS-3N6XJBC)	3.6 nH, 5%, 0603 (Coilcraft 0603CS-3N6XJBC)
R1	82 kΩ, 1%, 0603	82 kΩ, 1%, 0603	82 kΩ, 1%, 0603
R2	1.5 kΩ, 5%, 0603	2.2 kΩ, 5%, 0603	2.2 kΩ, 5%, 0603
R3	4.7 kΩ, 5%, 0603	6.8 kΩ, 5%, 0603	6.8 kΩ, 5%, 0603
XTAL	14.7456 MHz crystal, 16 pF load	14.7456 MHz crystal, 16 pF load	14.7456 MHz crystal, 16 pF load

Note: Items shaded are different for different frequencies. For 433 MHz, a loop filter with lower bandwidth is used to improve adjacent and alternate channel rejection for 12.5 kHz channels.

Table 3. Bill of materials for the application circuit in Figure 3

Note:

The PLL loop filter component values in Table 3 (R2, R3, C6-C8) can be used for data rates up to 4.8 kBaud. The SmartRF®

Studio software provides component values for other data rates using the equations on page 44.

Configuration Overview

CC1020 can be configured to achieve the best performance for different applications. Through the programmable configuration registers the following key parameters can be programmed:

- Receive / transmit mode
- RF output power
- Frequency synthesizer key parameters:
RF output frequency, FSK frequency

deviation, crystal oscillator reference frequency

- Power-down / power-up mode
- Crystal oscillator power-up / power down
- Data rate and data format (NRZ, Manchester coded or UART interface)
- Synthesizer lock indicator mode
- Digital RSSI and carrier sense
- FSK / GFSK / OOK (ASK) modulation

Configuration Software

Chipcon provides users of **CC1020** with a software program, SmartRF® Studio (Windows interface) that generates all necessary **CC1020** configuration data based on the user's selections of various parameters. These hexadecimal numbers will then be the necessary input to the microcontroller for the configuration of **CC1020**. In addition, the program will

provide the user with the component values needed for the input/output matching circuit, the PLL loop filter and the optional LC filter.

Figure 4 shows the user interface of the **CC1020** configuration software.

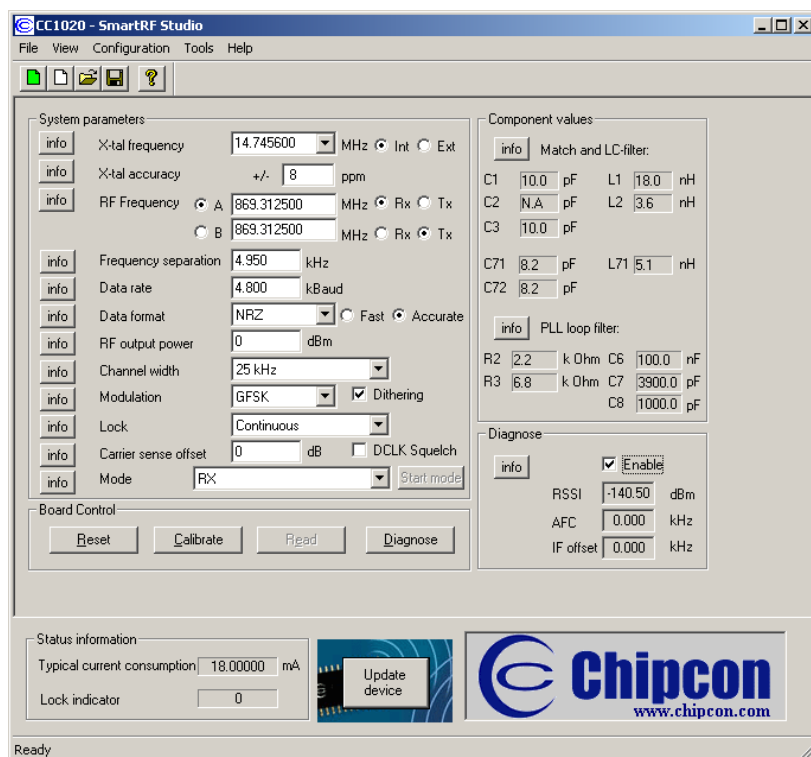


Figure 4. SmartRF® Studio user interface

Microcontroller Interface

Used in a typical system, **CC1020** will interface to a microcontroller. This microcontroller must be able to:

- Program **CC1020** into different modes via the 4-wire serial configuration interface (PDI, PDO, PCLK and PSEL)
- Interface to the bi-directional synchronous data signal interface (DIO and DCLK)
- Optionally, the microcontroller can do data encoding / decoding
- Optionally, the microcontroller can monitor the LOCK pin for frequency lock status, carrier sense status or other status information.
- Optionally, the microcontroller can read back digital RSSI value and other status information via the 4-wire serial interface

Configuration interface

The microcontroller interface is shown in Figure 5. The microcontroller uses 3 or 4 I/O pins for the configuration interface (PDI, PDO, PCLK and PSEL). PDO should be connected to an input at the microcontroller. PDI, PCLK and PSEL must be microcontroller outputs. One I/O pin can be saved if PDI and PDO are connected together and a bi-directional pin is used at the microcontroller.

The microcontroller pins connected to PDI, PDO and PCLK can be used for other

purposes when the configuration interface is not used. PDI, PDO and PCLK are high impedance inputs as long as PSEL is not activated (active low).

PSEL has an internal pull-up resistor and should be left open (tri-stated by the microcontroller) or set to a high level during power down mode in order to prevent a trickle current flowing in the pull-up.

Signal interface

A bi-directional pin is usually used for data (DIO) to be transmitted and data received. DCLK providing the data timing should be connected to a microcontroller input.

As an option, the data output in receive mode can be made available on a separate pin. See for page 21 more details.

PLL lock signal

Optionally, one microcontroller pin can be used to monitor the LOCK signal. This signal is at low logic level when the PLL is in lock. It can also be used for carrier sense and to monitor other internal test signals.

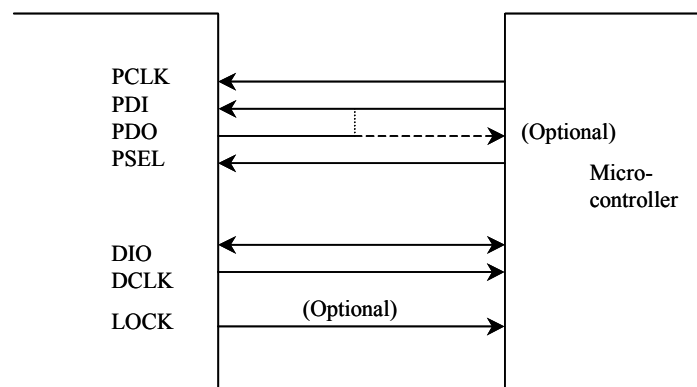


Figure 5. Microcontroller interface

4-wire Serial Configuration Interface

CC1020 is configured via a simple 4-wire SPI-compatible interface (PDI, PDO, PCLK and PSEL). There are 8-bit configuration registers, each addressed by a 7-bit address. A Read/Write bit initiates a read or write operation. A full configuration of **CC1020** requires sending 33 data frames of 16 bits each (7 address bits, R/W bit and 8 data bits). The time needed for a full configuration depends on the PCLK frequency. With a PCLK frequency of 10 MHz the full configuration is done in less than 53 μ s. Setting the device in power down mode requires sending one frame only and will in this case take less than 2 μ s. All registers are also readable.

In each write-cycle, 16 bits are sent on the PDI-line. The seven most significant bits of each data frame (A6:0) are the address-bits. A6 is the MSB (Most Significant Bit) of the address and is sent as the first bit. The next bit is the R/W bit (high for write, low for read). The 8 data-bits are then transferred (D7:0). During address and data transfer the PSEL (Program SElect) must be kept low. See Figure 6.

The timing for the programming is also shown in Figure 6 with reference to Table

4. The clocking of the data on PDI is done on the positive edge of PCLK. When the last bit, D0, of the 8 data-bits has been loaded, the data word is loaded in the internal configuration register.

The configuration data will be retained during a programmed power-down mode, but not when the power-supply is turned off. The registers can be programmed in any order.

The configuration registers can also be read by the microcontroller via the same configuration interface. The seven address bits are sent first, then the R/W bit set low to initiate the data read-back. **CC1020** then returns the data from the addressed register. PDO is used as the data output and must be configured as an input by the microcontroller. The PDO is set at the negative edge of PCLK and should be sampled at the positive edge. The read operation is illustrated in Figure 7.

PSEL must be set high between each read/write operation.

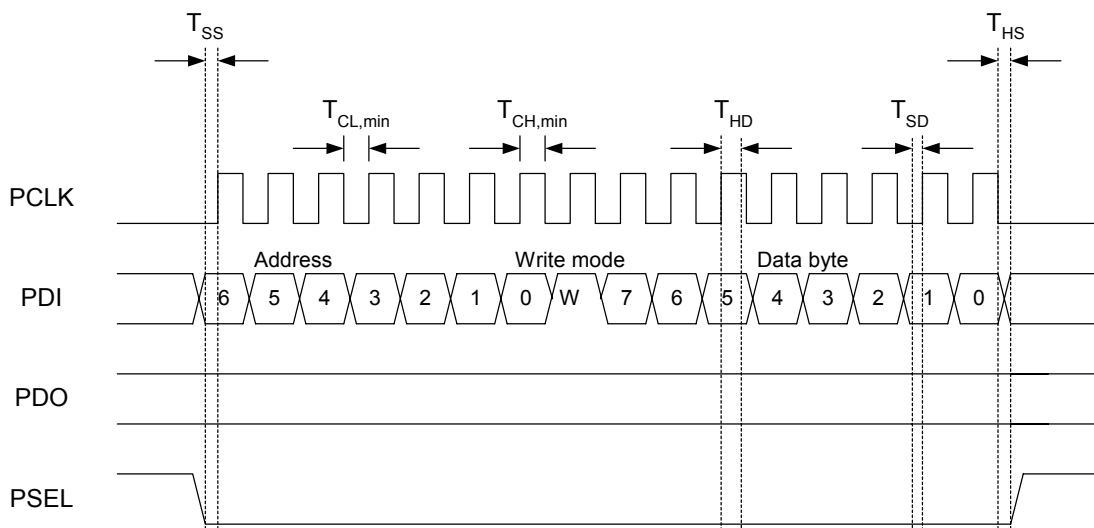


Figure 6. Configuration registers write operation

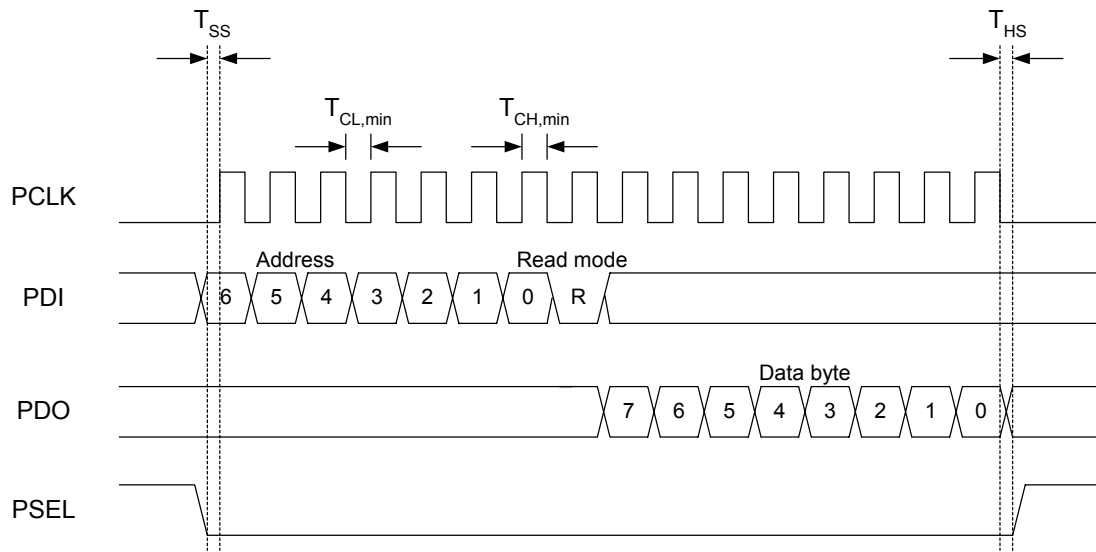


Figure 7. Configuration registers read operation

Parameter	Symbol	Min	Max	Units	Conditions
PCLK, clock frequency	F_{PCLK}		10	MHz	
PCLK low pulse duration	$T_{CL,min}$	50		ns	The minimum time PCLK must be low.
PCLK high pulse duration	$T_{CH,min}$	50		ns	The minimum time PCLK must be high.
PSEL setup time	T_{SS}	10		ns	The minimum time PSEL must be low before <i>positive</i> edge of PCLK.
PSEL hold time	T_{HS}	10		ns	The minimum time PSEL must be held low after the <i>negative</i> edge of PCLK.
PDI setup time	T_{SD}	10		ns	The minimum time data on PDI must be ready before the <i>positive</i> edge of PCLK.
PDI hold time	T_{HD}	10		ns	The minimum time data must be held at PDI, after the <i>positive</i> edge of PCLK.
Rise time	T_{rise}		100	ns	The maximum rise time for PCLK and PSEL
Fall time	T_{fall}		100	ns	The maximum fall time for PCLK and PSEL

Note: The set-up- and hold-times refer to 50% of VDD.

Table 4. Serial interface, timing specification

Signal Interface

The **CC1020** can be used with NRZ (Non-Return-to-Zero) data or Manchester (also known as bi-phase-level) encoded data. **CC1020** can also synchronize the data from the demodulator and provide the data clock at DCLK. The data format is controlled by the **DATA_FORMAT[1:0]** bits in the **MODEM** register.

CC1020 can be configured for three different data formats:

Synchronous NRZ mode

In transmit mode **CC1020** provides the data clock at DCLK and DIO is used as data input. Data is clocked into **CC1020** at the rising edge of DCLK. The data is modulated at RF without encoding.

In receive mode **CC1020** does the synchronization and provides received data clock at DCLK and data at DIO. The data should be clocked into the interfacing circuit at the rising edge of DCLK. See Figure 8.

Synchronous Manchester encoded mode

In transmit mode **CC1020** provides the data clock at DCLK and DIO is used as data input. Data is clocked into **CC1020** at the rising edge of DCLK and should be in NRZ format. The data is modulated at RF with Manchester code. The encoding is done by **CC1020**. In this mode the effective bit rate is half the baud rate due to the coding.

In receive mode **CC1020** does the synchronization and provides received data clock at DCLK and data at DIO. **CC1020** does the decoding and NRZ data is presented at DIO. The data should be clocked into the interfacing circuit at the rising edge of DCLK. See Figure 9.

In synchronous NRZ or Manchester mode the DCLK signal runs continuously both in RX and TX unless the DCLK signal is gated with the carrier sense signal or the PLL lock signal. Refer to page 37 for more details.

If **SEP_DI_DO** = 0 in the **INTERFACE** register, the DIO pin is the data output in receive mode and data input in transmit mode.

As an option, the data output can be made available at a separate pin. This is done by setting **SEP_DI_DO** = 1 in the **INTERFACE** register. Then, the LOCK pin will be used as data output in synchronous mode, overriding other use of the LOCK pin.

Transparent Asynchronous UART mode

In transmit mode DIO is used as data input. The data is modulated at RF without synchronization or encoding.

In receive mode the raw data signal from the demodulator is sent to the output (DIO). No synchronization or decoding of the signal is done in **CC1020** and should be done by the interfacing circuit.

If **SEP_DI_DO** = 0 in the **INTERFACE** register, the DIO pin is the data output in receive mode and data input in transmit mode. The DCLK pin is not active and can be set to a high or low level by **DATA_FORMAT[0]**.

If **SEP_DI_DO** = 1 in the **INTERFACE** register, the DCLK pin is the data output in receive mode and the DIO pin is the data input in transmit mode. In TX mode the DCLK pin is not active and can be set to a high or low level by **DATA_FORMAT[0]**. See Figure 10.

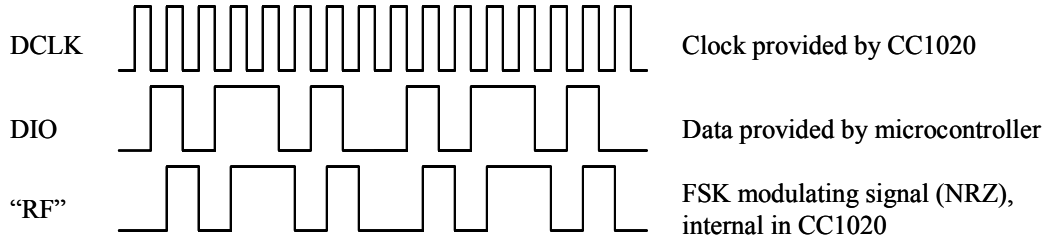
Manchester encoding and decoding

In the *Synchronous Manchester encoded mode* **CC1020** uses Manchester coding when modulating the data. The **CC1020** also performs the data decoding and synchronization. The Manchester code is based on transitions; a "0" is encoded as a low-to-high transition, a "1" is encoded as a high-to-low transition. See Figure 11.

The Manchester code ensures that the signal has a constant DC component, which is necessary in some FSK demodulators. Using this mode also

ensures compatibility with CC400/CC900 | designs.

Transmitter side:



Receiver side:

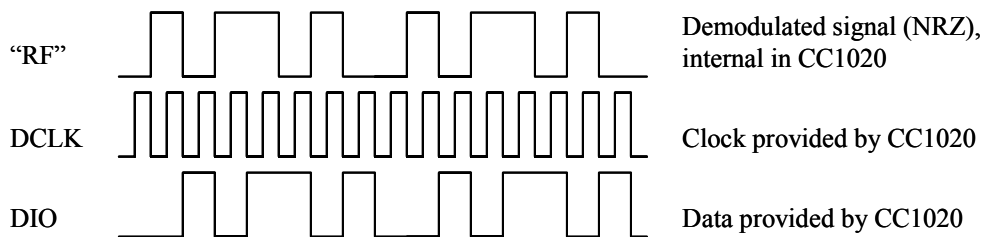
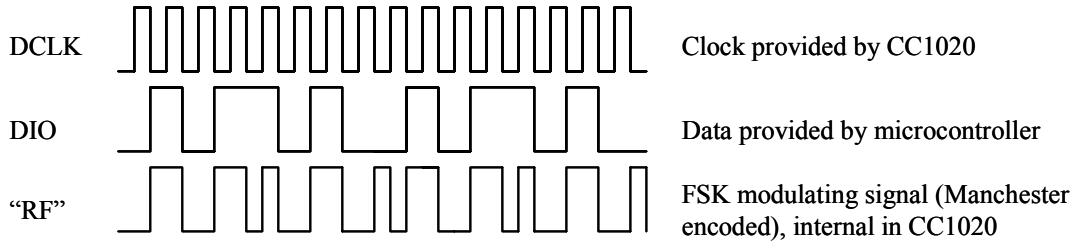


Figure 8. Synchronous NRZ mode

Transmitter side:



Receiver side:

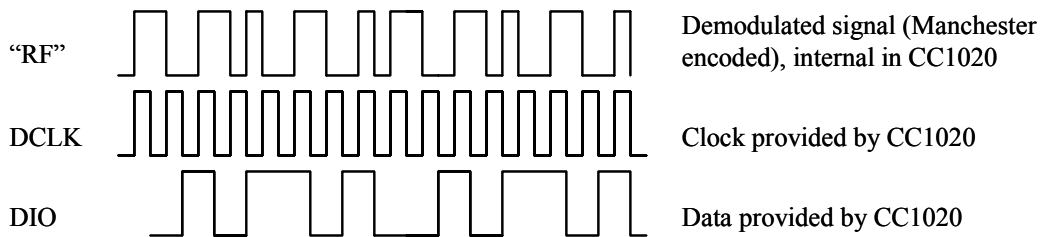


Figure 9. Synchronous Manchester encoded mode

Transmitter side:

DCLK

DIO

“RF”

DCLK is not used in transmit mode, and is used as data output in receive mode. It can be set to default high or low in transmit mode.

Data provided by UART (TXD)

FSK modulating signal, internal in CC1020

Receiver side:

“RF”

DCLK

DIO

Demodulated signal (NRZ), internal in CC1020

DCLK is used as data output provided by CC1020. Connect to UART (RXD)

DIO is not used in receive mode. Used only as data input in transmit mode

Figure 10. Transparent Asynchronous UART mode (*SEP_DI_DO* = 1)

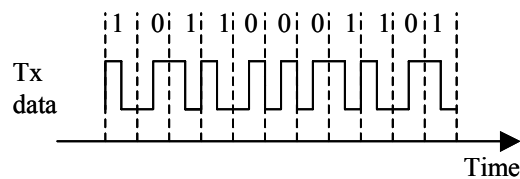


Figure 11. Manchester encoding

Built-in Test Pattern Generator

The **CC1020** has a built-in test pattern generator that generates a PN9 pseudo random sequence. The *PN9_ENABLE* bit in the *MODEM* register enables the PN9 generator. A transition on the DIO pin is required after enabling the PN9 pseudo random sequence.

The PN9 pseudo random sequence is defined by the polynomial $x^9 + x^5 + 1$.

The PN9 sequence is ‘XOR’ed with the DIO signal in both TX and RX mode as shown in Figure 12. Hence, by transmitting only zeros (DIO = 0), the BER (Bit Error Rate) can be tested by counting the

number of received ones. Note that the 9 first received bits should be discarded in this case. Also note that one bit error will generate 3 received ones.

Transmitting only ones (DIO = 1), the BER can be tested by counting the number of received zeroes.

The PN9 generator can also be used for transmission of ‘real-life’ data when measuring narrowband ACP (Adjacent Channel Power), modulation bandwidth or occupied bandwidth.

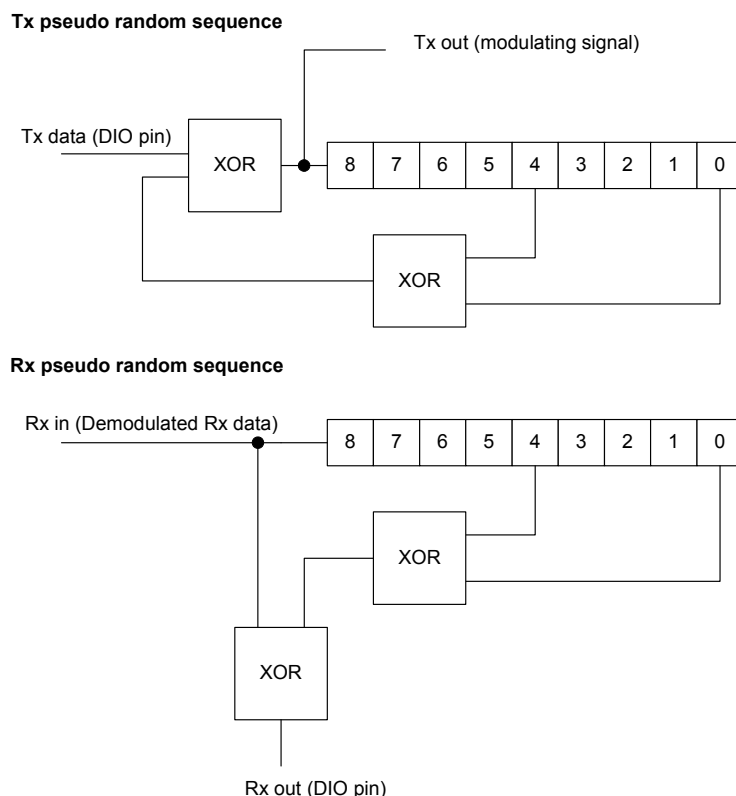


Figure 12. PN9 pseudo random sequence generator in Tx and Rx mode

FSK Modulation Formats

The data modulator can modulate FSK, which is a two level FSK (Frequency Shift Keying), or GFSK, which is a Gaussian filtered FSK with $BT = 0.5$. The purpose of the GFSK is to make a more bandwidth efficient system as shown in Figure 13. The modulation and the Gaussian filtering are done internally in the chip. The

TX_SHAPING bit in the *DEVIATION* register enables the GFSK. GFSK is recommended for narrowband operation.

Figure 14 and Figure 15 show typical eye diagrams for 433 MHz and 868 MHz operation respectively.

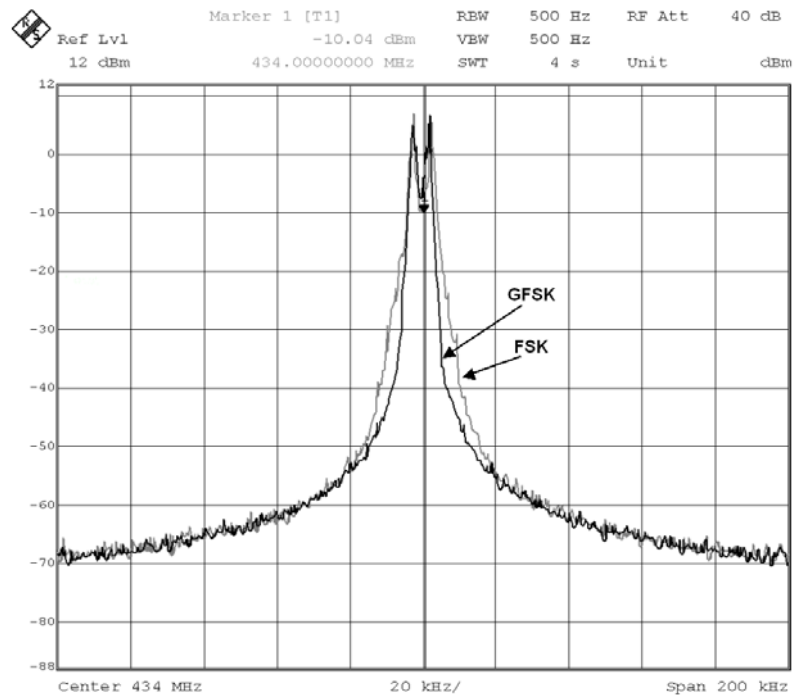


Figure 13. FSK vs. GFSK spectrum plot. 2.4 kBaud, NRZ, ± 2.4 kHz frequency deviation.

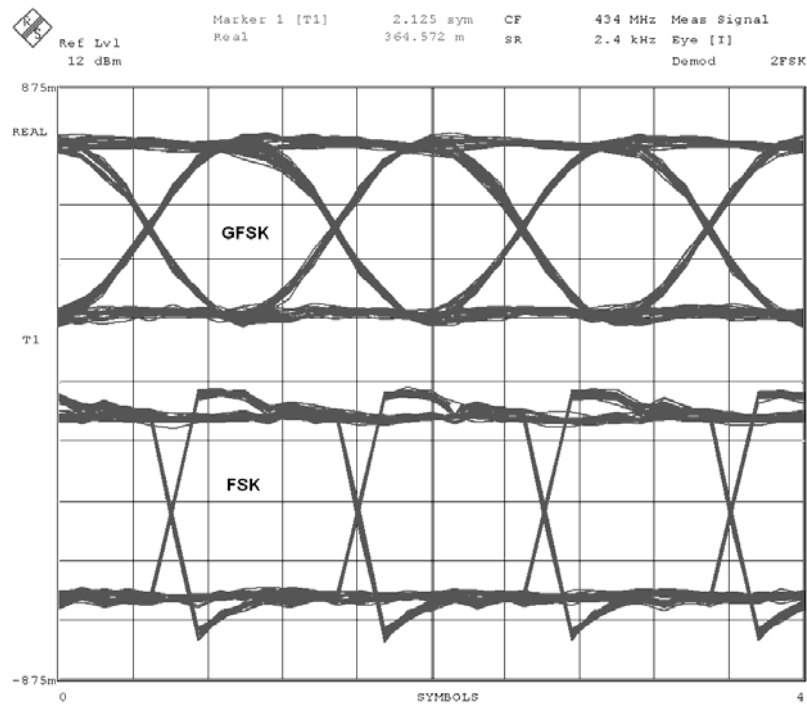


Figure 14. FSK vs. GFSK eye diagram. 2.4 kBaud, NRZ, ± 2.4 kHz frequency deviation.

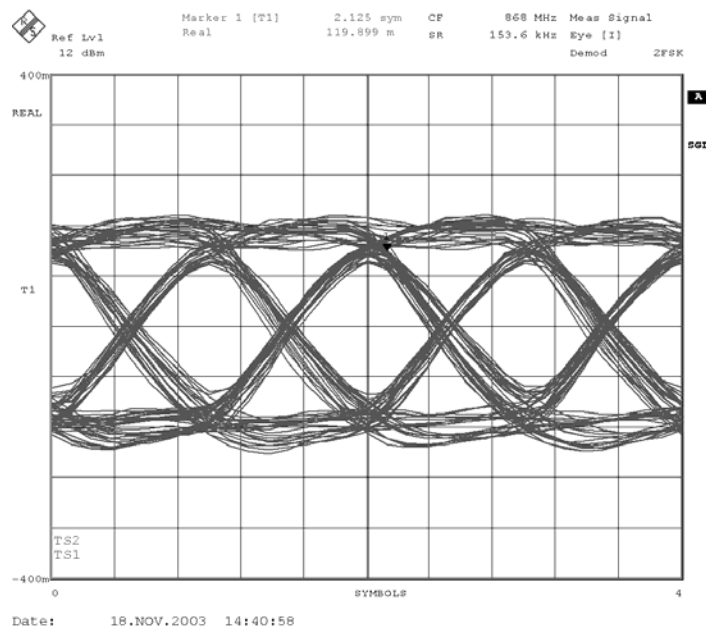


Figure 15. GFSK eye diagram. 153.6 kBaud, NRZ, ± 76.8 kHz frequency deviation.

OOK/ASK Modulation

The data modulator can also do OOK (On-Off Keying) modulation. OOK is an ASK (Amplitude Shift Keying) modulation using 100% modulation depth. OOK modulation is enabled in RX and in TX by setting `TXDEV_M[3:0] = 0000` in the `DEVIATION`

register. An OOK eye diagram is shown in Figure 16.

The automatic frequency control (AFC) cannot be used when receiving OOK/ASK, as it requires a frequency shift.

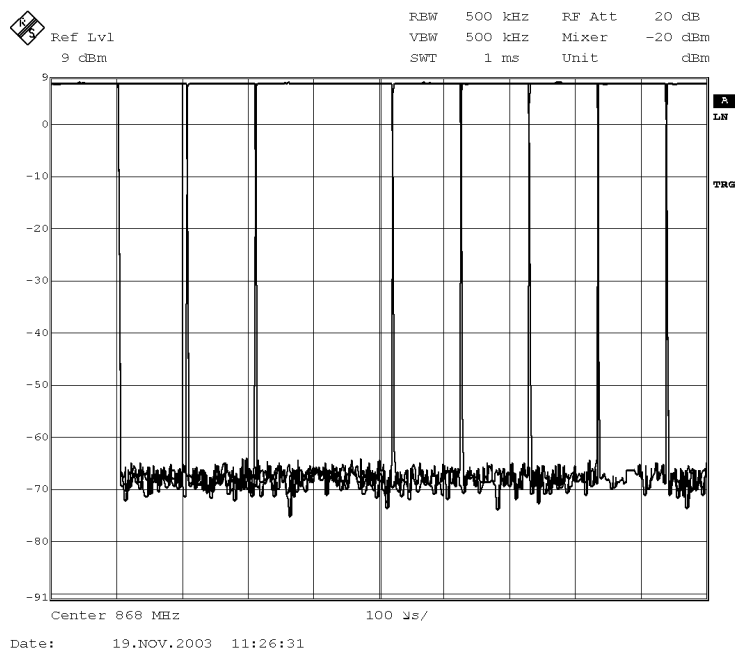


Figure 16. OOK eye diagram. 9.6 kBaud.

Receiver Channel Bandwidth

In order to meet different channel width requirements, the receiver channel filter bandwidth is programmable. It can be programmed from 9.6 to 307.2 kHz.

The *DEC_DIV[4:0]* bits in the *FILTER* register control the bandwidth. The 6 dB bandwidth is given by:

$$\text{ChBW} = 307.2 / (\text{DEC_DIV} + 1) \text{ [kHz]}$$

where the IF frequency is set to 307.2 kHz (see next section). The table below shows the recommended setting for some commonly used channel widths (FSK/GFSK data modulation).

Channel width [kHz]	Filter bandwidth [kHz]	FILTER.DEC_DIV [4:0] [decimal(binary)]
12.5	12.288	24 (11000b)
25	19.2	15 (01111b)
50	25.6	11 (01011b)
100	51.2	5 (00101b)
150	102.4	2 (00010b)
200	153.6	1 (00001b)
500	307.2	0 (00000b)

There is a tradeoff between selectivity as well as sensitivity and accepted frequency tolerance. In applications where larger frequency drift is expected, the filter bandwidth can be increased, but with reduced adjacent channel rejection (ACR).

IF Frequency

The IF frequency is derived from the crystal frequency as

$$f_{IF} = \frac{f_{xosc}}{8 \cdot (\text{ADC_DIV}[2:0] + 1)}$$

where *ADC_DIV[2:0]* is set in the *MODEM* register.

The analogue filter preceding the mixer is used for wide-band and anti-alias filtering which is important for the blocking performance at 1 MHz and larger offsets. This filter is fixed and centred on the nominal IF frequency of 307.2 kHz. The bandwidth of the analogue filter is about 160 kHz.

Using crystal frequencies which gives an IF frequency within 300 – 320 kHz means that the analogue filter can be used (assuming low frequency deviations and low data rates).

Large offsets, however, from the nominal IF frequency will give an un-symmetric filtering (variation in group delay and different attenuation) of the signal, resulting in decreased sensitivity and selectivity. See Application Note *AN022 Crystal Frequency Selection* for more details.

For other than 300 – 320 kHz IF frequencies (and for high frequency deviation and high data rates) the analogue filter must be bypassed by setting *FILTER_BYPASS* = 1 in the *FILTER* register.

The IF frequency is always the ADC clock frequency divided by 4. The ADC clock frequency should therefore be as close to 1.2288 MHz as possible.

Data Rate Programming

The data rate (baud rate) is programmable and depends on the crystal frequency and the programming of the *CLOCK* (*CLOCK_A* and *CLOCK_B*) registers.

The baud rate (B.R) is given by

$$B.R. = \frac{f_{xosc}}{8 \cdot (\text{REF_DIV} + 1) \cdot \text{DIV1} \cdot \text{DIV2}}$$

where DIV1 and DIV2 are given by the value of *MCLK_DIV1* and *MCLK_DIV2*.

Table 5 below shows some possible data rates as a function of crystal frequency in synchronous mode. In asynchronous transparent UART mode any data rate up to 153.6 kBaud can be used.

MCLK_DIV2[1:0]	DIV2
00	1
01	2
10	4
11	8

MCLK_DIV1[2:0]	DIV1
000	2.5
001	3
010	4
011	7.5
100	12.5
101	40
110	48
111	64

Data rate [kBaud]	Crystal frequency [MHz]						
	4.9152	7.3728	9.8304	12.288	14.7456	17.2032	19.6608
0.45		X			X		
0.5				X			
0.6	X	X	X	X	X	X	X
0.9		X			X		
1				X			
1.2	X	X	X	X		X	X
1.8		X			X		
2				X			
2.4	X	X	X	X	X	X	X
3.6		X			X		
4				X			
4.096			X				X
4.8	X	X	X	X	X	X	X
7.2		X			X		
8				X			
8.192			X				X
9.6	X	X	X	X	X	X	X
14.4		X			X		
16				X			
16.384			X				X
19.2	X	X	X	X	X	X	X
28.8		X			X		
32				X			
32.768			X				X
38.4	X	X	X	X	X	X	X
57.6		X			X		
64				X			
65.536							X
76.8	X	X	X	X	X	X	X
115.2		X			X		
128				X			
153.6		X		X	X	X	X

Table 5: Some possible data rates versus crystal frequency

Demodulator, Bit Synchronizer and Data Decision

The block diagram for the demodulator, data slicer and bit synchronizer is shown in Figure 17. The built-in bit synchronizer synchronizes the internal clock to the incoming data and performs data decoding. The data decision is done using over-sampling and digital filtering of the incoming signal. This improves the reliability of the data transmission. Using the synchronous modes simplifies the data-decoding task substantially.

The suggested preamble is a '010101...' bit pattern. The same bit pattern should also be used in Manchester mode, giving a '011001100110...' 'chip' pattern. This is necessary for the bit synchronizer to synchronize to the coding correctly. Other preamble patterns than '010101...' can also be used as long as the minimum number of *transitions* is present.

The data slicer does the bit decision. Ideally the two received FSK frequencies are placed symmetrically around the IF frequency. However, if there is some frequency error between the transmitter and the receiver, the bit decision level should be adjusted accordingly. In **CC1020** this is done automatically by measuring the two frequencies and use the average value as the decision level.

The digital data slicer in **CC1020** uses an average value of the minimum and maximum frequency deviation detected as the comparison level. The *RXDEV_X[1:0]* and *RXDEV_M[3:0]* in the *AFC_CONTROL* register are used to set the expected deviation of the incoming signal. Once a shift in the received

frequency larger than the expected deviation is detected, a bit transition is recorded and the average value to be used by the data slicer is calculated.

The minimum number of transitions required to calculate a slicing level is 3. That is, a 010 bit pattern (NRZ).

The actual number of bits used for the averaging can be increased, for better data decision accuracy. This is controlled by the *SETTLING[1:0]* bits in the *AFC_CONTROL* register. If RX data is present in the channel when the RX chain is turned on, then the data slicing estimate will usually give correct results after 3 bit transitions. The data slicing accuracy will increase after this, depending on the *SETTLING[1:0]* bits. If the start of transmission occurs after the RX chain has turned on, the minimum number of bit transitions (or preamble bits) before correct data slicing will depend on the *SETTLING[1:0]* bits.

The automatic data slicer average value function can be disabled by setting *SETTLING[1:0] = 00*. In this case a symmetrical signal around the IF is assumed.

The internally calculated average FSK frequency value gives a measure for the frequency offset of the receiver compared to the transmitter. This information can also be used for an automatic frequency control, as described on page 30.

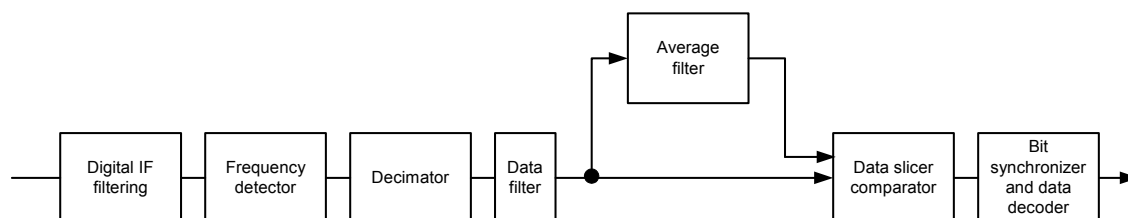


Figure 17. Demodulator block diagram

OOK/ASK Demodulation

The data demodulator can also do OOK/ASK demodulation. OOK/ASK modulation is enabled by setting $TXDEV_M[3:0] = 0000$ in the *DEVIATION* register.

When using OOK/ASK the demodulation is done by comparing the signal level with the "carrier sense" level (programmed as *CS_LEVEL* in the *VGA4* register). The signal is then decimated and filtered in the data filter. Data decision and bit synchronization are as for FSK reception.

In this mode *AGC_AVG* in the *VGA2* register must be set to 3. The channel bandwidth must be 4 times the Baud rate for data rates up to 9.6 kBaud. For higher data rates the channel bandwidth must be 2 times the Baud rate. Manchester coding must always be used for OOK/ASK.

Note that the automatic frequency control (AFC) cannot be used when receiving OOK/ASK, as it requires a frequency shift.

Automatic Frequency Control

CC1020 has a built-in feature called AFC (Automatic Frequency Control) that can be used to compensate for frequency drift.

The average frequency offset of the received signal (from the nominal IF frequency) can be read in the *AFC* register. The signed (2's-complement) 8-bit value $AFC[7:0]$ can be used to compensate for frequency offset between transmitter and receiver.

The frequency offset is given by:

$$\Delta F = AFC \times \text{Baud rate} / 16$$

The receiver can be calibrated against the transmitter by changing the operating frequency according to the measured offset. The new frequency must be calculated and written to the *FREQ* register by the microcontroller. The AFC can be used for an FSK/GFSK signal, but not for OOK/ASK.

This AFC feature reduces the requirement to the crystal accuracy, which is very important in 12.5 and 25 kHz channel width applications.

Digital FM

It is possible to read back the instantaneous IF from the FM demodulator as a frequency offset from the nominal IF frequency. This digital value can be used to do a pseudo analogue FM demodulation.

The frequency offset can be read from the *GAUSS_FILTER* register and is a signed 8-bit value coded as 2-complement.

The instantaneous deviation is given by:

$$F = GAUSS_FILTER \times \text{Baud rate} / 8$$

The digital value should be read from the register and sent to a DAC and filtered in order to get an analogue audio signal. The internal register value is updated at

the *MODEM_CLK* rate. *MODEM_CLK* is available at the *LOCK* pin when $LOCK_SELECT[3:0] = 1101$ in the *LOCK* register, and can be used to synchronize the reading.

For audio (300 – 4000 Hz) the sampling rate should be higher than or equal to 8 kHz (Nyquist) and is determined by the *MODEM_CLK*. The *MODEM_CLK*, which is the sampling rate, equals 8 times the baud rate. That is, the minimum baud rate, which can be programmed, is 1 kBaud. However, the incoming data will be filtered in the digital domain and the 3-dB cut-off frequency is 0.6 times the programmed Baud rate. Thus, for audio the minimum programmed Baud rate should be approximately 7.2 kBaud.

The *GAUSS_FILTER* resolution decreases with increasing baud rate. An accumulate and dump filter can be implemented in the uC to improve the resolution. Note that each *GAUSS_FILTER* reading should be synchronized to the *MODEM_CLK*. As an example, accumulating 4 readings and

dividing the total by 4 will improve the resolution by 2 bits.

Furthermore, to fully utilize the *GAUSS_FILTER* dynamic range the frequency deviation must be 16 times the programmed baud rate.

Automatic Power-up Sequencing

CC1020 has a built-in automatic power-up sequencing state machine. By setting the *CC1020* into this mode, the receiver can be powered-up automatically by a wake-up signal and will then check for a carrier signal (carrier sense). If carrier sense is not detected, it returns to power-down mode. A flow chart for automatic power-up sequencing is shown in Figure 18.

The automatic power-up sequencing mode is selected when *PD_MODE*[1:0] = 11 in the *MAIN* register. When the automatic power-up sequencing mode is selected, the functionality of the *MAIN* register is changed and used to control the sequencing.

By setting *SEQ_PD* = 1 in the *MAIN* register, *CC1020* is set in power down mode. If *SEQ_PSEL* = 1 in the *SEQUENCING* register the automatic power-up sequence is initiated by a negative transition on the PSEL pin.

If *SEQ_PSEL* = 0 in the *SEQUENCING* register, then the automatic power-up sequence is initiated by a negative transition on the DIO pin (as long as *SEP_DI_DO* = 1 in the *INTERFACE* register).

Sequence timing is controlled through *RX_WAIT*[2:0] and *CS_WAIT*[3:0] in the *SEQUENCING* register.

VCO and PLL calibration can also be done automatically as a part of the sequence. This is controlled through *SEQ_CAL*[1:0] in the *MAIN* register. Calibration can be done every time, every 16th sequence, every 256th sequence, or never. See the register description for details. A description of when to do, and how the VCO and PLL self-calibration is done, is given on page 45.

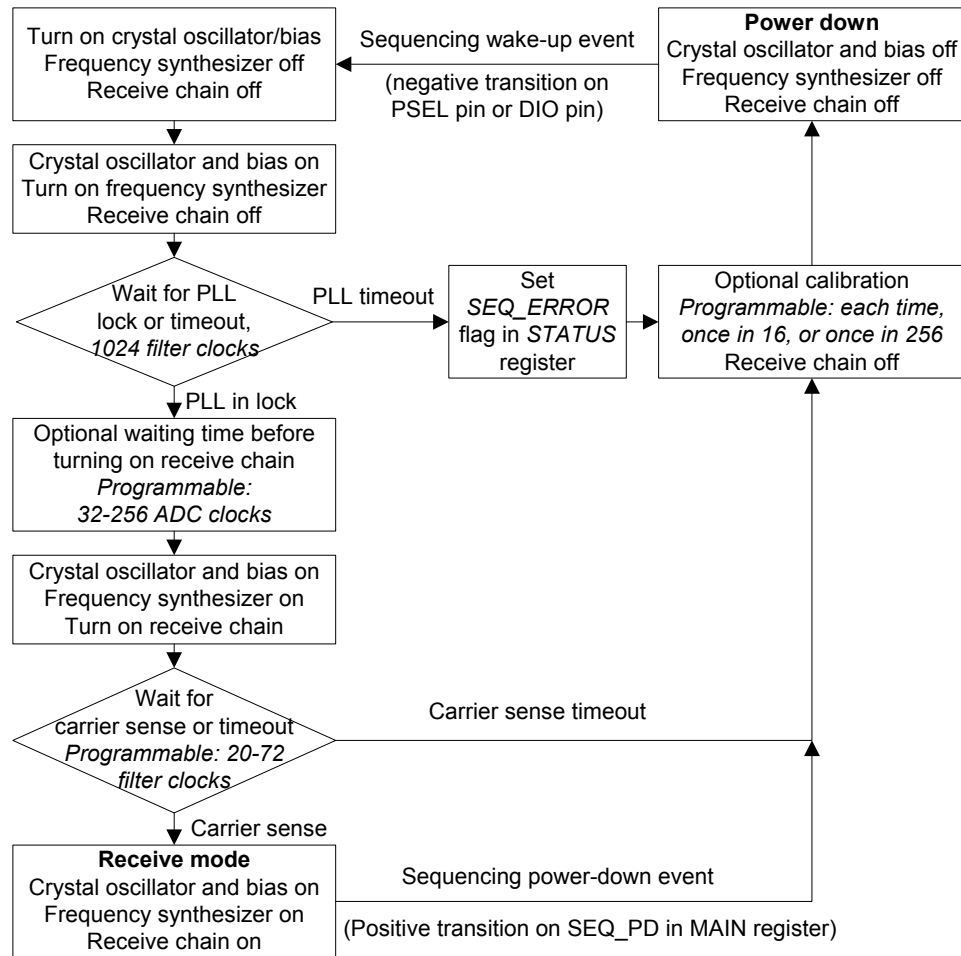


Figure 18. Automatic power-up sequencing flow chart

Notes to Figure 18:

Filter clock:

$$f_{\text{filter}} = 2 \cdot \text{ChBW}$$

where ChBW is defined on page 26.

ADC clock:

$$f_{\text{ADC}} = \frac{f_{\text{xoscx}}}{2 \cdot (\text{ADC_DIV}[2:0] + 1)}$$

where $\text{ADC_DIV}[2:0]$ is set in the *MODEM* register.

RSSI

CC1020 has a built-in RSSI (Received Signal Strength Indicator) giving a digital value that can be read from the *RSSI* register. The RSSI reading must be offset and adjusted for VGA gain setting ($\text{VGA_SETTING}[4:0]$ in the *VGA3* register).

The digital RSSI value is ranging from 0 to 106 (7 bits).

The RSSI reading is a logarithmic measure of the average voltage amplitude after the digital filter in the digital part of the IF chain:

$$\text{RSSI} = 4 \log_2(\text{signal amplitude})$$

The relative power is then given by $\text{RSSI} \times 1.5$ dB in a logarithmic scale.

The number of samples used to calculate the average signal amplitude is controlled by `AGC_AVG[1:0]` in the `VGA2` register. The RSSI update rate is given by:

$$f_{RSSI} = \frac{FILTER_CLK}{2^{AGC_AVG[1:0]+1}}$$

where `AGC_AVG[1:0]` is set in the `VGA2` register.

Maximum VGA gain is programmed by the `VGA_SETTING[4:0]` bits. The VGA gain is programmed in approximately 3 dB/LSB. The RSSI measurement can be referred to the power (absolute value) at the `RF_IN` pin by using the following equation:

$$P = 1.5 \times RSSI - 3 \times VGA_SETTING - RSSI_Offset [dBm]$$

The `RSSI_Offset` depends on the IF bandwidth used due to different VGA

settings. Typical plots of RSSI reading as function of input power for different channel widths are shown in Figure 19 and Figure 20. See the “Receiver Channel Bandwidth” section on page 26 for a list of IF bandwidths corresponding to the various channel widths.

The following method can be used to calculate the power `P` in dBm from the RSSI readout values in Figure 19 and Figure 20:

$$P = 1.5 \times [RSSI - RSSI_ref] + P_ref$$

where `P` is the output power in dBm for the current RSSI readout value. `RSSI_ref` is the RSSI readout value taken from Figure 19 or Figure 20 for an input power level of `P_ref`. Note that the RSSI reading in decimal value changes for different channel bandwidths.

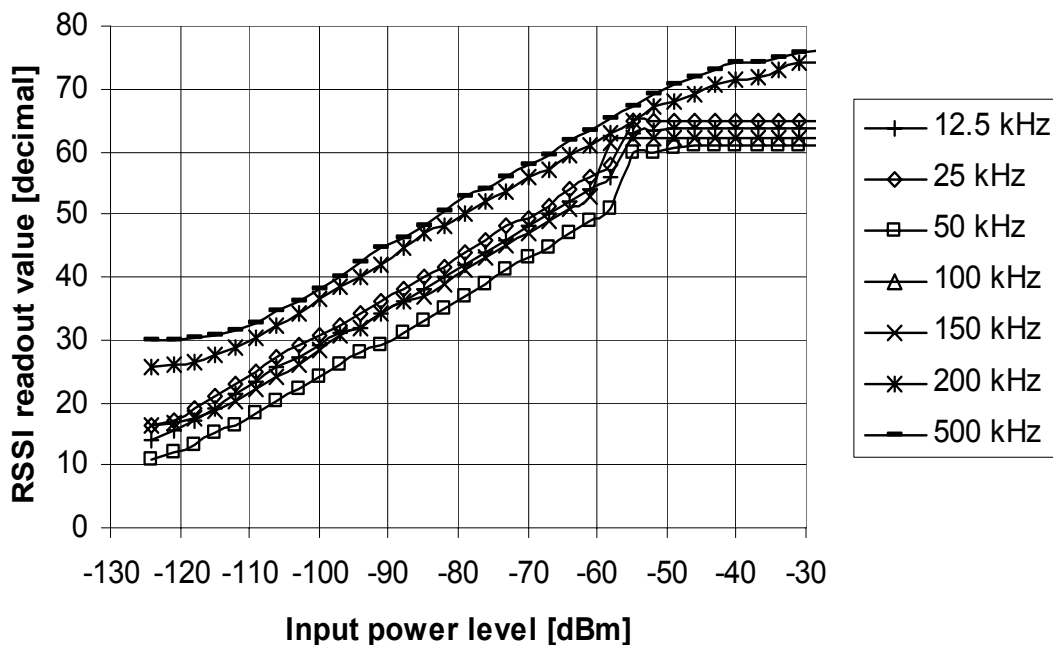


Figure 19. Typical RSSI value vs. input power for some typical channel widths, 433 MHz.

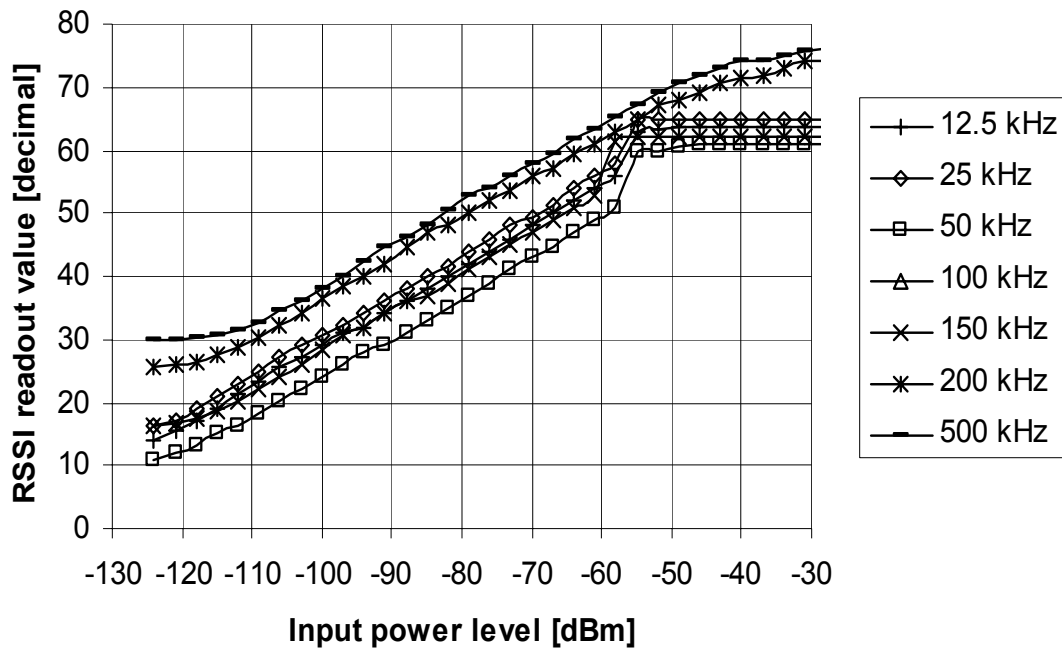


Figure 20. Typical RSSI value vs. input power for some typical channel widths, 868 MHz

Carrier Sense

The carrier sense signal is based on the RSSI value and a programmable threshold. The carrier-sense function can be used to simplify the implementation of a CSMA (Carrier Sense Multiple Access) medium access protocol.

Carrier sense threshold level is programmed by `CS_LEVEL[4:0]` in the `VGA4` register and `VGA_SETTING[4:0]` in the `VGA3` register.

`VGA_SETTING[4:0]` is used to set the maximum gain in the VGA (Variable Gain Amplifier). This value must be set so that the ADC (Analogue-Digital Converter) works with optimum dynamic range for a certain IF-filter bandwidth. The detected signal strength (after the ADC) will therefore depend on this setting.

`CS_LEVEL[4:0]` sets the threshold for this specific `VGA_SETTING[4:0]` value. If the `VGA_SETTING[4:0]` is changed, the `CS_LEVEL[4:0]` must be changed accordingly to maintain the same absolute carrier sense threshold. See Figure 21 for an explanation of the relationship between RSSI, AGC and carrier sense settings.

The carrier sense signal can be read as the `CARRIER_SENSE` bit in the `STATUS` register.

The carrier sense signal can also be made available at the `LOCK` pin by setting `LOCK_SELECT[3:0] = 0100` in the `LOCK` register.

Linear IF chain and AGC Settings

CC1020 is based on a linear IF chain where the signal amplification is done in an analogue VGA (variable gain amplifier). The gain is controlled by the digital part of the IF chain after the ADC (Analogue to Digital Converter). The AGC (Automatic Gain Control) loop ensures that the ADC operates inside its dynamic range by using an analogue/digital feedback loop.

The maximum VGA gain is programmed by the `VGA_SETTING[4:0]` in the `VGA3` register. The VGA gain is programmed in approximately 3 dB/LSB. The VGA gain should be set so that the amplified thermal noise from the front-end balance the quantization noise from the ADC. Therefore the optimum maximum VGA gain setting will depend on the IF bandwidth.

A digital RSSI is used to measure the signal strength after the ADC. The `CS_LEVEL[4:0]` in the `VCA4` register is used to set the nominal operating point of the gain control (and also the carrier sense level). Further explanation can be found in Figure 21.

The VGA gain will be changed according to a threshold set by the `VGA_DOWN[2:0]` in the `VGA3` register and the `VGA_UP[2:0]` in the `VGA4` register. Together, these two values specify the signal strength limits used by the AGC to adjust the VGA gain.

To avoid unnecessary tripping of the VGA, an extra hysteresis and filtering of the RSSI samples can be added. The `AGC_HYSTERESIS` bit in the `VGA2` register enables this.

The time dynamics of the loop can be altered by the `VGA_BLANKING` bit in the `ANALOG` register, and `VGA_FREEZE[1:0]` and `VGA_WAIT[2:0]` bits in the `VGA1` register.

When `VGA_BLANKING` is activated, the VGA recovery time from DC offset spikes after a gain step is reduced.

`VGA_FREEZE` determines the time to hold bit synchronization, VGA and RSSI levels after one of these events occur:

- RX power-up
- The PLL has been out of lock
- Frequency register setting is switched between A and B

This feature is useful to avoid AGC operation during start-up transients and to ensure minimum dwell time using frequency hopping. This means that bit synchronization can be maintained from hop to hop.

`VGA_WAIT` determines the time to hold the present bit synchronization and RSSI levels after changing VGA gain. This feature is useful to avoid AGC operation during the settling of transients after a VGA gain change. Some transients are expected due to DC offsets in the VGA.

At the sensitivity limit, the VGA gain is set by `VGA_SETTING`. In order to optimize selectivity, this gain should not be set higher than necessary. The SmartRF® Studio software gives the settings for `VGA1` – `VGA4` registers. For reference, the following method can be used to find the AGC settings:

1. Disable AGC and use maximum LNA2 gain by writing BFh to the `VGA2` register. Set minimum VGA gain by writing to the `VGA3` register with `VGA_SETTING = 0`.
2. Apply no RF input signal, and measure ADC noise floor by reading the `RSSI` register.
3. Apply no RF input signal, and write `VGA3` register with increasing `VGA_SETTING` value until the `RSSI` register value is approximately 4 larger than the value read in step 2. This places the front-end noise floor around 6 dB above the ADC noise floor.
4. Apply an RF signal with strength equal the desired carrier sense threshold. The RF signal should preferably be modulated with correct Baud rate and deviation. Read the `RSSI` register value, subtract 8, and write to `CS_LEVEL` in the `VGA4` register. Vary the RF signal level slightly and check that carrier sense indication (bit 3 in `STATUS` register) switches at the desired input level.
5. If desired, adjust the `VGA_UP` and `VGA_DOWN` settings according to the explanation in Figure 21.
6. Enable AGC and select LNA2 gain change level. Write 55h to `VGA2` register if the resulting `VGA_SETTING > 10`. Otherwise, write 45h to `VGA2`. Modify `AGC_AVG` in the above `VGA2` value if faster carrier sense and AGC settling is desired.

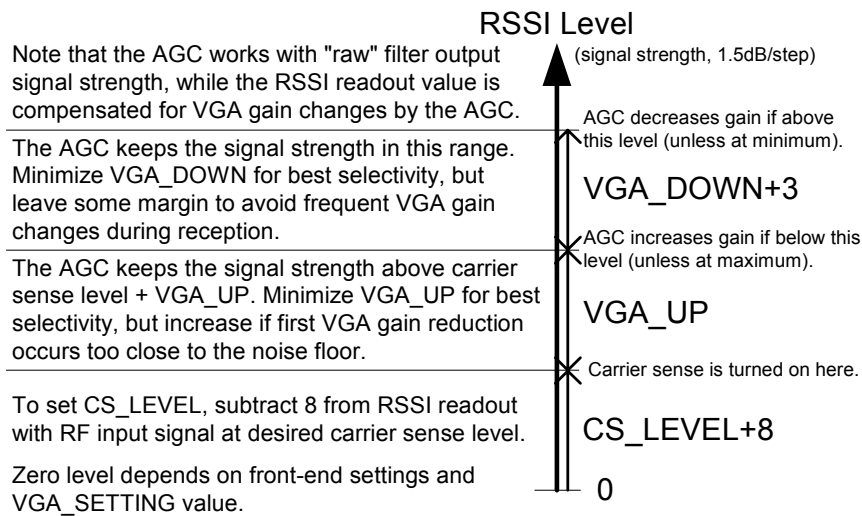


Figure 21. Relationship between RSSI, carrier sense level, and AGC settings `CS_LEVEL`, `VGA_UP` and `VGA_DOWN`.

AGC Settling

After turning on the RX chain, the following occurs:

A) The AGC waits 16-128 `ADC_CLK` (1.2288 MHz) periods, depending on the `VGA_FREEZE` setting in the `VGA1` register, for settling in the analogue parts. Default is 32 periods (about 26 us).

B) The AGC waits 16-48 `FILTER_CLK` periods, depending on the `VGA_WAIT` setting in the `VGA1` register, for settling in the analogue parts and the digital channel filter. 16 periods are recommended.

C) The AGC calculates the RSSI value as the average magnitude over the next 2-16 `FILTER_CLK` periods, depending of the `AGC_AVG` setting in the `VGA2` register. Default is 4 periods.

D) If the RSSI value is higher than `CS_LEVEL+8`, then the carrier sense indicator is set (if `RSSI_SET` = 0). If the RSSI value is too high according to the `CS_LEVEL`, `VGA_UP` and `VGA_DOWN` settings, and the VGA gain is not already

at minimum, then the VGA gain is reduced and the AGC continues from B).

E) If the RSSI value is too low according to the `CS_LEVEL` and `VGA_UP` settings, and the VGA gain is not already at maximum (given by `VGA_SETTING`), then the VGA gain is increased and the AGC continues from B).

2-3 VGA gain changes should be expected before the AGC has settled. Increasing `AGC_AVG` increases the settling time, but may be worthwhile if there is the time in the protocol, and for reducing false wake-up events when setting the carrier sense close to the noise floor.

The AGC settling time depends on the `FILTER_CLOCK` (= 2ChBW). Thus, there is a trade off between AGC settling time and receiver sensitivity because the AGC can be reduced for data rates lower than 76.8 kBaud by using a wider receiver IF filter bandwidth.

Preamble Length and Synch Word

The bit slicer finds the AFC level during the AGC settling, so using the register settings provided by the SmartRF[®] Studio software, 16 bits of '0101010...' preamble should be sufficient for both AGC and bit slicer settling even with *SETTLING[1:0]* = 11.

Packet error rates (PER) less than 1% is possible when using 16 bits of preamble and a 24 bit synch word. The recommended synch word is 0xD391DA. Using 16 bits of preamble and a 16 bit synch word (0xD391) a 1-3% PER can be achieved.

Interrupt upon PLL Lock

In synchronous mode the DCLK pin on **CC1020** can be used to give an interrupt signal to wake the microcontroller when the PLL is locked.

PD_MODE[1:0] in the *MAIN* register should be set to 01. If *DCLK_LOCK* in the *INTERFACE* register is set to 1 the DCLK signal is always logic high if the PLL is not in lock. When the PLL locks to the desired frequency the DCLK signal changes to

logic 0. When this interrupt has been detected write *PD_MODE[1:0]* = 00. This will enable the DCLK signal.

This function can be used to wait for the PLL to be locked before the PA is ramped up in transmit mode. In receive mode, it can be used to wait until the PLL is locked before searching for preamble.

Interrupt upon Received Signal Carrier Sense

In synchronous mode the DCLK pin on **CC1020** can also be used to give an interrupt signal to the microcontroller when the RSSI level exceeds a certain threshold (carrier sense threshold). This function can be used to wake or interrupt the microcontroller when a strong signal is received.

Gating the DCLK signal with the carrier sense signal makes the interrupt signal.

This function should only be used in receive mode and is enabled by setting *DCLK_CS* = 1 in the *INTERFACE* register.

The DCLK signal is always logic high unless carrier sense is indicated. When carrier sense is indicated the DCLK starts running.

In transmit mode *DCLK_CS* must be set to 0.

Interfacing an External LNA or PA

CC1020 has two digital output pins, *PA_EN* and *LNA_EN*, which can be used to control an external LNA or PA. The functionality of these pins are controlled through the *INTERFACE* register. The outputs can also be used as general digital output control signals.

EXT_PA_POL and *EXT_LNA_POL* control the active polarity of the signals.

EXT_PA and *EXT_LNA* control the function of the pins. If *EXT_PA* = 1, then

the *PA_EN* pin will be activated when the internal PA is turned on. Otherwise, the *EXT_PA_POL* bit controls the *PA_EN* pin directly. If *EXT_LNA* = 1, then the *LNA_EN* pin will be activated when the internal LNA is turned on. Otherwise, the *EXT_LNA_POL* bit controls the *LNA_EN* pin directly.

These two pins can therefore also be used as two general control signals, see the next section.

General Purpose Output Control Pins

The two digital output pins, PA_EN and LNA_EN, can be used as two general control signals by setting *EXT_PA* = 0 and *EXT_LNA* = 0. The output value is then set directly by the value written to *EXT_PA_POL* and *EXT_LNA_POL*.

The LOCK pin can also be used as a general-purpose output pin. The LOCK pin is controlled by *LOCK_SELECT[3:0]* in the

LOCK register. The LOCK pin is low when *LOCK_SELECT[3:0]* = 0000, and high when *LOCK_SELECT[3:0]* = 0001.

These features can be used to save I/O pins on the microcontroller when the other functions associated with these pins are not used.

Receiver Sensitivity versus Data Rate and Frequency Separation

The receiver sensitivity depends on the channel bandwidth, data rate, data format, FSK frequency separation and the RF frequency. Typical figures for the receiver sensitivity ($BER = 10^{-3}$) are shown in Table 6 and Table 7 for FSK and Table 8 for ASK/OOK. For best performance, the frequency deviation should be at least half the baud rate in FSK mode.

The sensitivity is measured using the matching network shown in the application

circuit in Figure 3 which also includes an external T/R switch and an LC low-pass filter.

Bit error rate (BER) as a function of input power level is shown in Figure 22. Sensitivity versus data rate is shown in Figure 23 and Figure 24 for 868 MHz and 433 MHz respectively. Sensitivity versus frequency offset is shown in Figure 25.

Data rate [kBaud]	Channel width [kHz]	Deviation [kHz]	Filter BW [kHz]	NRZ mode	Manchester mode	UART mode
2.4 optimized sensitivity	12.5	± 2	9.6	-118	-121	-118
2.4 optimized selectivity	12.5	± 2.4	12.288	-114	-117	-114
4.8	25	± 2.4	19.2	-115	-115	-115
4.8	25	± 4	19.2	-115	-118	-115
9.6	50	± 4.8	25.6	-113	-113	-113
19.2	100	± 9.6	51.2	-111	-111	-111
38.4	150	± 19.2	102.4	-108	-108	-108
76.8	200	± 38.4	153.6	-105	-105	-105
153.6	500	± 76.8	307.2	-97	-97	-97

Table 6. Receiver sensitivity as a function of data rate at 433 MHz, FSK modulation, $BER = 10^{-3}$, pseudo-random data (PN9 sequence).

Data rate [kBaud]	Channel width [kHz]	Deviation [kHz]	Filter BW [kHz]	NRZ mode	Manchester mode	UART mode
2.4 optimized sensitivity	12.5	± 2	9.6			
2.4 optimized selectivity	12.5	± 2.4	12.288	-114	-116	-114
4.8	25	± 2.4	19.2	-112	-113	-112
4.8	25	± 4	19.2	-112	-115	-112
9.6	50	± 4.8	25.6	-111	-111	-111
19.2	100	± 9.6	51.2	-108	-108	-108
38.4	150	± 19.2	102.4	-105	-105	-105
76.8	200	± 38.4	153.6	-100	-100	-100
153.6	500	± 76.8	307.2	-94	-94	-94

Table 7. Receiver sensitivity as a function of data rate at 868 MHz, FSK modulation, BER = 10^{-3} , pseudo-random data (PN9 sequence).

Data rate [kBaud]	Channel width [kHz]	Filter BW [kHz]	433 MHz Manchester mode	868 MHz Manchester mode
2.4	12.5	9.6	-116	TBD
4.8	25	19.2	-113	-107
9.6	80	38.4	-103	-104
19.2	100	51.2	-102	-101
38.4	150	102.4	-95	-97
76.8	200	153.6	-92	-94
153.6	500	307.2	-81	-87

Table 8. Receiver sensitivity as a function of data rate at 433 and 868 MHz, ASK/OOK modulation, BER = 10^{-3} , pseudo-random data (PN9 sequence).

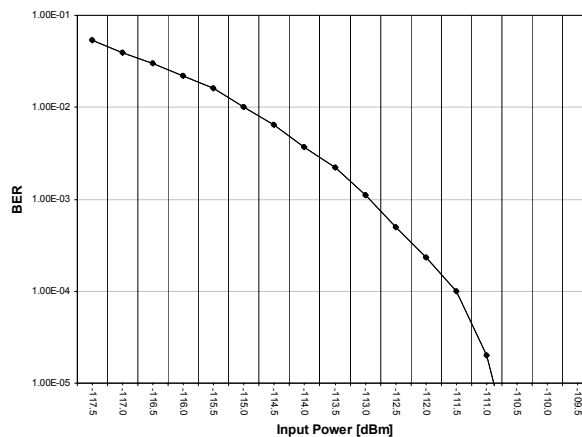


Figure 22. Bit error rate (BER) versus input power level, 868 MHz, 25 kHz channel width, 4.8 kBaud, NRZ, PN9 test pattern (FSK)

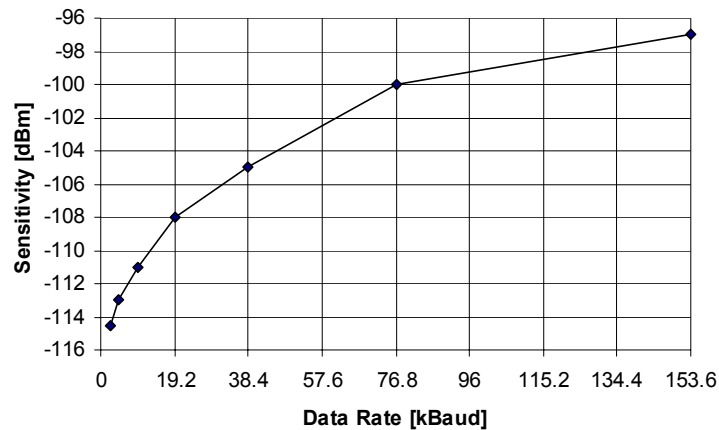


Figure 23. Sensitivity versus data rate at 868 MHz (FSK)

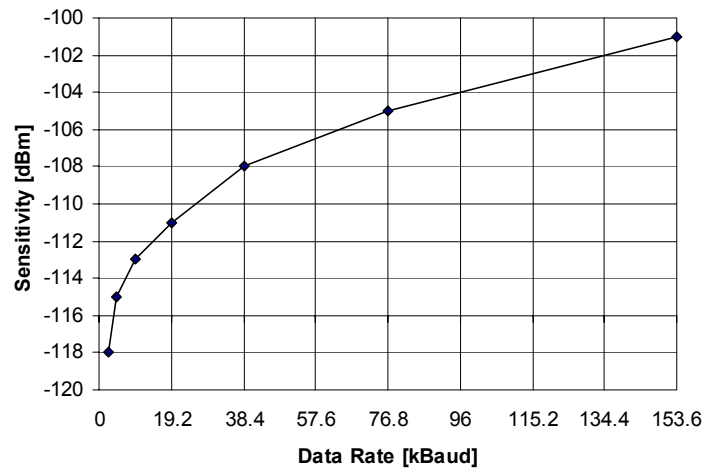


Figure 24. Sensitivity versus data rate at 433 MHz (FSK)

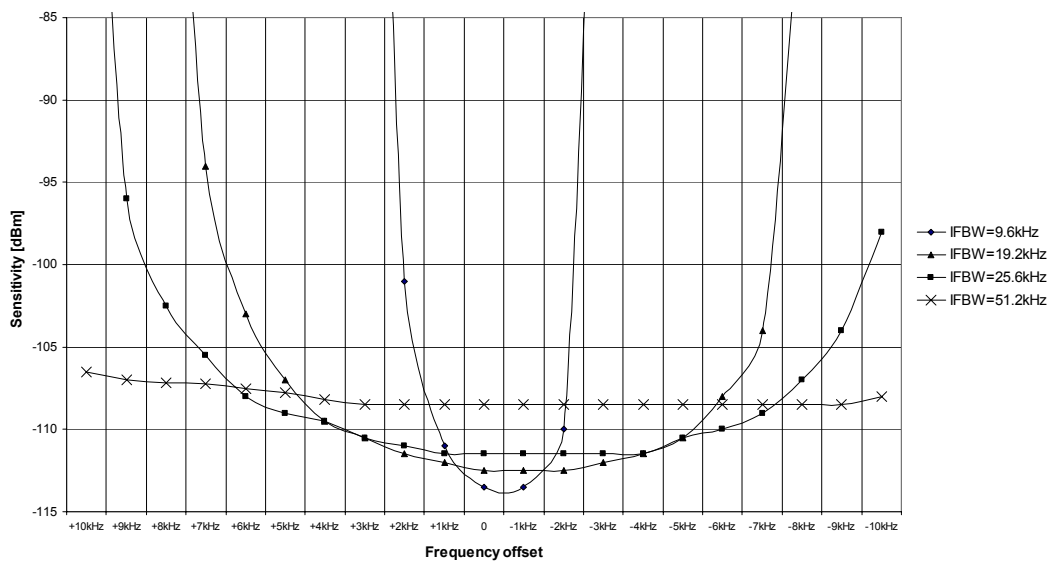


Figure 25. Sensitivity versus frequency offset, 868 MHz, 4.8 kBaud (FSK)

Blocking and Selectivity

Figure 26 and Figure 27 show the blocking/selectivity at 434 MHz and 868 MHz respectively. The blocking rejection is

the ratio between a modulated blocker (interferer) and a wanted signal 3 dB above the sensitivity limit.

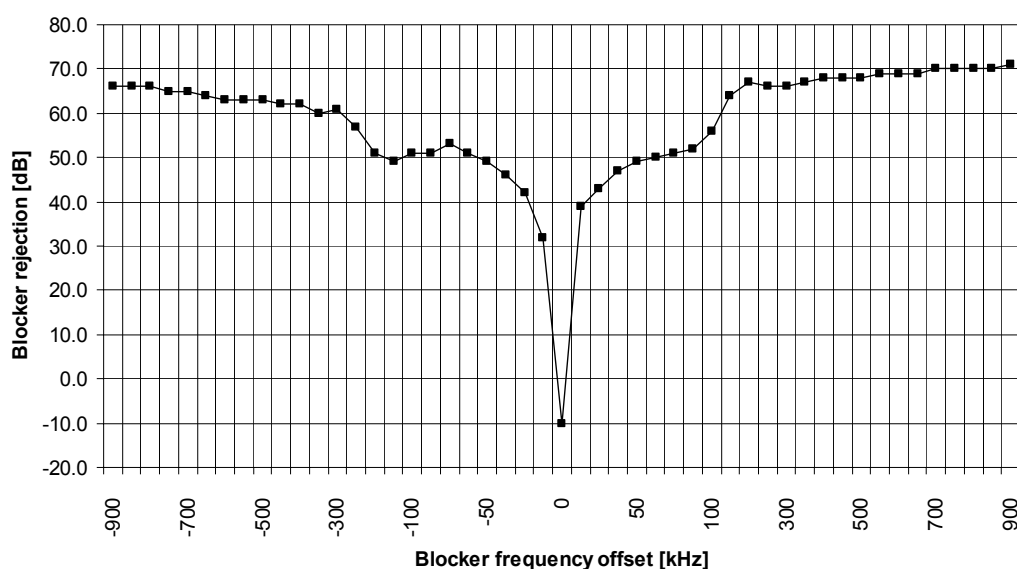


Figure 26. Typical blocker rejection. Carrier frequency set to 434.3072 MHz (12.5 kHz channel width)

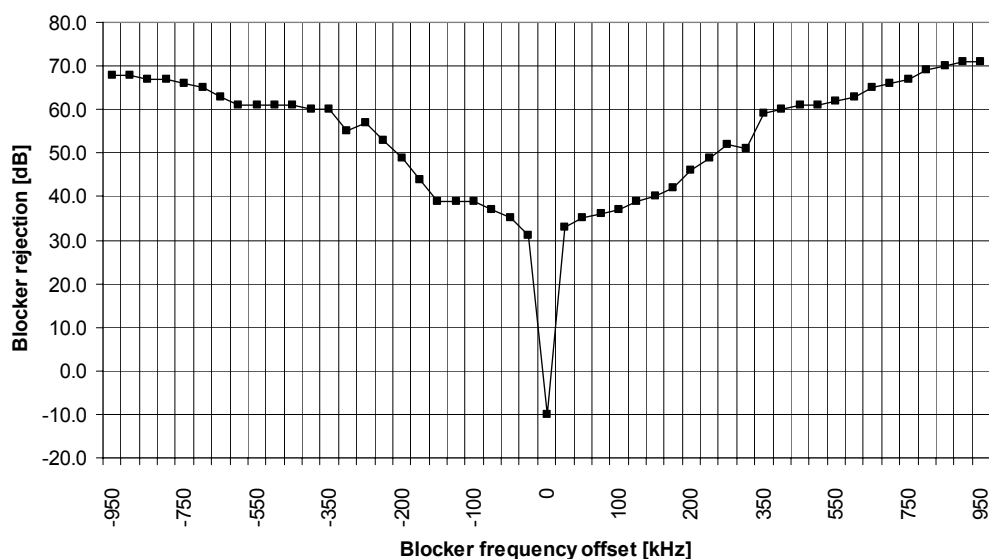


Figure 27. Typical blocker rejection. Carrier frequency set to 868.3072 MHz (25 kHz channel width)

Image Rejection Calibration

For perfect image rejection, the phase and gain of the “I” and “Q” parts of the analogue RX chain must be perfectly matched. To improve the image rejection, the “I” and “Q” phase and gain difference can be fine-tuned by adjusting the *PHASE_COMP* and *GAIN_COMP* registers. This allows compensation for process variations and other nonidealities. The calibration is done by injecting a signal at the image frequency, and adjusting the phase and gain difference for minimum RSSI value.

During image rejection calibration, an unmodulated carrier should be applied at the image frequency (614.4 kHz below the desired channel). No signal should be present in the desired channel. The signal level should be 50 - 60 dB above the sensitivity in the desired channel, but the optimum level will vary from application to application. Too large input level gives poor results due to limited linearity in the analogue IF chain, while too low input level gives poor results due to the receiver noise floor.

For best RSSI accuracy, use *AGC_AVG(1:0)* = 11 during image rejection calibration (RSSI value is averaged over 16 filter output samples). The RSSI register update rate then equals the receiver channel bandwidth (set in *FILTER* register) divided by 8, as the filter output rate is twice the receiver channel bandwidth. This gives the minimum waiting time between RSSI register reads (0.5 ms is used below). Chipcon recommends the following image calibration procedure:

1. Define 3 variables: *XP* = 0, *XG* = 0 and *DX* = 64.
Go to step 3.
2. Set *DX* = *DX*/2.
3. Write *XG* to *GAIN_COMP* register.
4. If *XP*+2·*DX* < 127 then
 write *XP*+2·*DX* to *PHASE_COMP* register
else
 write 127 to *PHASE_COMP* register.
5. Wait at least 3 ms. Measure signal strength *Y4* as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
6. Write *XP*+*DX* to *PHASE_COMP* register.
7. Wait at least 3 ms. Measure signal strength *Y3* as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
8. Write *XP* to *PHASE_COMP* register.

9. Wait at least 3 ms. Measure signal strength *Y2* as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
10. Write *XP*-*DX* to *PHASE_COMP* register.
11. Wait at least 3 ms. Measure signal strength *Y1* as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
12. Write *XP*-2·*DX* to *PHASE_COMP* register.
13. Wait at least 3 ms. Measure signal strength *Y0* as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
14. Set $AP = 2 \cdot (Y0 - Y2 + Y4) - (Y1 + Y3)$.
15. If *AP* > 0 then
 set $DP = \text{ROUND}(7 \cdot DX \cdot (2 \cdot (Y0 - Y4) + Y1 - Y3) / (10 \cdot AP))$
else
 if *Y0*+*Y1* > *Y3*+*Y4* then
 set *DP* = *DX*
 else
 set *DP* = -*DX*.
16. If *DP* > *DX* then
 set *DP* = *DX*
else
 if *DP* < -*DX* then set *DP* = -*DX*.
17. Set *XP* = *XP*+*DP*.
18. Write *XP* to *PHASE_COMP* register.
19. If *XG*+2·*DX* < 127 then
 write *XG*+2·*DX* to *GAIN_COMP* register
else
 write 127 to *GAIN_COMP* register.
20. Wait at least 3 ms. Measure signal strength *Y4* as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
21. Write *XG*+*DX* to *GAIN_COMP* register.
22. Wait at least 3 ms. Measure signal strength *Y3* as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
23. Write *XG* to *GAIN_COMP* register.
24. Wait at least 3 ms. Measure signal strength *Y2* as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
25. Write *XG*-*DX* to *GAIN_COMP* register.
26. Wait at least 3 ms. Measure signal strength *Y1* as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
27. Write *XG*-2·*DX* to *GAIN_COMP* register.
28. Wait at least 3 ms. Measure signal strength *Y0* as filtered average of 8 reads from RSSI register with 0.5 ms of delay between each RSSI read.
29. Set $AG = 2 \cdot (Y0 - Y2 + Y4) - (Y1 + Y3)$.
30. If *AG* > 0 then
 set $DG = \text{ROUND}(7 \cdot DX \cdot (2 \cdot (Y0 - Y4) + Y1 - Y3) / (10 \cdot AG))$
else
 if *Y0*+*Y1* > *Y3*+*Y4* then
 set *DG* = *DX*
 else
 set *DG* = -*DX*.
31. If *DG* > *DX* then
 set *DG* = *DX*
else
 if *DG* < -*DX* then set *DG* = -*DX*.
32. Set *XG* = *XG*+*DG*.
33. If *DX* > 1 then go to step 2.
34. Write *XP* to *PHASE_COMP* register and *XG* to *GAIN_COMP* register.

If repeated calibration gives varying results, try to change the input level or increase the number of RSSI reads N . A good starting point is $N=8$. As accuracy is

more important in the last fine-calibration steps, it can be worthwhile to increase N for each loop iteration (for example by increasing N in step 16).

Frequency Programming

Programming the frequency word in the configuration registers sets the operation frequency. There are two frequency words registers, termed *FREQ_A* and *FREQ_B*, which can be programmed to two different frequencies. One of the frequency words can be used for RX (local oscillator frequency) and the other for TX (transmitting carrier frequency) in order to be able to switch very fast between RX mode and TX mode. They can also be used for RX (or TX) at two different channels. The *F_REG* bit in the *MAIN* register selects frequency word A or B.

The frequency word is located in *FREQ_2A:FREQ_1A:FREQ_0A* and *FREQ_2B:FREQ_1B:FREQ_0B* for the *FREQ_A* and *FREQ_B* word respectively. The LSB of the *FREQ_0* registers are used to enable dithering, see next section.

The PLL output frequency is given by:

$$f_c = f_{ref} \cdot \left(\frac{3}{4} + \frac{FREQ + 0.5 \cdot DITHER}{32768} \right)$$

in the frequency band 402 – 470 MHz, and

$$f_c = f_{ref} \cdot \left(\frac{3}{2} + \frac{FREQ + 0.5 \cdot DITHER}{16384} \right)$$

in the frequency band 804 – 940 MHz.

The *BANDSELECT* bit in the *ANALOG* register controls the frequency band used. *BANDSELECT* = 0 gives 402 - 470 MHz, and *BANDSELECT* = 1 gives 804 - 940 MHz.

The reference frequency is the crystal oscillator clock frequency divided by *REF_DIV* (3 bits in the *CLOCK_A* or *CLOCK_B* register), a number between 1 and 7:

$$f_{ref} = \frac{f_{xosc}}{REF_DIV + 1}$$

FSK frequency deviation is programmed in the *DEVIATION* register. The deviation programming is divided into a mantissa (*TXDEV_M[3:0]*) and an exponent (*TXDEV_X[2:0]*).

Generally *REF_DIV* should be as low as possible but the following requirements must be met

$$9.8304 \geq f_{ref} > \frac{f_c}{256} [MHz]$$

in the frequency band 402 – 470 MHz, and

$$9.8304 \geq f_{ref} > \frac{f_c}{512} [MHz]$$

in the frequency band 804 - 940 MHz.

The PLL output frequency equations above give the carrier frequency, f_c , in transmit mode (center frequency). The two FSK modulation frequencies are given by:

$$f_0 = f_c - f_{dev}$$

$$f_1 = f_c + f_{dev}$$

where f_{dev} is set by the *DEVIATION* register:

$$f_{dev} = f_{ref} \cdot TXDEV_M \cdot 2^{(TXDEV_X-16)}$$

in the frequency band 402 – 470 MHz and

$$f_{dev} = f_{ref} \cdot TXDEV_M \cdot 2^{(TXDEV_X-15)}$$

in the frequency band 804 - 940 MHz.

OOK (On-Off Keying) is used if *TXDEV_M[3:0]* = 0000.

The *TX_SHAPING* bit in the *DEVIATION* register controls Gaussian shaping of the modulation signal.

In receive mode the frequency must be programmed to be the LO frequency. Low side LO injection is used, hence:

$$f_{LO} = f_c - f_{IF}$$

where f_{IF} is the IF frequency (ideally 307.2 kHz).

Dithering

Spurious signals will occur at certain frequencies depending on the division ratios in the PLL. To reduce the strength of these spurs, a common technique is to use a dithering signal in the control of the frequency dividers. Dithering is activated

by setting the *DITHER* bit in the *FREQ_0* registers. It is recommended to use the dithering in order to achieve the best possible performance.

VCO, Charge Pump and PLL Loop Filter

The VCO is completely integrated and operates at 1608 – 1880 MHz. A frequency divider is used to get a frequency in the UHF range (402 – 470 and 804 – 940 MHz). The *BANDSELECT* bit in the *ANALOG* register selects the frequency band.

The VCO frequency is given by:

$$f_{VCO} = f_{ref} \cdot \left(3 + \frac{FREQ + 0.5 \cdot DITHER}{8192} \right)$$

The VCO frequency is divided by 2 and by 4 to generate frequencies in the two bands, respectively.

The VCO sensitivity (sometimes referred to as VCO gain) varies over frequency and operating conditions. Typically the VCO sensitivity varies between 12 and 36 MHz/V. For calculations the geometrical mean at 21 MHz/V can be used. The PLL calibration (explained below) measures the actual VCO sensitivity and adjusts the charge pump current accordingly to achieve correct PLL loop gain and bandwidth (higher charge pump current when VCO sensitivity is lower).

The PLL loop filter component values, see Figure 3, can be calculated using the following equations for a desired PLL loop bandwidth, BW:

$$\begin{aligned} C7 &= 3037 (f_{ref} / BW^2) - 7 & [\text{pF}] \\ R2 &= 7126 (BW / f_{ref}) & [\text{k}\Omega] \end{aligned}$$

$$\begin{aligned} C6 &= 80.75 (f_{ref} / BW^2) & [\text{nF}] \\ R3 &= 21823 (BW / f_{ref}) & [\text{k}\Omega] \\ C8 &= 839 (f_{ref} / BW^2) - 6 & [\text{pF}] \end{aligned}$$

After calibration the PLL bandwidth is set by the *PLL_BW* register in combination with the external loop filter components calculated above. The *PLL_BW* can be found from:

$$PLL_BW = 174 + 16 \log_2(BW/R2)$$

where BW is the desired loop bandwidth (in Hz) and R2 is the value (in ohm) of the loop filter resistor, see Figure 3. The PLL loop filter bandwidth increases with increasing *PLL_BW* setting. Note that in SmartRF® Studio *PLL_BW* is fixed to 9E hex for 2.4 kBaud, optimized selectivity. BW is set to Baud rate/3 in SmartRF® Studio for data rates above 4.8 kBaud.

After calibration the applied charge pump current (*CHP_CURRENT[3:0]*) can be read in the *STATUS1* register. The charge pump current is approximately given by:

$$I_{CHP} = 16 \cdot 2^{CHP_CURRENT / 4} [\mu A]$$

The combined charge pump and phase detector gain (in A/rad) is given by the charge pump current divided by 2π .

The PLL bandwidth will limit the maximum modulation frequency and hence data rate.

VCO and PLL Self-Calibration

To compensate for supply voltage, temperature and process variations, the VCO and PLL must be calibrated. The calibration is performed automatically and sets the maximum VCO tuning range and optimum charge pump current for PLL stability. After setting up the device at the operating frequency, the self-calibration can be initiated by setting the **CAL_START** bit in the **CALIBRATE** register. The calibration result is stored internally in the chip, and is valid as long as power is not turned off. If large supply voltage drops (more than -0.25 V) or temperature variations (more than 40°C) occur after calibration, a new calibration should be performed.

The **CAL_COMPLETE** bit in the **STATUS** register indicates that calibration has finished. The user can poll this bit, or simply wait a certain time. The calibration wait time (**CAL_WAIT**) is programmable and is proportional to the internal PLL reference frequency. The highest possible reference frequency should be used to get the minimum calibration time. It is recommended to use **CAL_WAIT[1:0] = 11** in order to get the most accurate loop bandwidth.

Calibration time [ms]	Reference frequency [MHz]		
CAL_WAIT	1.8432	7.3728	9.8304
00	49 ms	12 ms	10 ms
01	60 ms	15 ms	11 ms
10	71 ms	18 ms	13 ms
11	109 ms	27 ms	20 ms

The **CAL_COMPLETE** bit can also be monitored at the LOCK pin, configured by

LOCK_SELECT[3:0] = 0101, and used as an interrupt input to the microcontroller.

There are separate calibration values for the two frequency registers, but the results of a single calibration can be used for both registers. The **CAL_DUAL** bit in the **CALIBRATE** register controls dual or separate calibration. Dual calibration should only be used if all of the below conditions apply:

- The two frequencies A and B differ by less than 1 MHz
- Reference frequencies are equal (**REF_DIV_A[2:0] = REF_DIV_B[2:0]** in the **CLOCK_A/CLOCK_B** registers)
- VCO currents are equal (**VCO_CURRENT_A[3:0] = VCO_CURRENT_B[3:0]** in the **VCO** register).

The single calibration algorithm using separate calibration for RX and TX frequency is illustrated in Figure 28. Application Note *AN023 CC1020 MCU Interfacing*, available from the Chipcon web site, includes example source code for single calibration.

In Figure 29, the dual calibration algorithm is shown for two RX frequencies. It could also be used for two TX frequencies, or even for one RX and one TX frequency if the same VCO current is used.

Chipcon recommends that single calibration be used for more robust operation.

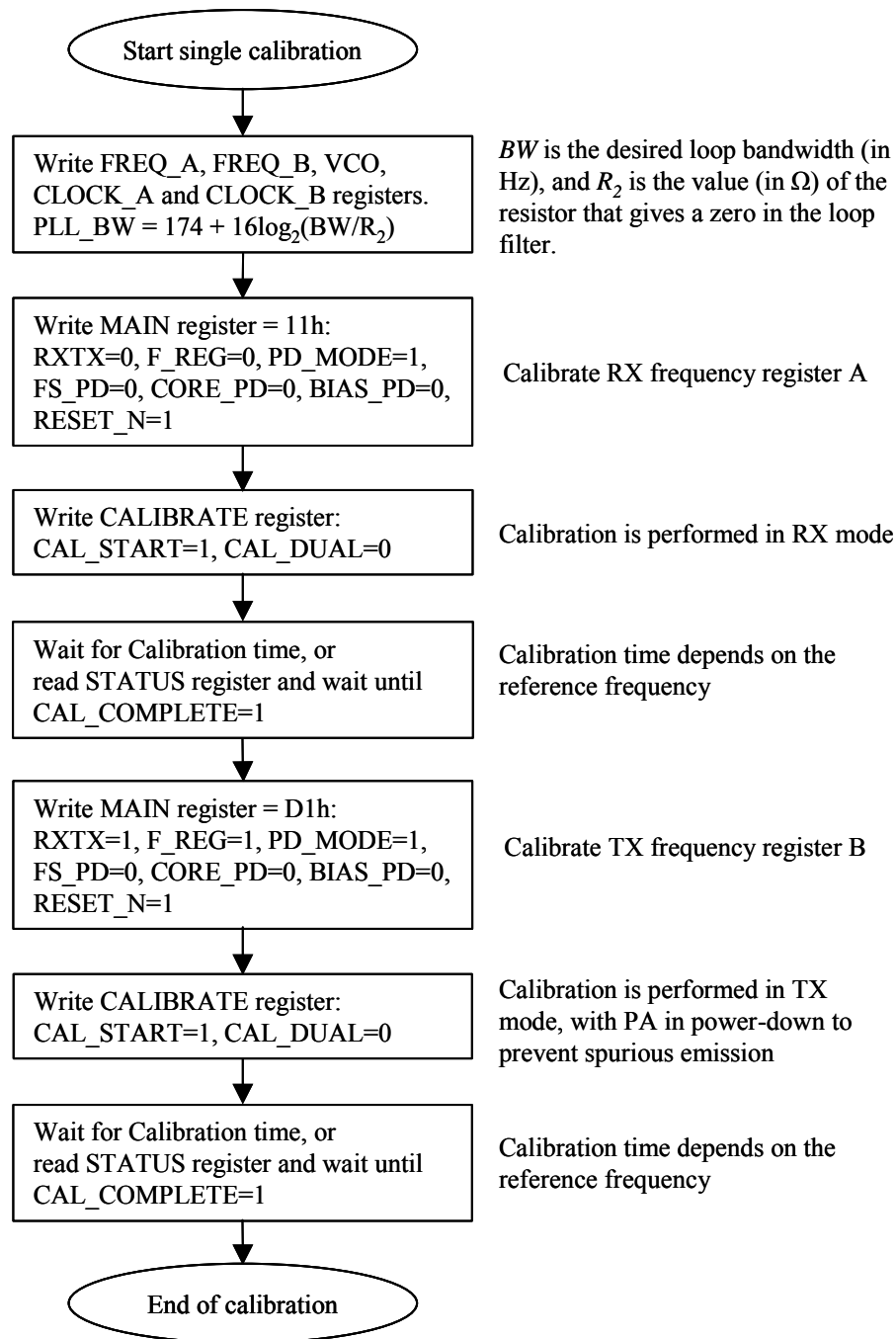


Figure 28. Single calibration algorithm for RX and TX

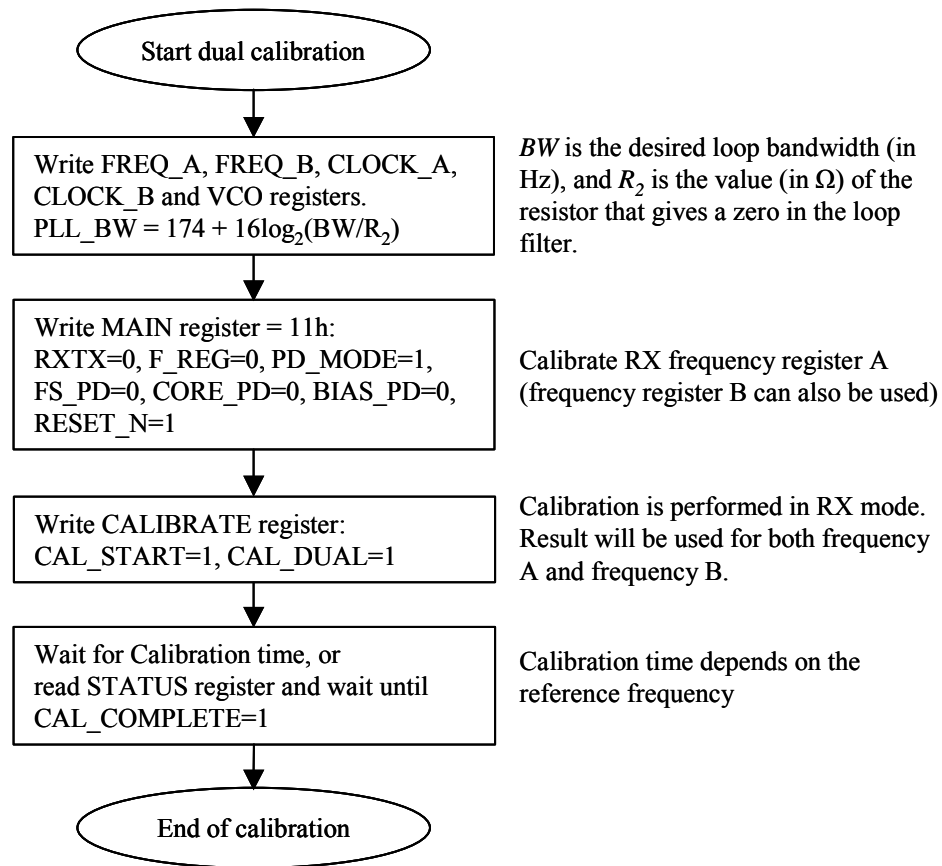


Figure 29. Dual calibration algorithm for RX mode

PLL Turn-on Time versus Loop Filter Bandwidth

It is only required to calibrate the VCO and PLL when **CC1020** is initially power up.

If calibration has been performed the PLL turn-on time is the time needed for the PLL to lock to the desired frequency when going from power down mode (with the

crystal oscillator running) to Tx or Rx mode. The PLL turn-on time depends on the PLL loop filter bandwidth. Table 9 gives the PLL turn-on time for different PLL loop filter bandwidths.

C6 [nF]	C7 [pF]	C8 [pF]	R2 [k Ω]	R3 [k Ω]	PLL turn-on time [μ s]	Comment
220	8200	2200	1.5	4.7	3200	Up to 4.8 kBaud data rate, 12.5 kHz channel width
100	3900	1000	2.2	6.8	2500	Up to 4.8 kBaud data rate, 25 kHz channel width
56	2200	560	3.3	10	1400	Up to 9.6 kBaud data rate, 50 kHz channel width
15	560	150	5.6	18	1300	Up to 19.2 kBaud data rate, 100 kHz channel width
3.9	120	33	12	39	1080	Up to 38.4 kBaud data rate, 150 kHz channel width
1.0	27	3.3	27	82	950	Up to 76.8 kBaud data rate, 200 kHz channel width
0.2	1.5	-	47	150	700	Up to 153.6 kBaud data rate, 500 kHz channel width

Table 9. Typical PLL turn-on time to within $\pm 10\%$ of channel width for different loop filter bandwidths.

PLL Lock Time versus Loop Filter Bandwidth

It is only required to calibrate the VCO and PLL when **CC1020** is initially power up.

If calibration has been performed the PLL lock time is the time needed for the PLL to lock to the desired frequency when going

from Rx to Tx mode or vice versa. The PLL lock time depends on the PLL loop filter bandwidth. The table below gives the PLL lock time for different PLL loop filter bandwidths.

C6 [nF]	C7 [pF]	C8 [pF]	R2 [kΩ]	R3 [kΩ]	PLL lock time [μs]			Comment
					1	2	3	
220	8200	2200	1.5	4.7	900	180	1300	Up to 4.8 kBaud data rate, 12.5 kHz channel width
100	3900	1000	2.2	6.8	640	270	830	Up to 4.8 kBaud data rate, 25 kHz channel width
56	2200	560	3.3	10	400	140	490	Up to 9.6 kBaud data rate, 50 kHz channel width
15	560	150	5.6	18	140	70	230	Up to 19.2 kBaud data rate, 100 kHz channel width
3.9	120	33	12	39	75	50	180	Up to 38.4 kBaud data rate, 150 kHz channel width
1.0	27	3.3	27	82	30	15	55	Up to 76.8 kBaud data rate, 200 kHz channel width
0.2	1.5	-	47	150	14	14	28	Up to 153.6 kBaud data rate, 500 kHz channel width

Table 10. Typical PLL lock time to within ±10% of channel width for different loop filter bandwidths. 1) 307.2 kHz step, 2) 1 channel step, 3) 1 MHz step.

VCO and LNA Current Control

The VCO current is programmable and should be set according to operating frequency, RX/TX mode and output power. Recommended settings for the **VCO_CURRENT** bits in the **VCO** register are shown in the register overview and also given by SmartRF[®] Studio. The VCO current for frequency **FREQ_A** and

FREQ_B can be programmed independently.

The bias currents for the LNA, mixer and the LO and PA buffers are also programmable. The **FRONTEND** and the **BUFF_CURRENT** registers control these currents.

Power Management

CC1020 offers great flexibility for power management in order to meet strict power consumption requirements in battery-operated applications. Power down mode is controlled through the **MAIN** register. There are separate bits to control the RX part, the TX part, the frequency synthesizer and the crystal oscillator in the **MAIN** register. This individual control can be used to optimize for lowest possible current consumption in each application. Figure 30 shows a typical power-on and initializing sequence for minimum power consumption.

Figure 31 shows a typical sequence for activating RX and TX mode from power down mode for minimum power consumption.

Note that **PSEL** should be tri-stated or set to a high level during power down mode in order to prevent a trickle current from flowing in the internal pull-up resistor.

Application Note **AN023 CC1020 MCU Interfacing** includes example source code and is available from the Chipcon web site.

Chipcon recommends resetting the **CC1020** (by clearing the **RESET_N** bit in the **MAIN** register) when the chip is powered up initially. All registers that need to be configured should then be programmed (those which differ from their default values). Registers can be programmed freely in any order. The **CC1020** should then be calibrated in both RX and TX mode. After this is completed, the **CC1020** is ready for use. See the detailed procedure flowcharts in Figure 28 - Figure 31.

With reference to Application Note **AN023 CC1020 MCU Interfacing** Chipcon recommends the following sequence:

After power up:

- 1) ResetCC1020
- 2) Initialise
- 3) WakeUpCC1020ToRX
- 4) Calibrate
- 5) WakeUpCC1020ToTX
- 6) Calibrate

After calibration is completed, enter TX mode (SetupCC1020TX), RX mode (SetupCC1020RX) or power down mode (SetupCC1020PD)

From power-down mode to Rx:

- 1) WakeUpCC1020ToRX
- 2) SetupCC1020RX

From power-down mode to Tx:

- 1) WakeUpCC1020ToTX
- 2) SetupCC1020TX

Switching from RX to Tx mode:

- 1) SetupCC1020TX

Switching from TX to Rx mode:

- 1) SetupCC1020RX

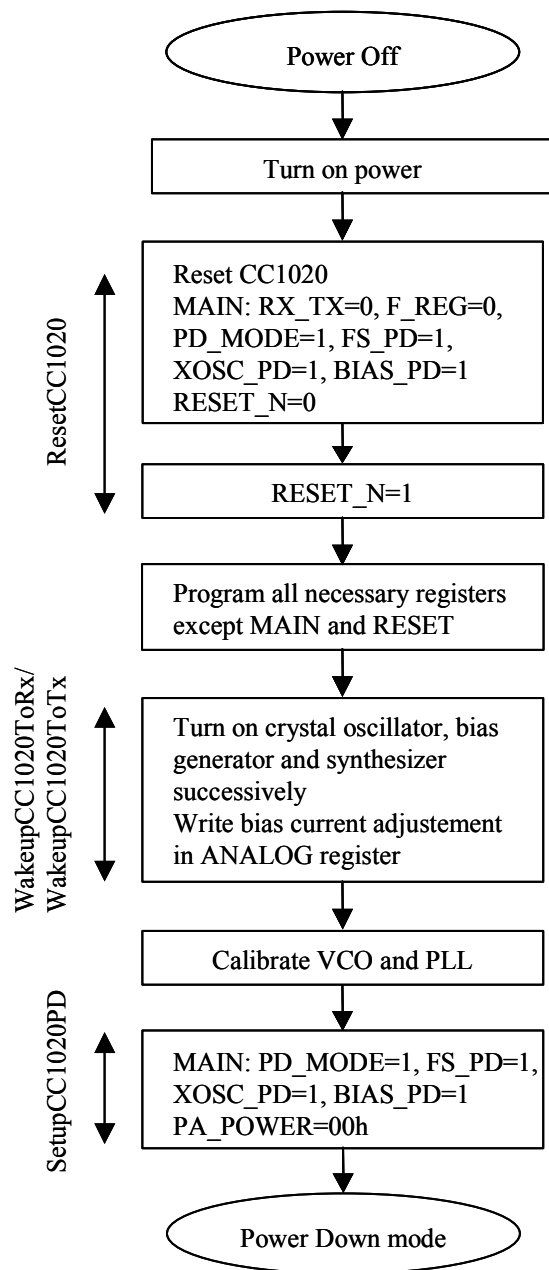


Figure 30. Initializing sequence

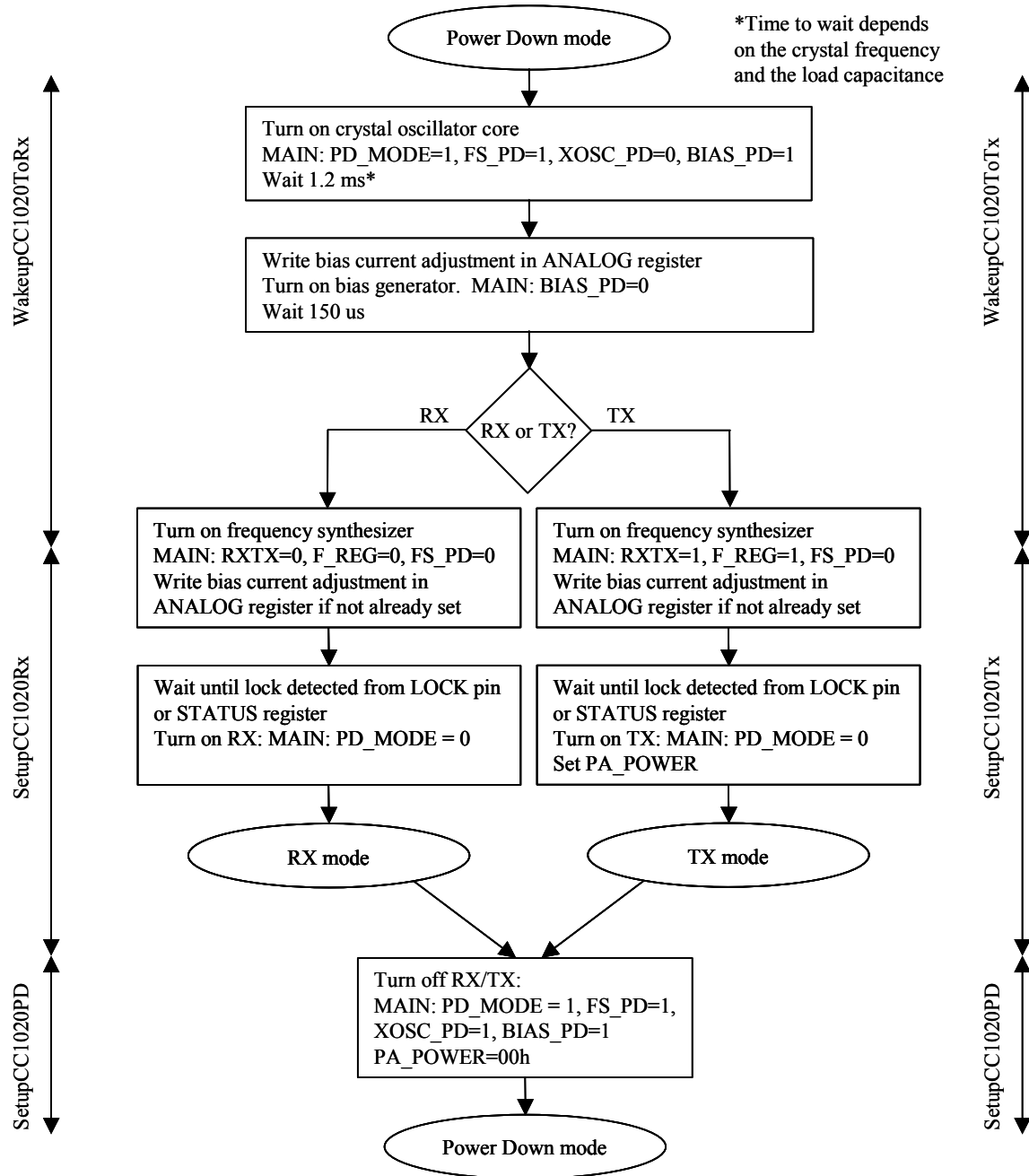


Figure 31. Sequence for activating RX or TX mode

Output Power Programming

The RF output power from the device is programmable by the 8-bit *PA_POWER* register. Figure 32 and Figure 33 shows the output power and total current consumption as a function of the *PA_POWER* register setting. It is more current efficient in terms of current

consumption to use either the lower or upper 4-bits in the register to control the power, as shown in the figures. However, the output power can be controlled in finer steps using all the available bits in the *PA_POWER* register.

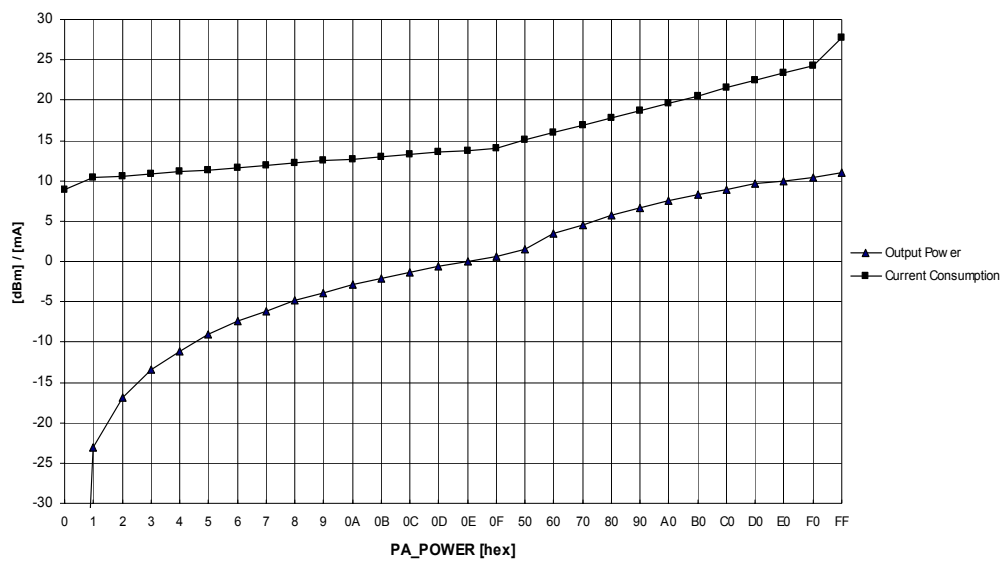


Figure 32. Output power settings and typical current consumption, 433 MHz

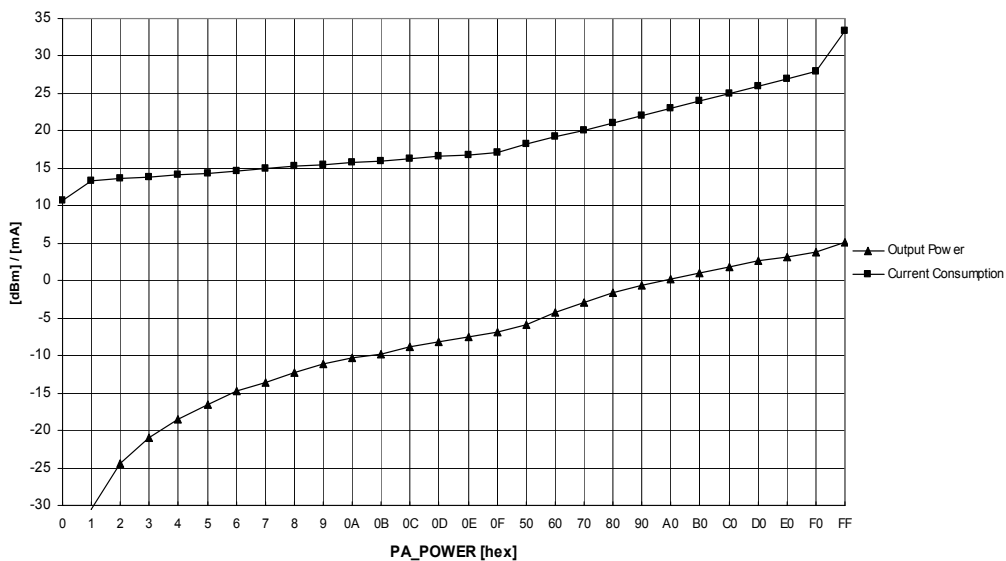


Figure 33. Output power settings and typical current consumption, 868 MHz

Crystal Oscillator

The recommended crystal frequency is 14.7456 MHz, but any crystal frequency in the range 4 - 20 MHz can be used. Using a crystal frequency different from 14.7456 MHz might in some applications give degraded performance. Refer to Application Note AN022 *Crystal Frequency Selection* for more details on the use of other crystal frequencies than 14.7456 MHz. The crystal frequency is used as reference for the data rate (as well as other internal functions) and in the 4 – 20 MHz range the frequencies 4.9152, 7.3728, 9.8304, 12.2880, 14.7456, 17.2032, 19.6608 MHz will give accurate data rates as shown in Table 5 and an IF-frequency of 307.2 kHz. The crystal frequency will influence the programming of the *CLOCK_A*, *CLOCK_B* and *MODEM* registers.

An external clock signal or the internal crystal oscillator can be used as main frequency reference. An external clock signal should be connected to XOSC_Q1, while XOSC_Q2 should be left open. The XOSC_BYPASS bit in the *INTERFACE* register should be set to '1' when an external digital rail-to-rail clock signal is used. No DC block should be used then. A sine with smaller amplitude can also be used. A DC blocking capacitor must then be used (10 nF) and the XOSC_BYPASS bit in the *INTERFACE* register should be set to '0'. For input signal amplitude, see "Electrical Specifications" on page 4.

Using the internal crystal oscillator, the crystal must be connected between the XOSC_Q1 and XOSC_Q2 pins. The oscillator is designed for parallel mode operation of the crystal. In addition, loading capacitors (C4 and C5) for the crystal are required. The loading capacitor values depend on the total load capacitance, C_L , specified for the crystal. The total load capacitance seen between the crystal terminals should equal C_L for

the crystal to oscillate at the specified frequency.

$$C_L = \frac{1}{\frac{1}{C_4} + \frac{1}{C_5}} + C_{\text{parasitic}}$$

The parasitic capacitance is constituted by pin input capacitance and PCB stray capacitance. Total parasitic capacitance is typically 8 pF. A trimming capacitor may be placed across C5 for initial tuning if necessary.

The crystal oscillator circuit is shown in Figure 34. Typical component values for different values of C_L are given in Table 11.

The crystal oscillator is amplitude regulated. This means that a high current is required to initiate the oscillations. When the amplitude builds up, the current is reduced to what is necessary to maintain approximately 600 mVpp amplitude. This ensures a fast start-up, keeps the drive level to a minimum and makes the oscillator insensitive to ESR variations. As long as the recommended load capacitance values are used, the ESR is not critical.

The initial tolerance, temperature drift, aging and load pulling should be carefully specified in order to meet the required frequency accuracy in a certain application. By specifying the *total* expected frequency accuracy in SmartRF[®] Studio together with data rate and frequency separation, the software will estimate the total bandwidth and compare to the available IF bandwidth. The software will report any contradictions and a more accurate crystal will be recommended if required.

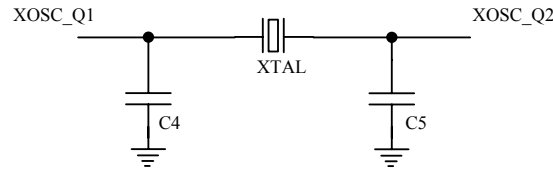


Figure 34. Crystal oscillator circuit

Item	$C_L = 12\text{ pF}$	$C_L = 16\text{ pF}$	$C_L = 22\text{ pF}$
C4	6.8 pF	18 pF	27 pF
C5	6.8 pF	18 pF	27 pF

Table 11. Crystal oscillator component values

Input / Output Matching

A few passive external components combined with the internal matching circuitry ensure match in both RX and TX mode. A recommended matching network is shown in Figure 35. Component values for various frequencies are given in Table 3. Component values for other frequencies can be found using the SmartRF® Studio software.

The use of an external T/R switch reduces current consumption in TX for high output power levels and improves the sensitivity in RX. A recommended application circuit is available from the Chipcon web site

(CC1020EMX). The external T/R switch can be omitted in certain applications but performance might then be degraded. Refer to Application Note *AN022 Crystal Frequency Selection* for more details.

The match can also be tuned by a shunt capacitor array at the PA output (RF_OUT). The capacitance can be set in 0.4 pF steps and used either in RX mode or TX mode. The *RX_MATCH[3:0]* and *TX_MATCH[3:0]* bits in the *MATCH* register control the capacitor array.

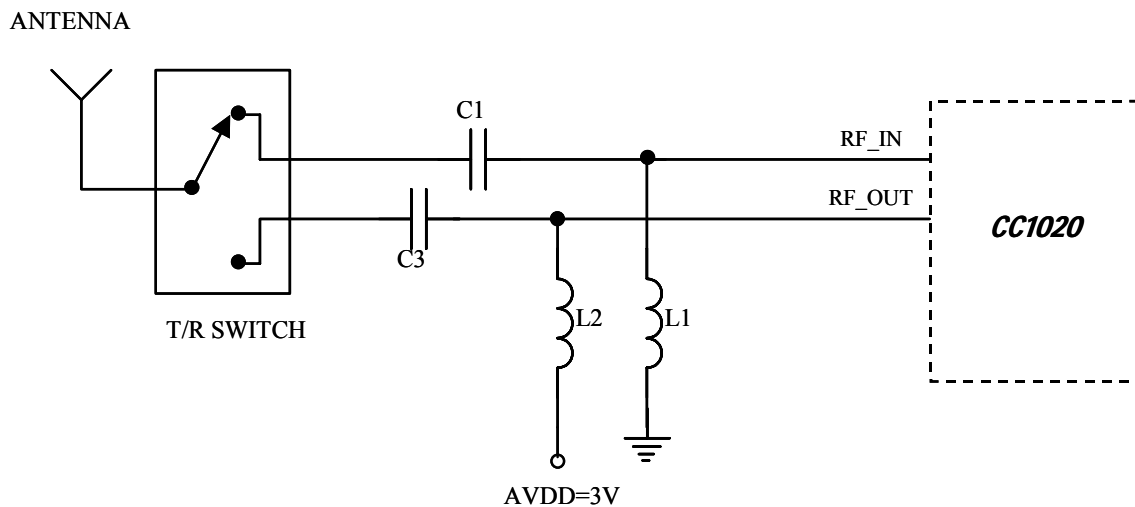


Figure 35. Input/output matching network

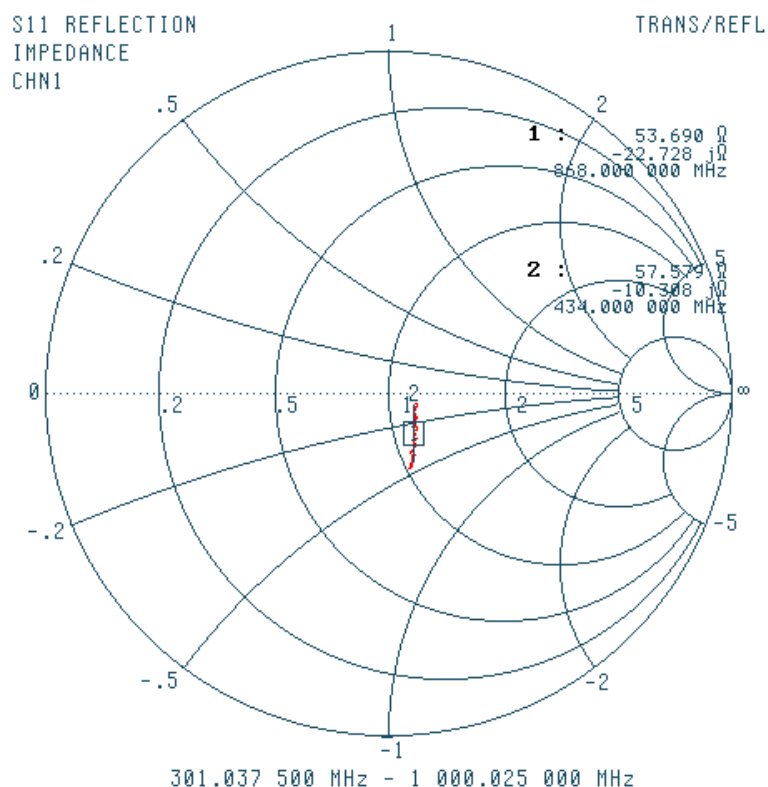


Figure 36. Typical LNA input impedance, 200 – 1000 MHz

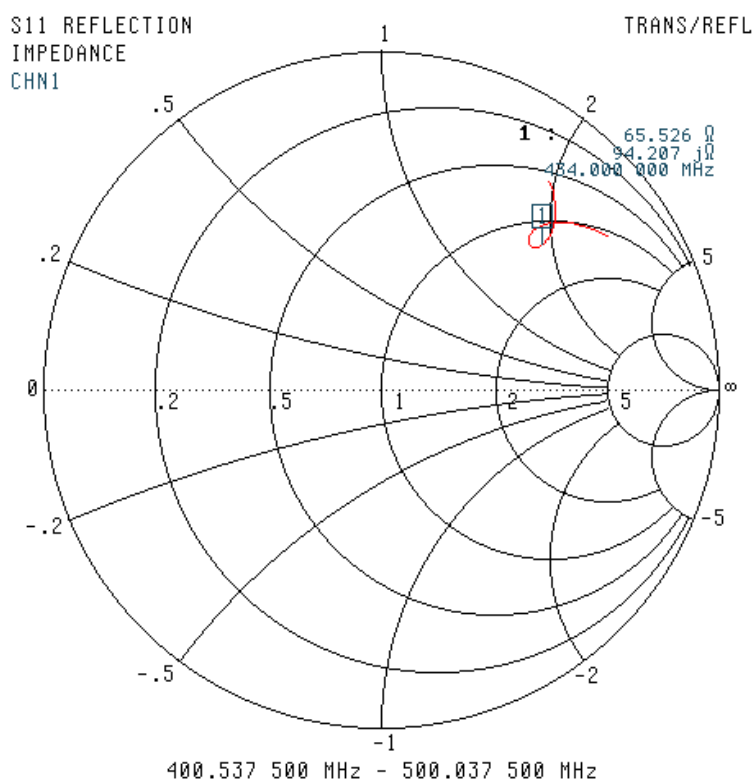


Figure 37. Typical optimum PA output impedance, 434 MHz

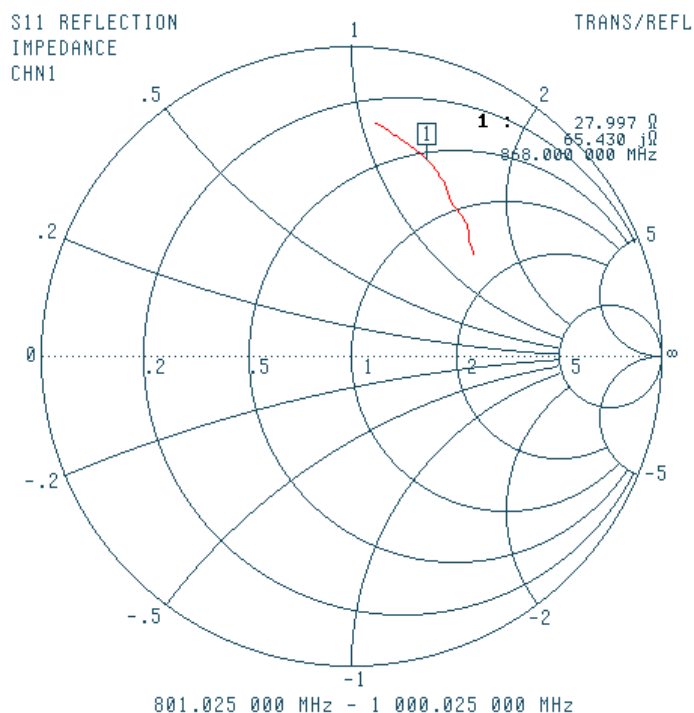


Figure 38. Typical optimum PA output impedance, 868 MHz

Optional LC Filter

An optional LC filter may be added between the antenna and the T/R switch in certain applications. The filter will reduce the emission of harmonics and increase the receiver selectivity.

An alternative is to insert the filter in the Tx-path only as shown in Figure 3. The filter will then reduce the emission of harmonics

A Pi-type filter topology is shown in Figure 39. The component values used for the **CC1020** reference designs are given in Table 12. The filter is designed for 50 Ω loads, e.g. an antenna. The component values have been tuned to compensate for

layout parasitics and non-ideal terminations.

If a standard Pi-type filter (such as the one used on the **CC1020** reference design and shown in Figure 39) is not sufficient to attenuate harmonics an alternative is to use a T-type LC filter. A T-type filter provides much better stop-band attenuation than a Pi-type filter due to improved insulation between input and output. For more details refer to Application Note *AN028 LC Filter with Improved High-Frequency Attenuation* available from the Chipcon web site.

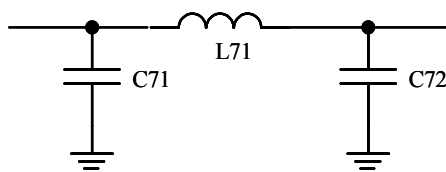


Figure 39. LC filter (Pi-type)

Item	433 MHz	868 MHz
C71	18 pF	8.2 pF
C72	18 pF	8.2 pF
L71	10 nH	5.1 nH

Table 12. LC filter component values for the application circuit in Figure 3

PA_EN and LNA_EN Pin Drive

Figure 40 gives the PA_EN and LNA_EN pins pin drive. The sink and source

currents have opposite signs but absolute values are used in Figure 40.

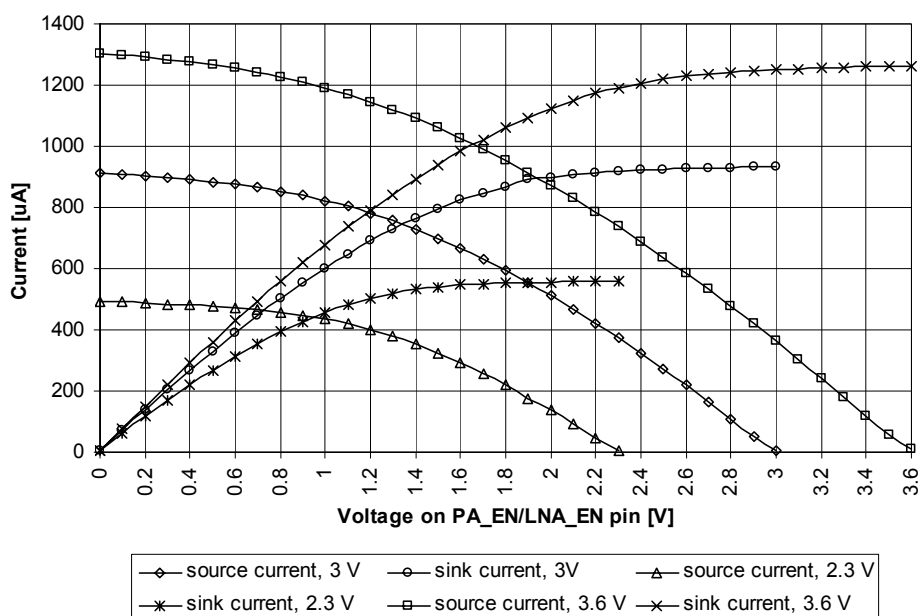


Figure 40. PA_EN and PA_EN pin drive

System Considerations and Guidelines

SRD regulations

International regulations and national laws regulate the use of radio receivers and transmitters. SRDs (Short Range Devices) for license free operation are allowed to operate in the 433 and 868 - 870 MHz bands in most European countries. In the United States, such devices operate in the 260 – 470 and 902 - 928 MHz bands. A summary of the most important aspects of these regulations can be found in Application Note *AN001 SRD regulations for license free transceiver operation*, available from the Chipcon web site.

Narrow band systems

CC1020 is specifically designed for narrowband systems. The **CC1020** meets the strict requirements to ACP (Adjacent Channel Power) and occupied bandwidth for a narrowband transmitter.

For the receiver side, **CC1020** gives very good ACR (Adjacent Channel Rejection), image frequency suppression and blocking properties for channel widths down to 12.5 kHz.

Such narrowband performance normally requires the use of external ceramic filters.

The **CC1020** provides this performance as a true single-chip solution with integrated IF filters.

Japan and Korea have allocated several frequency bands at 424, 426, 429, 449 and 469 MHz for narrowband license free operation. **CC1020** is designed to meet the requirements for operation in all these bands, including the strict requirements for narrowband operation down to 12.5 kHz channel width.

Due to on-chip complex filtering, the image frequency is removed. An on-chip calibration circuit is used to get the best possible image rejection. A narrowband preselector filter is not necessary to achieve image rejection.

A unique feature in **CC1020** is the very fine frequency resolution. This can be used for temperature compensation of the crystal if the temperature drift curve is known and a temperature sensor is included in the system. Even initial adjustment can be performed using the frequency programmability. This eliminates the need for an expensive TCXO and trimming in some applications.

In less demanding applications, a crystal with low temperature drift and low aging could be used without further compensation. A trimmer capacitor in the crystal oscillator circuit (in parallel with C5) could be used to set the initial frequency accurately.

The frequency offset between a transmitter and receiver is measured in the **CC1020** and can be read back from the **AFC** register. The measured frequency offset can be used to calibrate the receiver frequency using the transmitter as the reference.

CC1020 also has the possibility to use Gaussian shaped FSK (GFSK). This spectrum-shaping feature improves adjacent channel power (ACP) and occupied bandwidth. In 'true' FSK systems with abrupt frequency shifting, the spectrum is inherently broad. By making the frequency shift 'softer', the spectrum can be made significantly narrower. Thus,

higher data rates can be transmitted in the same bandwidth using GFSK.

Low cost systems

As the **CC1020** provide true narrowband multi-channel performance without any external filters, a very low cost high performance system can be achieved.

The oscillator crystal can then be a low cost crystal with 50 ppm frequency tolerance using the on-chip frequency tuning possibilities.

Battery operated systems

In low power applications, the power down mode should be used when not being active. Depending on the start-up time requirement, the oscillator core can be powered during power down. See page 48 for information on how effective power management can be implemented.

High reliability systems

Using a SAW filter as a preselector will improve the communication reliability in harsh environments by reducing the probability of blocking. The receiver sensitivity and the output power will be reduced due to the filter insertion loss. By inserting the filter in the RX path only, together with an external RX/TX switch, only the receiver sensitivity is reduced and output power is remained. The **PA_EN** and **LNA_EN** pin can be configured to control an external LNA, RX/TX switch or power amplifier. This is controlled by the **INTERFACE** register.

Frequency hopping spread spectrum systems (FHSS)

Due to the very fast frequency shift properties of the PLL, the **CC1020** is also very suitable for frequency hopping systems. Hop rates of 1-100 hops/s are commonly used depending on the bit rate and the amount of data to be sent during each transmission. The two frequency registers (**FREQ_A** and **FREQ_B**) are designed such that the 'next' frequency can be programmed while the 'present' frequency is used. The switching between the two frequencies is done through the **MAIN** register. Several features have been included to do the hopping without a need to re-synchronize the receiver. For more details refer to Application Note **AN014**

Frequency Hopping Systems available from the Chipcon web site.

In order to implement a frequency hopping system with **CC1020** do the following:

Set the desired frequency, calibrate and store the following register settings in non-volatile memory:

*STATUS1[3:0]: CHP_CURRENT[3:0]
STATUS2[4:0]: VCO_ARRAY[4:0]
STATUS3[5:0]: VCO_CAL_CURRENT[5:0]*

Repeat the calibration for each desired frequency. *VCO_CAL_CURRENT[5:0]* is not dependent on the RF frequency and

the same value can be used for all frequencies.

When performing frequency hopping, write the stored values to the corresponding *TEST1*, *TEST2* and *TEST3* registers, and enable override:

*TEST1[3:0]: CHP_CO[3:0]
TEST2[4:0]: VCO_AO[4:0]
TEST2[5]: VCO_OVERRIDE
TEST2[6]: CHP_OVERRIDE
TEST3[5:0]: VCO_CO[5:0]
TEST3[6]: VCO_CAL_OVERRIDE*

PCB Layout Recommendations

A four layer PCB is highly recommended. The second layer of the PCB should be the "ground-layer".

The top layer should be used for signal routing, and the open areas should be filled with metallisation connected to ground using several vias.

The area under the chip is used for grounding and must be connected to the bottom ground plane with several vias. In the Chipcon reference designs we have placed 9 vias inside the exposed die attached pad. These vias should be "tented" (covered with solder mask) on the component side of the PCB to avoid migration of solder through the vias during the solder reflow process.

Each decoupling capacitor should be placed as close as possible to the supply pin it is supposed to decouple. Each decoupling capacitor should be connected to the power (-plane) by separate vias. The best routing is from the power (-plane) to the decoupling capacitor and then to the

CC1020 supply pin. Supply power filtering is very important, especially for the VCO supply (pin 23).

A separate via to the ground plane connected to the ground pad on the other side of the decoupling capacitor should be used. Direct connections between neighboring power pins will increase noise coupling and should be avoided, unless absolutely necessary.

The external components should ideally be as small as possible and surface mount devices are highly recommended.

Precaution should be used when placing the microcontroller in order to avoid noise interfering with the RF circuitry.

A CC1020/1070DK Development Kit with a fully assembled CC1020EMX Evaluation Module is available. It is strongly advised that this reference layout is followed very closely in order to get the best performance. The layout Gerber files are available from the Chipcon web site.

Antenna Considerations

CC1020 can be used together with various types of antennas. The most common antennas for short-range communication are monopole, helical and loop antennas.

Monopole antennas are resonant antennas with a length corresponding to one quarter of the electrical wavelength ($\lambda/4$). They are very easy to design and can be implemented simply as a “piece of wire” or even integrated onto the PCB.

Non-resonant monopole antennas shorter than $\lambda/4$ can also be used, but at the expense of range. In size and cost critical applications such an antenna may very well be integrated onto the PCB.

Helical antennas can be thought of as a combination of a monopole and a loop antenna. They are a good compromise in size critical applications. But helical antennas tend to be more difficult to optimize than the simple monopole.

Loop antennas are easy to integrate into the PCB, but are less effective due to

difficult impedance matching because of their very low radiation resistance.

For low power applications the $\lambda/4$ -monopole antenna is recommended due to its simplicity as well as providing the best range.

The length of the $\lambda/4$ -monopole antenna is given by:

$$L = 7125 / f$$

where f is in MHz, giving the length in cm. An antenna for 869 MHz should be 8.2 cm, and 16.4 cm for 434 MHz.

The antenna should be connected as close as possible to the IC. If the antenna is located away from the input pin the antenna should be matched to the feeding transmission line (50 Ω).

For a more thorough background on antennas, please refer to Application Note *AN003 SRD Antennas* available from the Chipcon web site.

Configuration Registers

The configuration of **CC1020** is done by programming the 8-bit configuration registers. The configuration data based on selected system parameters are most easily found by using the SmartRF[®] Studio software. Complete descriptions of the

registers are given in the following tables. After a RESET is programmed, all the registers have default values. The *TEST* registers also get default values after a RESET, and should not be altered by the user.

CC1020 Register Overview

ADDRESS	Byte Name	Description
00h	MAIN	Main control register
01h	INTERFACE	Interface control register
02h	RESET	Digital module reset register
03h	SEQUENCING	Automatic power-up sequencing control register
04h	FREQ_2A	Frequency register 2A
05h	FREQ_1A	Frequency register 1A
06h	FREQ_0A	Frequency register 0A
07h	CLOCK_A	Clock generation register A
08h	FREQ_2B	Frequency register 2B
09h	FREQ_1B	Frequency register 1B
0Ah	FREQ_0B	Frequency register 0B
0Bh	CLOCK_B	Clock generation register B
0Ch	VCO	VCO current control register
0Dh	MODEM	Modem control register
0Eh	DEVIATION	TX frequency deviation register
0Fh	AFC_CONTROL	RX AFC control register
10h	FILTER	Channel filter / RSSI control register
11h	VGA1	VGA control register 1
12h	VGA2	VGA control register 2
13h	VGA3	VGA control register 3
14h	VGA4	VGA control register 4
15h	LOCK	Lock control register
16h	FRONTEND	Front end bias current control register
17h	ANALOG	Analogue modules control register
18h	BUFF_SWING	LO buffer and prescaler swing control register
19h	BUFF_CURRENT	LO buffer and prescaler bias current control register
1Ah	PLL_BW	PLL loop bandwidth / charge pump current control register
1Bh	CALIBRATE	PLL calibration control register
1Ch	PA_POWER	Power amplifier output power register
1Dh	MATCH	Match capacitor array control register, for RX and TX impedance matching
1Eh	PHASE_COMP	Phase error compensation control register for LO I/Q
1Fh	GAIN_COMP	Gain error compensation control register for mixer I/Q
20h	POWERDOWN	Power-down control register
21h	TEST1	Test register for overriding PLL calibration
22h	TEST2	Test register for overriding PLL calibration
23h	TEST3	Test register for overriding PLL calibration
24h	TEST4	Test register for charge pump and IF chain testing
25h	TEST5	Test register for ADC testing
26h	TEST6	Test register for VGA testing
27h	TEST7	Test register for VGA testing
40h	STATUS	Status information register (PLL lock, RSSI, calibration ready, etc.)
41h	RESET_DONE	Status register for digital module reset
42h	RSSI	Received signal strength register
43h	AFC	Average received frequency deviation from IF (can be used for AFC)
44h	GAUSS_FILTER	Digital FM demodulator register
45h	STATUS1	Status of PLL calibration results etc. (test only)
46h	STATUS2	Status of PLL calibration results etc. (test only)
47h	STATUS3	Status of PLL calibration results etc. (test only)
48h	STATUS4	Status of ADC signals (test only)
49h	STATUS5	Status of channel filter "I" signal (test only)
4Ah	STATUS6	Status of channel filter "Q" signal (test only)
4Bh	STATUS7	Status of AGC (test only)

MAIN Register (00h)

REGISTER	NAME	Default value	Active	Description
MAIN[7]	RXTX	-	-	RX/TX switch, 0: RX , 1: TX
MAIN[6]	F_REG	-	-	Selection of Frequency Register, 0: Register A, 1: Register B
MAIN[5:4]	PD_MODE[1:0]	-	-	Power down mode 0 (00): Receive Chain in power-down in TX, PA in power-down in RX 1 (01): Receive Chain and PA in power-down in both TX and RX 2 (10): Individual modules can be put in power-down by programming the POWERDOWN register 3 (11): Automatic power-up sequencing is activated (see below)
MAIN[3]	FS_PD	-	H	Power Down of Frequency Synthesizer
MAIN[2]	XOSC_PD	-	H	Power Down of Crystal Oscillator Core
MAIN[1]	BIAS_PD	-	H	Power Down of BIAS (Global Current Generator) and Crystal Oscillator Buffer
MAIN[0]	RESET_N	-	L	Reset, active low. Writing RESET_N low will write default values to all other registers than MAIN. Bits in MAIN do not have a default value, and will be written directly through the configuration interface. Must be set high to complete reset.

MAIN Register (00h) when using automatic power-up sequencing (RXTX = 0, PD_MODE[1:0] = 11)

REGISTER	NAME	Default value	Active	Description
MAIN[7]	RXTX	-	-	Automatic power-up sequencing only works in RX (RXTX=0)
MAIN[6]	F_REG	-	-	Selection of Frequency Register, 0: Register A, 1: Register B
MAIN[5:4]	PD_MODE[1:0]	-	H	Set PD_MODE[1:0]=3 (11) to enable sequencing
MAIN[3:2]	SEQ_CAL[1:0]	-	-	Controls PLL calibration before re-entering power-down 0: Never perform PLL calibration as part of sequence 1: Always perform PLL calibration at end of sequence 2: Perform PLL calibration at end of every 16 th sequence 3: Perform PLL calibration at end of every 256 th sequence
MAIN[1]	SEQ_PD	-	↑	↑1: Put the chip in power down and wait for start of new power-up sequence
MAIN[0]	RESET_N	-	L	Reset, active low. Writing RESET_N low will write default values to all other registers than MAIN. Bits in MAIN do not have a default value, and will be written directly through the configuration interface. Must be set high to complete reset.

INTERFACE Register (01h)

REGISTER	NAME	Default value	Active	Description
INTERFACE[7]	XOSC_BYPASS	0	H	Bypass internal crystal oscillator, use external clock 0: Internal crystal oscillator is used, or external sine wave fed through a coupling capacitor 1: Internal crystal oscillator in power down, external clock with rail-to-rail swing is used
INTERFACE[6]	SEP_DI_DO	0	H	Use separate pin for RX data output 0: DIO is data output in RX and data input in TX. LOCK pin is available (Normal operation). 1: DIO is always input, and a separate pin is used for RX data output (synchronous mode: LOCK pin, asynchronous mode: DCLK pin). If SEP_DI_DO=1 and SEQ_PSEL=0 in SEQUENCING register, then negative transitions on DIO is used to start power-up sequencing when PD_MODE=3 (power-up sequencing is enabled).
INTERFACE[5]	DCLK_LOCK	0	H	Gate DCLK signal with PLL lock signal in synchronous mode Only applies when PD_MODE = "01" 0: DCLK is always 0 1: DCLK is always 1 unless PLL is in lock
INTERFACE[4]	DCLK_CS	0	H	Gate DCLK signal with carrier sense indicator in synchronous mode Use when receive chain is active (in power-up) Always set to 0 in Tx mode. 0: DCLK is independent of carrier sense indicator. 1: DCLK is always 1 unless carrier sense is indicated
INTERFACE[3]	EXT_PA	0	H	Use PA_EN pin to control external PA 0: PA_EN pin always equals EXT_PA_POL bit 1: PA_EN pin is asserted when internal PA is turned on
INTERFACE[2]	EXT_LNA	0	H	Use LNA_EN pin to control external LNA 0: LNA_EN pin always equals EXT_LNA_POL bit 1: LNA_EN pin is asserted when internal LNA is turned on
INTERFACE[1]	EXT_PA_POL	0	H	Polarity of external PA control 0: PA_EN pin is "0" when activating external PA 1: PA_EN pin is "1" when activating external PA
INTERFACE[0]	EXT_LNA_POL	0	H	Polarity of external LNA control 0: LNA_EN pin is "0" when activating external LNA 1: LNA_EN pin is "1" when activating external LNA

Note: If TF_ENABLE=1 or TA_ENABLE=1 in TEST4 register, then INTERFACE[3:0] controls analogue test module: INTERFACE[3] = TEST_PD, INTERFACE[2:0] = TEST_MODE[2:0]. Otherwise, TEST_PD=1 and TEST_MODE[2:0]=001.

RESET Register (02h)

REGISTER	NAME	Default value	Active	Description
RESET[7]	ADC_RESET_N	0	L	Reset ADC control logic
RESET[6]	AGC_RESET_N	0	L	Reset AGC (VGA control) logic
RESET[5]	GAUSS_RESET_N	0	L	Reset Gaussian data filter
RESET[4]	AFC_RESET_N	0	L	Reset AFC / FSK decision level logic
RESET[3]	BITSYNC_RESET_N	0	L	Reset modulator, bit synchronization logic and PN9 PRBS generator
RESET[2]	SYNTH_RESET_N	0	L	Reset digital part of frequency synthesizer
RESET[1]	SEQ_RESET_N	0	L	Reset power-up sequencing logic
RESET[0]	CAL_LOCK_RESET_N	0	L	Reset calibration logic and lock detector

Note: For reset of CC1020 write RESET_N=0 in the MAIN register. The reset register should not be used during normal operation.

Bits in the RESET register are self-clearing (will be set to 1 when the reset operation starts). Relevant digital clocks must be running for the resetting to complete. After writing to the RESET register, the user should verify that all reset operations have been completed, by reading the RESET_DONE status register (41h) until all bits equal 1.

SEQUENCING Register (03h)

REGISTER	NAME	Default value	Active	Description
SEQUENCING[7]	SEQ_PSEL	1	H	Use PSEL pin to start sequencing 0: PSEL pin does not start sequencing. Negative transitions on DIO starts power-up sequencing if SEP_DI_DO=1. 1: Negative transitions on the PSEL pin will start power-up sequencing
SEQUENCING[6:4]	RX_WAIT[2:0]	0	-	Waiting time from PLL enters lock until RX power-up 0: Wait for approx. 32 ADC_CLK periods (26 µs) 1: Wait for approx. 44 ADC_CLK periods (36 µs) 2: Wait for approx. 64 ADC_CLK periods (52 µs) 3: Wait for approx. 88 ADC_CLK periods (72 µs) 4: Wait for approx. 128 ADC_CLK periods (104 µs) 5: Wait for approx. 176 ADC_CLK periods (143 µs) 6: Wait for approx. 256 ADC_CLK periods (208 µs) 7: No additional waiting time before RX power-up
SEQUENCING[3:0]	CS_WAIT[3:0]	10	-	Waiting time for carrier sense from RX power-up 0: Wait 20 FILTER_CLK periods before power down 1: Wait 22 FILTER_CLK periods before power down 2: Wait 24 FILTER_CLK periods before power down 3: Wait 26 FILTER_CLK periods before power down 4: Wait 28 FILTER_CLK periods before power down 5: Wait 30 FILTER_CLK periods before power down 6: Wait 32 FILTER_CLK periods before power down 7: Wait 36 FILTER_CLK periods before power down 8: Wait 40 FILTER_CLK periods before power down 9: Wait 44 FILTER_CLK periods before power down 10: Wait 48 FILTER_CLK periods before power down 11: Wait 52 FILTER_CLK periods before power down 12: Wait 56 FILTER_CLK periods before power down 13: Wait 60 FILTER_CLK periods before power down 14: Wait 64 FILTER_CLK periods before power down 15: Wait 72 FILTER_CLK periods before power down

FREQ_2A Register (04h)

REGISTER	NAME	Default value	Active	Description
FREQ_2A[7:0]	FREQ_A[22:15]	131	-	8 MSB of frequency control word A

FREQ_1A Register (05h)

REGISTER	NAME	Default value	Active	Description
FREQ_1A[7:0]	FREQ_A[14:7]	177	-	Bit 15 to 8 of frequency control word A

FREQ_0A Register (06h)

REGISTER	NAME	Default value	Active	Description
FREQ_0A[7:1]	FREQ_A[6:0]	124	-	7 LSB of frequency control word A
FREQ_0A[0]	DITHER_A	1	H	Enable dithering for frequency A

CLOCK_A Register (07h)

REGISTER	NAME	Default value	Active	Description
CLOCK_A[7:5]	REF_DIV_A[2:0]	2	-	Reference frequency divisor (A): 0: Not supported 1: REF_CLK frequency = Crystal frequency / 2 ... 7: REF_CLK frequency = Crystal frequency / 8 It is recommended to use the highest possible reference clock frequency that allows the desired Baud rate.
CLOCK_A[4:2]	MCLK_DIV1_A[2:0]	4	-	Modem clock divider 1 (A): 0: Divide by 2.5 1: Divide by 3 2: Divide by 4 3: Divide by 7.5 (2.5·3) 4: Divide by 12.5 (2.5·5) 5: Divide by 40 (2.5·16) 6: Divide by 48 (3·16) 7: Divide by 64 (4·16)
CLOCK_A[1:0]	MCLK_DIV2_A[1:0]	0	-	Modem clock divider 2 (A): 0: Divide by 1 1: Divide by 2 2: Divide by 4 3: Divide by 8 MODEM_CLK frequency is FREF frequency, divided by the product of divider 1 and divider 2. Baud rate is MODEM_CLK frequency divided by 8.

FREQ_2B Register (08h)

REGISTER	NAME	Default value	Active	Description
FREQ_2B[7:0]	FREQ_B[22:15]	131	-	8 MSB of frequency control word B

FREQ_1B Register (09h)

REGISTER	NAME	Default value	Active	Description
FREQ_1B[7:0]	FREQ_B[14:7]	189	-	Bit 15 to 8 of frequency control word B

FREQ_0B Register (0Ah)

REGISTER	NAME	Default value	Active	Description
FREQ_0B[7:1]	FREQ_B[6:0]	124	-	7 LSB of frequency control word B
FREQ_0B[0]	DITHER_B	1	H	Enable dithering for frequency B

CLOCK_B Register (0Bh)

REGISTER	NAME	Default value	Active	Description
CLOCK_B[7:5]	REF_DIV_B[2:0]	2	-	Reference frequency divisor (B): 0: Not supported 1: REF_CLK frequency = Crystal frequency / 2 ... 7: REF_CLK frequency = Crystal frequency / 8
CLOCK_B[4:2]	MCLK_DIV1_B[2:0]	4	-	Modem clock divider 1 (B): 0: Divide by 2.5 1: Divide by 3 2: Divide by 4 3: Divide by 7.5 (2.5·3) 4: Divide by 12.5 (2.5·5) 5: Divide by 40 (2.5·16) 6: Divide by 48 (3·16) 7: Divide by 64 (4·16)
CLOCK_B[1:0]	MCLK_DIV2_B[1:0]	0	-	Modem clock divider 2 (B): 0: Divide by 1 1: Divide by 2 2: Divide by 4 3: Divide by 8 MODEM_CLK frequency is FREF frequency, divided by the product of divider 1 and divider 2. Baud rate is MODEM_CLK frequency divided by 8.

VCO Register (0Ch)

REGISTER	NAME	Default value	Active	Description
VCO[7:4]	VCO_CURRENT_A[3:0]	8	-	Control of current in VCO core for frequency A 0: 1.4 mA current in VCO core 1: 1.8 mA current in VCO core 2: 2.1 mA current in VCO core 3: 2.5 mA current in VCO core 4: 2.8 mA current in VCO core 5: 3.2 mA current in VCO core 6: 3.5 mA current in VCO core 7: 3.9 mA current in VCO core 8: 4.2 mA current in VCO core 9: 4.6 mA current in VCO core 10: 4.9 mA current in VCO core 11: 5.3 mA current in VCO core 12: 5.6 mA current in VCO core 13: 6.0 mA current in VCO core 14: 6.4 mA current in VCO core 15: 6.7 mA current in VCO core Recommended setting: VCO_CURRENT_A=4
VCO[3:0]	VCO_CURRENT_B[3:0]	8	-	Control of current in VCO core for frequency B The current steps are the same as for VCO_CURRENT_A Recommended setting: VCO_CURRENT_B=4

MODEM Register (0Dh)

REGISTER	NAME	Default value	Active	Description
MODEM[7]	-	0	-	Reserved, write 0
MODEM[6:4]	ADC_DIV[2:0]	3	-	<p>ADC clock divisor</p> <p>0: Not supported 1: ADC frequency = XOSC frequency / 4 2: ADC frequency = XOSC frequency / 6 3: ADC frequency = XOSC frequency / 8 4: ADC frequency = XOSC frequency / 10 5: ADC frequency = XOSC frequency / 12 6: ADC frequency = XOSC frequency / 14 7: ADC frequency = XOSC frequency / 16</p> <p>Note that the intermediate frequency should be as close to 307.2 kHz as possible. ADC clock frequency is always 4 times the intermediate frequency, and should therefore be as close to 1.2288 MHz as possible.</p>
MODEM[3]	-	0	-	Reserved, write 0
MODEM[2]	PN9_ENABLE	0	H	<p>Enable scrambling of TX and RX with PN9 pseudo-random bit sequence</p> <p>0: PN9 scrambling is disabled 1: PN9 scrambling is enabled ($x^9 + x^5 + 1$)</p> <p>The PN9 pseudo-random bit sequence can be used for BER testing by only transmitting zeros, and then counting the number of received ones.</p>
MODEM[1:0]	DATA_FORMAT[1:0]	0	-	<p>Modem data format</p> <p>0 (00): NRZ operation 1 (01): Manchester operation 2 (10): Transparent asynchronous UART operation, set DCLK=0 3 (11): Transparent asynchronous UART operation, set DCLK=1</p>

DEVIATION Register (0Eh)

REGISTER	NAME	Default value	Active	Description
DEVIATION[7]	TX_SHAPING	1	H	Enable Gaussian shaping of transmitted data Recommended setting: TX_SHAPING=1
DEVIATION[6:4]	TXDEV_X[2:0]	6	-	Transmit frequency deviation exponent
DEVIATION [3:0]	TXDEV_M[3:0]	8	-	<p>Transmit frequency deviation mantissa</p> <p>Deviation in 402-470 MHz band: $F_{REF} \cdot TXDEV_M \cdot 2^{(TXDEV_X-16)}$</p> <p>Deviation in 804-940 MHz band: $F_{REF} \cdot TXDEV_M \cdot 2^{(TXDEV_X-15)}$</p> <p>On-off-keying (ASK) is used in RX/TX if TXDEV_M[3:0]=0</p> <p>To find TXDEV_M given the deviation and TXDEV_X:</p> <p>$TXDEV_M = deviation \cdot 2^{(16-TXDEV_X)} / F_{REF}$ in 402-470 MHz band,</p> <p>$TXDEV_M = deviation \cdot 2^{(15-TXDEV_X)} / F_{REF}$ in 804-940 MHz band.</p> <p>Decrease TXDEV_X and try again if TXDEV_M < 8. Increase TXDEV_X and try again if TXDEV_M ≥ 16.</p>

AFC_CONTROL Register (0Fh)

REGISTER	NAME	Default value	Active	Description
AFC_CONTROL[7:6]	SETTLING[1:0]	2	-	Controls AFC settling time versus accuracy 0: AFC off; zero average frequency is used in demodulator 1: Fastest settling; frequency averaged over 1 0/1 bit pair 2: Medium settling; frequency averaged over 2 0/1 bit pairs 3: Slowest settling; frequency averaged over 4 0/1 bit pairs Recommended setting: AFC_CONTROL=3 for higher accuracy unless it is essential to have the fastest settling time when transmission starts after RX is activated.
AFC_CONTROL[5:4]	RXDEV_X[1:0]	1	-	RX frequency deviation exponent
AFC_CONTROL[3:0]	RXDEV_M[3:0]	12	-	RX frequency deviation mantissa Expected RX deviation should be: $Baud\ rate \cdot RXDEV_M \cdot 2^{(RXDEV_X-3)} / 3$ To find RXDEV_M given the deviation and RXDEV_X: $RXDEV_M = 3 \cdot deviation \cdot 2^{(3-RXDEV_X)} / Baud\ rate$ Decrease RXDEV_X and try again if RXDEV_M < 8. Increase RXDEV_X and try again if RXDEV_M ≥ 16.

Note: The Rx frequency deviation should be close to half the Tx frequency deviation

FILTER Register (10h)

REGISTER	NAME	Default value	Active	Description
FILTER[7]	FILTER_BYPASS	0	H	Bypass analogue image rejection / anti-alias filter. Set to 1 for increased dynamic range at high Baud rates. Recommended setting: FILTER_BYPASS=0 below 76.8 kBaud, FILTER_BYPASS=1 for 76.8 kBaud and up.
FILTER[6:5]	DEC_SHIFT[1:0]	0	-	Number of extra bits to shift decimator input (may improve filter accuracy and lower power consumption). Recommended settings: DEC_SHIFT=0 when DEC_DIV ≤ 1 (receiver channel bandwidth ≥ 153.6 kHz), DEC_SHIFT=1 when optimized sensitivity and 1 < DEC_DIV < 24 (12.29 kHz < receiver channel bandwidth < 153.6 kHz), DEC_SHIFT=2 when optimized selectivity and DEC_DIV ≥ 24 (receiver channel bandwidth ≤ 12.29 kHz)
FILTER[4:0]	DEC_DIV[4:0]	0	-	Decimation clock divisor 0: Decimation clock divisor = 1, 307.2 kHz IF filter bandwidth. 1: Decimation clock divisor = 2, 153.6 kHz IF filter bandwidth. ... 30: Decimation clock divisor = 31, 9.91 kHz IF filter bandwidth. 31: Decimation clock divisor = 32, 9.6 kHz IF filter bandwidth. Channel (IF) filter bandwidth is 307.2 kHz divided by the decimation clock divisor.

VGA1 Register (11h)

REGISTER	NAME	Default value	Active	Description
VGA1[7:6]	CS_SET[1:0]	1	-	<p>Sets the number of consecutive samples at or above carrier sense level before carrier sense is indicated (e.g. on LOCK pin)</p> <p>0: Set carrier sense after first sample at or above carrier sense level</p> <p>1: Set carrier sense after second sample at or above carrier sense level</p> <p>2: Set carrier sense after third sample at or above carrier sense level</p> <p>3: Set carrier sense after fourth sample at or above carrier sense level</p> <p>Increasing CS_SET reduces the number of "false" carrier sense events due to noise, at the expense of increased carrier sense response time.</p>
VGA1[5]	CS_RESET	1	-	<p>Sets the number of consecutive samples below carrier sense level before carrier sense indication (e.g. on lock pin) is reset</p> <p>0: Carrier sense is reset after first sample below carrier sense level</p> <p>1: Carrier sense is reset after second sample below carrier sense level</p> <p>Recommended setting: CS_RESET=1, in order to reduce the chance of losing carrier sense due to noise.</p>
VGA1[4:2]	VGA_WAIT[2:0]	1	-	<p>Controls how long AGC, bit synchronization, AFC and RSSI levels are frozen after VGA gain is changed, when frequency is changed between A and B, or PLL has been out of lock, or after RX power-up</p> <p>0: Freeze operation for 16 filter clocks, 8/(filter BW) seconds</p> <p>1: Freeze operation for 20 filter clocks, 10/(filter BW) seconds</p> <p>2: Freeze operation for 24 filter clocks, 12/(filter BW) seconds</p> <p>3: Freeze operation for 28 filter clocks, 14/(filter BW) seconds</p> <p>4: Freeze operation for 32 filter clocks, 16/(filter BW) seconds</p> <p>5: Freeze operation for 40 filter clocks, 20/(filter BW) seconds</p> <p>6: Freeze operation for 48 filter clocks, 24/(filter BW) seconds</p> <p>7: Freeze present levels unconditionally</p>
VGA1[1:0]	VGA_FREEZE[1:0]	1	-	<p>Controls the additional time AGC, bit synchronization, AFC and RSSI levels are frozen when frequency is changed between A and B, or PLL has been out of lock, or after RX power-up</p> <p>0: Freeze levels for approx. 16 ADC_CLK periods (13 µs)</p> <p>1: Freeze levels for approx. 32 ADC_CLK periods (26 µs)</p> <p>2: Freeze levels for approx. 64 ADC_CLK periods (52 µs)</p> <p>3: Freeze levels for approx. 128 ADC_CLK periods (104 µs)</p>

VGA2 Register (12h)

REGISTER	NAME	Default value	Active	Description
VGA2[7]	LNA2_MIN	0	-	Minimum LNA2 setting used in VGA 0: Minimum LNA2 gain 1: Medium LNA2 gain Recommended setting: LNA2_MIN=0 for best selectivity.
VGA2[6]	LNA2_MAX	1	-	Maximum LNA2 setting used in VGA 0: Medium LNA2 gain 1: Maximum LNA2 gain Recommended setting: LNA2_MAX=1 for best sensitivity.
VGA2[5:4]	LNA2_SETTING[1:0]	3	-	Selects at what VGA setting the LNA gain should be changed 0: Apply LNA2 change below min. VGA setting. 1: Apply LNA2 change at approx. 1/3 VGA setting (around VGA setting 10). 2: Apply LNA2 change at approx. 2/3 VGA setting (around VGA setting 19). 3: Apply LNA2 change above max. VGA setting. Recommended setting: LNA2_SETTING=0 if VGA_SETTING<10, LNA2_SETTING=1 otherwise. If LNA2_MIN=1 and LNA2_MAX=0, then the LNA2 setting is controlled by LNA2_SETTING: 0: Between medium and maximum LNA2 gain 1: Minimum LNA2 gain 2: Medium LNA2 gain 3: Maximum LNA2 gain
VGA2[3]	AGC_DISABLE	0	H	Disable AGC 0: AGC is enabled 1: AGC is disabled (VGA_SETTING determines VGA gain) Recommended setting: AGC_DISABLE=0 for good dynamic range.
VGA2[2]	AGC_HYSTERESIS	1	H	Enable AGC hysteresis 0: No hysteresis. Immediate gain change for smallest up/down step 1: Hysteresis enabled. Two samples in a row must indicate gain change for smallest up/down step Recommended setting: AGC_HYSTERESIS=1.
VGA2[1:0]	AGC_AVG[1:0]	1	-	Sets how many samples that are used to calculate average output magnitude for AGC/RSSI. 0: Magnitude is averaged over 2 filter output samples 1: Magnitude is averaged over 4 filter output samples 2: Magnitude is averaged over 8 filter output samples 3: Magnitude is averaged over 16 filter output samples Recommended setting: AGC_AVG=1. For best AGC/RSSI accuracy AGC_AVG=3. For automatic power-up sequencing, the AGC_AVG and RSSI_SET values must be chosen so that carrier sense is available in time to be detected before the chip re-enters power-down.

VGA3 Register (13h)

REGISTER	NAME	Default value	Active	Description
VGA3[7:5]	VGA_DOWN[2:0]	1	-	Decides how much the signal strength must be above CS_LEVEL+VGA_UP before VGA gain is decreased. 0: Gain is decreased 4.5 dB above CS_LEVEL+VGA_UP 1: Gain is decreased 6 dB above CS_LEVEL+VGA_UP ... 6: Gain is decreased 13.5 dB above CS_LEVEL+VGA_UP 7: Gain is decreased 15 dB above CS_LEVEL+VGA_UP See Figure 21 on page 36 for an explanation of the relationship between RSSI, AGC and carrier sense settings.
VGA3[4:0]	VGA_SETTING[4:0]	24	H	VGA setting to be used when receive chain is turned on This is also the maximum gain that the AGC is allowed to use. See Figure 21 on page 36 for an explanation of the relationship between RSSI, AGC and carrier sense settings.

VGA4 Register (14h)

REGISTER	NAME	Default value	Active	Description
VGA4[7:5]	VGA_UP[2:0]	1	-	Decides the level where VGA gain is increased if it is not already at the maximum set by VGA_SETTING. 0: Gain is increased when signal is below CS_LEVEL 1: Gain is increased when signal is below CS_LEVEL+1.5 dB ... 6: Gain is increased when signal is below CS_LEVEL+9 dB 7: Gain is increased when signal below CS_LEVEL+10.5 dB See Figure 21 on page 36 for an explanation of the relationship between RSSI, AGC and carrier sense settings.
VGA4[4:0]	CS_LEVEL[4:0]	24	H	Reference level for Received Signal Strength Indication (carrier sense level) and AGC. See page 32 and Figure 21 on page 36 for an explanation of the relationship between RSSI, AGC and carrier sense settings.

LOCK Register (15h)

REGISTER	NAME	Default value	Active	Description
LOCK[7:4]	LOCK_SELECT[3:0]	0	-	Selection of signals to LOCK pin 0: Set to 0 1: Set to 1 2: LOCK_CONTINUOUS (active low) 3: LOCK_INSTANT (active low) 4: CARRIER_SENSE (RSSI above threshold, active low) 5: CAL_COMPLETE (active low) 6: SEQ_ERROR (active low) 7: FXOSC 8: REF_CLK 9: FILTER_CLK 10: DEC_CLK 11: PRE_CLK 12: DS_CLK 13: MODEM_CLK 14: VCO_CAL_COMP 15: F_COMP
LOCK[3]	WINDOW_WIDTH	0	-	Selects lock window width 0: Lock window is 2 prescaler clock cycles wide 1: Lock window is 4 prescaler clock cycles wide Recommended setting: WINDOW_WIDTH=0.
LOCK[2]	LOCK_MODE	0	-	Selects lock detector mode 0: Counter restart mode 1: Up/Down counter mode Recommended setting: LOCK_MODE=0.
LOCK[1:0]	LOCK_ACCURACY[1:0]	0	-	Selects lock accuracy (counter threshold values) 0: Declare lock at counter value 127, out of lock at value 111 1: Declare lock at counter value 255, out of lock at value 239 2: Declare lock at counter value 511, out of lock at value 495 3: Declare lock at counter value 1023, out of lock at value 1007 Recommended settings: LOCK_ACCURACY=2 for 12.5 kHz channels at 402-470 MHz / 25kHz channels at 804-940 MHz, LOCK_ACCURACY=1 for 25 kHz channels at 402-470 MHz / 50kHz channels at 804-940 MHz, LOCK_ACCURACY=0 otherwise.

Note: Set LOCK_SELECT=2 to use the LOCK pin as a lock indicator.

FRONTEND Register (16h)

REGISTER	NAME	Default value	Active	Description
FRONTEND[7:6]	LNAMIX_CURRENT[1:0]	2	-	Controls current in LNA, LNA2 and mixer 0: 1.7 mA nominal front-end current consumption 1: 2.2 mA nominal front-end current consumption 2: 2.7 mA nominal front-end current consumption 3: 3.2 mA nominal front-end current consumption Recommended setting: LNAMIX_CURRENT=1
FRONTEND[5:4]	LNA_CURRENT[1:0]	1	-	Controls current in the LNA 0: 0.72 mA LNA current with nom. LNAMIX_CURRENT 1: 0.94 mA LNA current with nom. LNAMIX_CURRENT 2: 1.39 mA LNA current with nom. LNAMIX_CURRENT 3: 2.26 mA LNA current with nom. LNAMIX_CURRENT Recommended setting: LNA_CURRENT=3. Can be lowered to save power, at the expense of reduced sensitivity.
FRONTEND[3]	MIX_CURRENT	0	-	Controls current in the mixer 0: 0.55 mA mixer current with nom. LNAMIX_CURRENT 1: 0.80 mA mixer current with nom. LNAMIX_CURRENT Recommended setting: MIX_CURRENT=0.
FRONTEND[2]	LNA2_CURRENT	0	-	Controls current in LNA 2 0: 0.80 mA LNA2 current with nom. LNAMIX_CURRENT 1: 1.18 mA LNA2 current with nom. LNAMIX_CURRENT Recommended settings: LNA2_CURRENT=0 at 402-470 MHz, LNA2_CURRENT=1 at 804-940 MHz.
FRONTEND[1]	SDC_CURRENT	0	-	Controls current in the single-to-diff. converter 0: 0.29 mA SDC current with nom. LNAMIX_CURRENT 1: 0.56 mA SDC current with nom. LNAMIX_CURRENT Recommended settings: SDC_CURRENT=0 at 402-470 MHz, SDC_CURRENT=1 at 804-940 MHz.
FRONTEND[0]	LNAMIX_BIAS	1	-	Controls how front-end bias currents are generated 0: Constant current biasing 1: Constant Gm-R biasing (reduces gain variation) Recommended setting: LNAMIX_BIAS=0.

ANALOG Register (17h)

REGISTER	NAME	Default value	Active	Description
ANALOG[7]	BANDSELECT	1	-	Frequency band selection 0: 402-470 MHz band 1: 804-940 MHz band
ANALOG[6]	LO_DC	1	-	Lower LO DC level to mixers 0: High LO DC level to mixers 1: Low LO DC level to mixers Recommended settings: LO_DC=1 for 402-470 MHz, LO_DC=0 for 804-940 MHz.
ANALOG[5]	VGA_BLANKING	1	H	Enable analogue blanking switches in VGA when changing VGA gain. 0: Blanking switches are disabled 1: Blanking switches are turned on for approx. 0.8µs when gain is changed (always on if AGC_DISABLE=1) Recommended setting: VGA_BLANKING=0.
ANALOG[4]	PD_LONG	0	H	Selects short or long reset delay in phase detector 0: Short reset delay 1: Long reset delay Recommended setting: PD_LONG=0.
ANALOG[3]	-	0	-	Reserved, write 0
ANALOG[2]	PA_BOOST	0	H	Boost PA bias current for higher output power Recommended setting: PA_BOOST=1.
ANALOG[1:0]	DIV_BUFF_CURRENT[1:0]	3	-	Overall bias current adjustment for VCO divider and buffers 0: 4/6 of nominal VCO divider and buffer current 1: 4/5 of nominal VCO divider and buffer current 2: Nominal VCO divider and buffer current 3: 4/3 of nominal VCO divider and buffer current Recommended settings: DIV_BUFF_CURRENT=3

BUFF_SWING Register (18h)

REGISTER	NAME	Default value	Active	Description
BUFF_SWING[7:6]	PRE_SWING[1:0]	3	-	Prescaler swing. Fractions for PRE_CURRENT=0: 0: 2/3 of nominal swing 1: 1/2 of nominal swing 2: 4/3 of nominal swing 3: Nominal swing Recommended setting: PRE_SWING=1.
BUFF_SWING[5:3]	RX_SWING[2:0]	4	-	LO buffer swing, in RX (to mixers) 0: Smallest load resistance (smallest swing) ... 7: Largest load resistance (largest swing) Recommended setting: RX_SWING=2.
BUFF_SWING[2:0]	TX_SWING[2:0]	1	-	LO buffer swing, in TX (to power amplifier driver) 0: Smallest load resistance (smallest swing) ... 7: Largest load resistance (largest swing) Recommended settings: TX_SWING=4 for 402-470 MHz, TX_SWING=0 for 804-940 MHz.

BUFF_CURRENT Register (19h)

REGISTER	NAME	Default value	Active	Description
BUFF_CURRENT[7:6]	PRE_CURRENT[1:0]	1	-	Prescaler current scaling 0: Nominal current 1: 2/3 of nominal current 2: 1/2 of nominal current 3: 2/5 of nominal current Recommended setting: PRE_CURRENT=0.
BUFF_CURRENT[5:3]	RX_CURRENT[2:0]	4	-	LO buffer current, in RX (to mixers) 0: Minimum buffer current ... 7: Maximum buffer current Recommended setting: RX_CURRENT=4.
BUFF_CURRENT[2:0]	TX_CURRENT[2:0]	5	-	LO buffer current, in TX (to PA driver) 0: Minimum buffer current ... 7: Maximum buffer current Recommended settings: TX_CURRENT=2 for 402-470 MHz, TX_CURRENT=5 for 804-940 MHz.

PLL_BW Register (1Ah)

REGISTER	NAME	Default value	Active	Description
PLL_BW[7:0]	PLL_BW[7:0]	134	-	Charge pump current scaling/rounding factor. Used to calibrate charge pump current for the desired PLL loop bandwidth. The value is given by: $PLL_BW = 174 + 16 \cdot \log_2(BW / R_2)$, where BW is the desired loop bandwidth (in Hz), and R_2 is the value (in Ω) of the resistor that gives a zero in the external loop filter.

CALIBRATE Register (1Bh)

REGISTER	NAME	Default value	Active	Description
CALIBRATE[7]	CAL_START	0	↑	↑ 1: Calibration started 0: Calibration inactive
CALIBRATE[6]	CAL_DUAL	0	H	Use calibration results for both frequency A and B 0: Store results in A or B defined by F_REG (MAIN[6]) 1: Store calibration results in both A and B
CALIBRATE[5:4]	CAL_WAIT[1:0]	0	-	Selects calibration wait time (affects accuracy) 0 (00): Calibration time is approx. 90000 F_REF periods 1 (01): Calibration time is approx. 110000 F_REF periods 2 (10): Calibration time is approx. 130000 F_REF periods 3 (11): Calibration time is approx. 200000 F_REF periods Recommended setting: CAL_WAIT=3 for best accuracy in calibrated PLL loop filter bandwidth.
CALIBRATE[3]	-	0	-	Reserved, write 0
CALIBRATE[2:0]	CAL_ITERATE[2:0]	5	-	Iteration start value for calibration DAC 0 (000): DAC start value 1, VC<0.49 V after calibration 1 (001): DAC start value 2, VC<0.66 V after calibration 2 (010): DAC start value 3, VC<0.82 V after calibration 3 (011): DAC start value 4, VC<0.99 V after calibration 4 (100): DAC start value 5, VC<1.15 V after calibration 5 (101): DAC start value 6, VC<1.32 V after calibration 6 (110): DAC start value 7, VC<1.48 V after calibration 7 (111): DAC start value 8, VC<1.65 V after calibration Recommended setting: CAL_ITERATE=5.

PA_POWER Register (1Ch)

REGISTER	NAME	Default value	Active	Description
PA_POWER[7:4]	PA_HIGH [3:0]	0	-	Controls output power in high-power array 0: High-power array is off 1: Minimum high-power array output power ... 15: Maximum high-power array output power
PA_POWER[3:0]	PA_LOW[3:0]	15	-	Controls output power in low-power array 0: Low-power array is off 1: Minimum low-power array output power ... 15: Maximum low-power array output power It is more efficient in terms of current consumption to use either the lower or upper 4-bits in the PA_POWER register to control the power.

MATCH Register (1Dh)

REGISTER	NAME	Default value	Active	Description
MATCH[7:4]	RX_MATCH[3:0]	0	-	Selects matching capacitor array value for RX. Each step is approximately 0.4 pF.
MATCH[3:0]	TX_MATCH[3:0]	0	-	Selects matching capacitor array value for TX. Each step is approximately 0.4 pF.

PHASE_COMP Register (1Eh)

REGISTER	NAME	Default value	Active	Description
PHASE_COMP[7:0]	PHASE_COMP[7:0]	0	-	Signed compensation value for LO I/Q phase error. Used for image rejection calibration. -128: approx. -6.2° adjustment between I and Q phase -1: approx. -0.02° adjustment between I and Q phase 0: approx. +0.02° adjustment between I and Q phase 127: approx. +6.2° adjustment between I and Q phase

GAIN_COMP Register (1Fh)

REGISTER	NAME	Default value	Active	Description
GAIN_COMP[7:0]	GAIN_COMP[7:0]	0	-	Signed compensation value for mixer I/Q gain error. Used for image rejection calibration. -128: approx. -1.16 dB adjustment between I and Q gain -1: approx. -0.004 dB adjustment between I and Q gain 0: approx. +0.004 dB adjustment between I and Q gain 127: approx. +1.16 dB adjustment between I and Q gain

POWERDOWN Register (20h)

REGISTER	NAME	Default value	Active	Description
POWERDOWN[7]	PA_PD	0	H	Sets PA in power-down when PD_MODE[1:0]=2
POWERDOWN[6]	VCO_PD	0	H	Sets VCO in power-down when PD_MODE[1:0]=2
POWERDOWN[5]	BUFF_PD	0	H	Sets VCO divider, LO buffers and prescaler in power-down when PD_MODE[1:0]=2
POWERDOWN[4]	CHP_PD	0	H	Sets charge pump in power-down when PD_MODE[1:0]=2
POWERDOWN[3]	LNAMIX_PD	0	H	Sets LNA/mixer in power-down when PD_MODE[1:0]=2
POWERDOWN[2]	VGA_PD	0	H	Sets VGA in power-down when PD_MODE[1:0]=2
POWERDOWN[1]	FILTER_PD	0	H	Sets image filter in power-down when PD_MODE[1:0]=2
POWERDOWN[0]	ADC_PD	0	H	Sets ADC in power-down when PD_MODE[1:0]=2

TEST1 Register (21h, for test only)

REGISTER	NAME	Default value	Active	Description
TEST1[7:4]	CAL_DAC_OPEN[3:0]	4	-	Calibration DAC override value, active when BREAK_LOOP=1
TEST1[3:0]	CHP_CO[3:0]	13	-	Charge pump current override value

TEST2 Register (22h, for test only)

REGISTER	NAME	Default value	Active	Description
TEST2[7]	BREAK_LOOP	0	H	0: PLL loop closed 1: PLL loop open
TEST2[6]	CHP_OVERRIDE	0	H	0: use calibrated value 1: use CHP_CO[3:0] value
TEST2[5]	VCO_OVERRIDE	0	H	0: use calibrated value 1: use VCO_AO[4:0] value
TEST2[4:0]	VCO_AO[4:0]	16	-	VCO_ARRAY override value

TEST3 Register (23h, for test only)

REGISTER	NAME	Default value	Active	Description
TEST3[7]	VCO_CAL_MANUAL	0	H	Enables "manual" VCO calibration (test only)
TEST3[6]	VCO_CAL_OVERRIDE	0	H	Override VCO current calibration 0: Use calibrated value 1: Use VCO_CO[5:0] value VCO_CAL_OVERRIDE controls VCO_CAL_CLK if VCO_CAL_MANUAL=1. Negative transitions are then used to sample VCO_CAL_COMP.
TEST3[5:0]	VCO_CO[5:0]	6	-	VCO_CAL_CURRENT override value

TEST4 Register (24h, for test only)

REGISTER	NAME	Default value	Active	Description
TEST4[7]	CHP_DISABLE	0	H	Disable normal charge pump operation
TEST4[6]	CHP_TEST_UP	0	H	Force charge pump to output "up" current
TEST4[5]	CHP_TEST_DN	0	H	Force charge pump to output "down" current
TEST4[4:3]	TM_IQ[1:0]	0	-	Value of differential I and Q outputs from mixer when TM_ENABLE=1 0: I output negative, Q output negative 1: I output negative, Q output positive 2: I output positive, Q output negative 3: I output positive, Q output positive
TEST4[2]	TM_ENABLE	0	H	Enable DC control of mixer output (for testing)
TEST4[1]	TF_ENABLE	0	H	Connect analogue test module to filter inputs
TEST4[0]	TA_ENABLE	0	H	Connect analogue test module to ADC inputs

If TF_ENABLE=1 or TA_ENABLE=1 in TEST4 register, then INTERFACE[3:0] controls analogue test module: INTERFACE[3] = TEST_PD, INTERFACE[2:0] = TEST_MODE[2:0]. Otherwise, TEST_PD=1 and TEST_MODE[2]=1.

TEST5 Register (25h, for test only)

REGISTER	NAME	Default value	Active	Description
TEST5[7]	F_COMP_ENABLE	0	H	Enable frequency comparator output F_COMP from phase detector
TEST5[6]	SET_DITHER_CLOCK	1	H	Enable dithering of delta-sigma clock
TEST5[5]	ADC_TEST_OUT	0	H	Outputs ADC samples on LOCK and DIO, while ADC_CLK is output on DCLK
TEST5[4]	CHOP_DISABLE	0	H	Disable chopping in ADC integrators
TEST5[3]	SHAPING_DISABLE	0	H	Disable ADC feedback mismatch shaping
TEST5[2]	VCM_ROT_DISABLE	0	H	Disable rotation for VCM mismatch shaping
TEST5[1:0]	ADC_ROTATE[1:0]	0	-	Control ADC input rotation 0: Rotate in 00 01 10 11 sequence 1: Rotate in 00 10 11 01 sequence 2: Always use 00 position 3: Rotate in 00 10 00 10 sequence

TEST6 Register (26h, for test only)

REGISTER	NAME	Default value	Active	Description
TEST6[7:4]	-	0	-	Reserved, write 0
TEST6[3]	VGA_OVERRIDE	0	-	Override VGA settings
TEST6[2]	AC1O	0	-	Override value to first AC coupler in VGA 0: Approx. 0 dB gain 1: Approx. -12 dB gain
TEST6[1:0]	AC2O[1:0]	0	-	Override value to second AC coupler in VGA 0: Approx. 0 dB gain 1: Approx. -3 dB gain 2: Approx. -12 dB gain 3: Approx. -15 dB gain

TEST7 Register (27h, for test only)

REGISTER	NAME	Default value	Active	Description
TEST7[7:6]	-	0	-	Reserved, write 0
TEST7[5:4]	VGA1O[1:0]	0	-	Override value to VGA stage 1
TEST7[3:2]	VGA2O[1:0]	0	-	Override value to VGA stage 2
TEST7[1:0]	VGA3O[1:0]	0	-	Override value to VGA stage 3

STATUS Register (40h, read only)

REGISTER	NAME	Default value	Active	Description
STATUS[7]	CAL_COMPLETE	-	H	Set to 0 when PLL calibration starts, and set to 1 when calibration has finished
STATUS[6]	SEQ_ERROR	-	H	Set to 1 when PLL failed to lock during automatic power-up sequencing
STATUS[5]	LOCK_INSTANT	-	H	Instantaneous PLL lock indicator
STATUS[4]	LOCK_CONTINUOUS	-	H	PLL lock indicator, as defined by LOCK_ACCURACY. Set to 1 when PLL is in lock
STATUS[3]	CARRIER_SENSE	-	H	Carrier sense when RSSI is above CS_LEVEL
STATUS[2]	LOCK	-	H	Logical level on LOCK pin
STATUS[1]	DCLK	-	H	Logical level on DCLK pin
STATUS[0]	DIO	-	H	Logical level on DIO pin

RESET_DONE Register (41h, read only)

REGISTER	NAME	Default value	Active	Description
RESET_DONE[7]	ADC_RESET_DONE	-	H	Reset of ADC control logic done
RESET_DONE[6]	AGC_RESET_DONE	-	H	Reset of AGC (VGA control) logic done
RESET_DONE[5]	GAUSS_RESET_DONE	-	H	Reset of Gaussian data filter done
RESET_DONE[4]	AFC_RESET_DONE	-	H	Reset of AFC / FSK decision level logic done
RESET_DONE[3]	BITSYNC_RESET_DONE	-	H	Reset of modulator, bit synchronization logic and PN9 PRBS generator done
RESET_DONE[2]	SYNTH_RESET_DONE	-	H	Reset digital part of frequency synthesizer done
RESET_DONE[1]	SEQ_RESET_DONE	-	H	Reset of power-up sequencing logic done
RESET_DONE[0]	CAL_LOCK_RESET_DONE	-	H	Reset of calibration logic and lock detector done

RSSI Register (42h, read only)

REGISTER	NAME	Default value	Active	Description
RSSI[7]	-	-	-	Not in use, will read 0
RSSI[6:0]	RSSI[6:0]	-	-	Received signal strength indicator. The relative power is given by $RSSI \times 1.5$ dB in a logarithmic scale. The VGA gain set by <i>VGA_SETTING</i> must be taken into account. See page 32 for more details.

AFC Register (43h, read only)

REGISTER	NAME	Default value	Active	Description
AFC[7:0]	AFC[7:0]	-	-	Average received frequency deviation from IF. This 8-bit 2-complement signed value equals the demodulator decision level and can be used for AFC. The average frequency offset from the IF frequency is $\Delta F = \text{Baud rate} \cdot \text{AFC} / 16$

GAUSS_FILTER Register (44h)

REGISTER	NAME	Default value	Active	Description
GAUSS_FILTER[7:0]	GAUSS_FILTER[7:0]	-	-	Readout of instantaneous IF frequency offset from nominal IF. Signed 8-bit value. $\Delta F = \text{Baud rate} \times \text{GAUSS_FILTER} / 8$

STATUS1 Register (45h, for test only)

REGISTER	NAME	Default value	Active	Description
STATUS1[7:4]	CAL_DAC[3:0]	-	-	Status vector defining applied Calibration DAC value
STATUS1[3:0]	CHP_CURRENT[3:0]	-	-	Status vector defining applied CHP_CURRENT value

STATUS2 Register (46h, for test only)

REGISTER	NAME	Default value	Active	Description
STATUS2[7:5]	CC1020_VERSION[2:0]	-	-	CC1020 version code: 0: Pre-production version 1: First productions version 2-7: Reserved for future use
STATUS2[4:0]	VCO_ARRAY[4:0]	-	-	Status vector defining applied VCO_ARRAY value

STATUS3 Register (47h, for test only)

REGISTER	NAME	Default value	Active	Description
STATUS3[7]	F_COMP	-	-	Frequency comparator output from phase detector
STATUS3[6]	VCO_CAL_COMP	-	-	Readout of VCO current calibration comparator. Equals 1 if current defined by VCO_CURRENT_A/B is larger than the VCO core current
STATUS3[5:0]	VCO_CAL_CURRENT[5:0]	-	-	Status vector defining applied VCO_CAL_CURRENT value

STATUS4 Register (48h, for test only)

REGISTER	NAME	Default value	Active	Description
STATUS4[7:6]	ADC_MIX[1:0]	-	-	Readout of mixer input to ADC
STATUS4[5:3]	ADC_I[2:0]	-	-	Readout of ADC "I" output
STATUS4[2:0]	ADC_Q[2:0]	-	-	Readout of ADC "Q" output

STATUS5 Register (49h, for test only)

REGISTER	NAME	Default value	Active	Description
STATUS5[7:0]	FILTER_I[7:0]	-	-	Upper bits of "I" output from channel filter

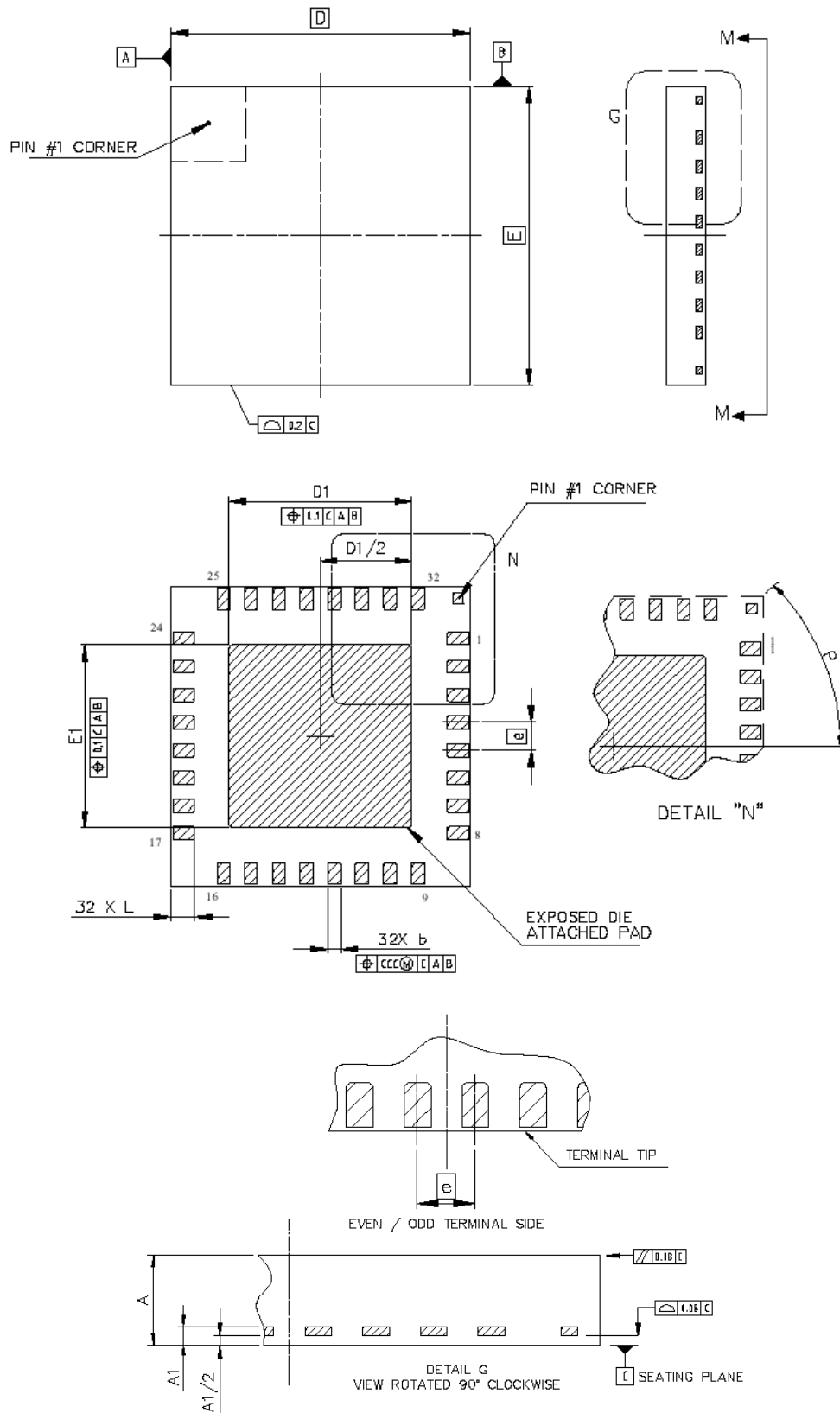
STATUS6 Register (4Ah, for test only)

REGISTER	NAME	Default value	Active	Description
STATUS6[7:0]	FILTER_Q[7:0]	-	-	Upper bits of "Q" output from channel filter

STATUS7 Register (4Bh, for test only)

REGISTER	NAME	Default value	Active	Description
STATUS7[7:5]	-	-	-	Not in use, will read 0
STATUS7[4:0]	VGA_GAIN_OFFSET[4:0]	-	-	Readout of offset between VGA_SETTING and actual VGA gain set by AGC

Package Description (QFN 32)



Quad Flat Pack - No Lead Package (QFN)											
		D	E	A	A1	e	b	L	D1	E1	P
QFN 32	Min			0.8			0.25	0.45	4.18	4.18	
		7.0	7.0	0.9	0.203	0.65	0.30	0.55	4.28	4.28	
	Max			1.0			0.35	0.65	4.38	4.38	45°
All dimensions in mm. Angles are in degrees.											

Package is compliant to JEDEC: MO-220.

Package Thermal Properties

Thermal resistance			
Air velocity [m/s]	0	1	2
Rth,j-a [K/W]	21.4	18.9	17.0

Soldering Information

Recommended soldering profile is according to IPC/JEDEC J-STD-020B, July 2002.

Plastic Tube Specification

QFN 7x7 mm antistatic tube.

Tube Specification				
Package	Tube Width	Tube Height	Tube Length	Units per Tube
QFN 32	8.5 ± 0.2 mm	2.2 +0.2/-0.1 mm	315 ± 1.25 mm	43

Carrier Tape and Reel Specification

Carrier tape and reel is in accordance with EIA Specification 481.

Tape and Reel Specification					
Package	Tape Width	Component Pitch	Hole Pitch	Reel Diameter	Units per Reel
QFN 32	16 mm	12 mm	4 mm	13"	4000

Ordering Information

Ordering part number	Description	MOQ
CC1020	Single Chip RF Transceiver	43 (tube)
CC1020/T&R	Single Chip RF Transceiver	4000 (tape and reel)
CC1020/1070DK-433	CC1020/1070 Development Kit, 433 MHz	1
CC1020/1070DK-868/915	CC1020/1070 Development Kit, 868/915 MHz	1
CC1020SK	CC1020 Sample Kit (5 pcs)	1

MOQ = Minimum Order Quantity

General Information

Document Revision History

Revision	Date	Description/Changes
1.4	November 2003	New improved image calibration routine. Changes to preamble length and synchronization word for improved packet error rate. Included plot of blocking/selectivity. Included data on PA_EN and LNA_EN pin drive. Changes to Digital FM. Changes to some of the electrical specification parameters.

Product Status Definitions

Data Sheet Identification	Product Status	Definition
Advance Information	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. Chipcon reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains the final specifications. Chipcon reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by Chipcon. The data sheet is printed for reference information only.

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