

# Chrontel CH7304 Single LVDS Transmitter

## Features

- Single LVDS transmitter
- Supports pixel rate up to 100M pixels/sec
- Supports up to SXGA resolution (1280 x 1024)
- LVDS low jitter PLL
- LVDS 24-bit or 18-bit output
- 2D dither engine for 18-bit output
- Panel protection and power down sequencing
- Programmable power management
- Fully programmable through serial port
- Complete Windows and DOS driver support
- Variable voltage interface to graphics device
- Offered in a 64-pin LQFP package

## 1.0 General Description

The CH7304 is a Display Controller device, which accepts a graphics data stream over one 12-bit wide variable voltage (1.1V to 3.3V) port. The data stream outputs through an LVDS transmitter to an LCD panel. A maximum of 100M pixels per second can be output through a single LVDS link.

The LVDS transmitter supports 24-bit panels; it also includes a programmable dither function for support of 18-bit panels. Data is encoded into commonly used formats, including those detailed in the OpenLDI and the SPWG specification. Serialized data output on four differential channels.

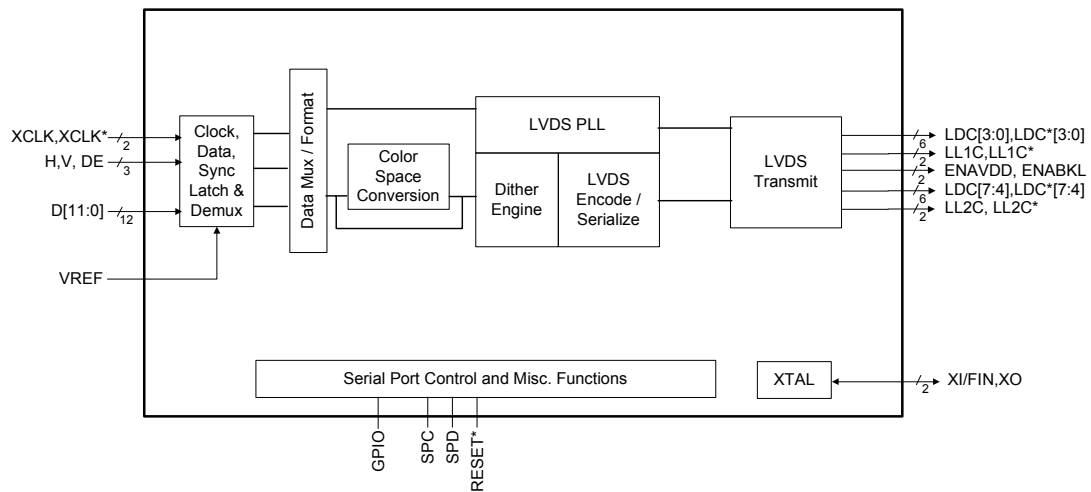


Figure 1: Functional Block Diagram

## 2.0 Pin Assignment

### 2.1 Package Diagram

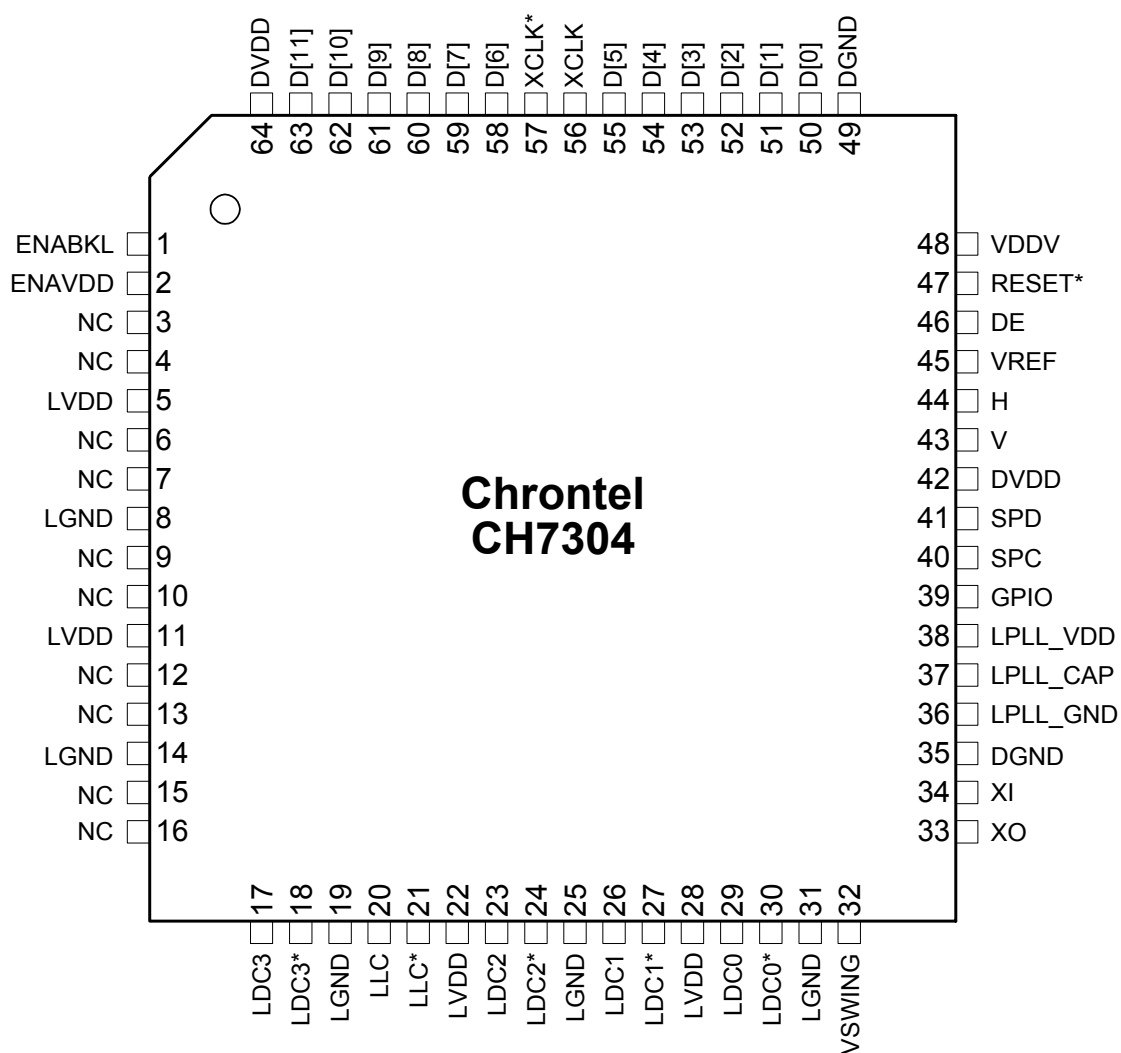


Figure 2: 64 Pin LQFP Package (Top View)

## 2.2 Pin Description

Table 1: Pin Description

| Pin #                        | # of Pins | Type   | Symbol    | Description   |
|------------------------------|-----------|--------|-----------|---|
| 1                            | 1         | Out    | ENABLK    | <b>Back Light Enable</b><br>Enable Back-Light of LCD Panel. Output is driven from 0 to DVDD.  |
| 2                            | 1         | Out    | ENAVDD    | <b>Panel Power Enable</b><br>Enable panel VDD. Output is driven from 0 to DVDD.   |
| 3,4,6,7,9,10,<br>12,13,15,16 | 10        | -      | NC        | <b>No Connect</b>   |
| 20, 21                       | 2         | Out    | LLC, LLC* | <b>LVDS Differential Clock</b>  |
| 17,23,26,29                  | 4         | Out    | LDC[3:0]  | <b>Positive LVDS differential data[3:0]</b>   |
| 18,24,27,30                  | 4         | Out    | LDC[3:0]* | <b>Negative LVDS differential data [3:0]</b>  |
| 32                           | 1         | In     | VSWING    | <b>LVDS Voltage Swing Control</b><br>This pin sets the swing level of the LVDS outputs. A 2.4K Ohm resistor should be connected between this pin and LGND (pin 31) using short and wide traces.   |
| 33                           | 1         | Out    | XO        | <b>Crystal Output</b><br>A parallel resonance 14.31818MHz crystal ( $\pm 20$ ppm) should be attached between this pin and XI. However, if an external CMOS clock is attached to XI, XO should be left open.   |
| 34                           | 1         | In     | XI        | <b>Crystal Input / External Reference Input</b><br>A parallel resonance 14.31818MHz crystal ( $\pm 20$ ppm) should be attached between this pin and XO. However, an external CMOS compatible clock can drive the XI input.  |
| 37                           | 1         | Analog | LPLL_CAP  | <b>LVDS PLL Capacitor</b><br>This pin allows coupling of any signal to the on-chip loop filter capacitor.   |
| 39                           | 1         | In/Out | GPIO      | <b>General Purpose Input / Output</b><br>This pin provides general purpose I/O and is controlled via the serial port. The voltage level on input and output is DVDD. See description of GPIO Controls for I/O configuration.  |
| 40                           | 1         | In     | SPC       | <b>Serial Port Clock Input</b><br>This pin functions as the clock input of the serial port and can operate with inputs from 1.1V ~ 3.3V. The serial port address of the CH7304 is 75h. For more details on CH7304 serial port read/write operations, please refer to AN61.  |
| 41                           | 1         | In/Out | SPD       | <b>Serial Port Data Input / Output</b><br>This pin functions as the bi-directional data pin of the serial port and can operate with inputs from 1.1V ~ 3.3V. Outputs are driven from 0 to VDDV. The serial port address of the CH7304 is 75h. For more details on CH7304 serial port read/write operations, please refer to AN61. |
| 43                           | 1         | In     | V         | <b>Vertical Sync Input</b><br>This pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDV. VREF signal is the threshold level.  |
| 44                           | 1         | In     | H         | <b>Horizontal Sync Input</b><br>This pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDV. VREF is the threshold level for this input.  |
| 45                           | 1         | In     | VREF      | <b>Reference Voltage Input</b><br>The VREF pin inputs a reference voltage of $VDDV / 2$ . The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync and clock inputs.  |
| 46                           | 1         | In     | DE        | <b>Data Enable</b><br>This pin accepts a data enable signal which is high when active video data is input to the device, and remains low during all other times. The levels are 0 to VDDV. VREF is the threshold level.   |

Table 1: Pin Description (continued)

| Pin #         | # of Pins | Type  | Symbol         | Description   |
|---------------|-----------|-------|----------------|---|
| 47            | 1         | In    | RESET*         | <b>Reset * Input</b> (Internal Pull-up)<br>When this pin is low, the device is held in the power on reset condition.<br>When this pin is high, reset is controlled through the serial port.   |
| 50-55, 58-63  | 12        | In    | D[11:0]        | <b>Data[11] through Data[0] Inputs</b><br>These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV. VREF is the threshold level.   |
| 56, 57        | 2         | In    | XCLK,<br>XCLK* | <b>External Clock Inputs</b><br>These inputs form a differential clock signal input to the device for use with the H, V and D[11:0] data. If differential clocks are not available, the XCLK* input should be connected to VREF. The clock polarity can be selected by the MCP control bit ( <b>Register 1Ch</b> ). |
| 42, 64        | 2         | Power | DVDD           | <b>Digital Supply Voltage</b> (3.3V)  |
| 35, 49        | 2         | Power | DGND           | <b>Digital Ground</b>   |
| 48            | 1         | Power | VDDV           | <b>I/O Supply Voltage</b> (1.1V to 3.3V)  |
| 5,11,22,28    | 4         | Power | LVDD           | <b>LVDS Supply Voltage</b> (3.3V)   |
| 8,14,19,25,31 | 5         | Power | LGND           | <b>LVDS Ground</b>  |
| 38            | 1         | Power | LPLL_VDD       | <b>LVDS PLL Supply Voltage</b> (3.3V)   |
| 36            | 1         | Power | LPLL_GND       | <b>LVDS PLL Ground</b>  |

### 3.0 Package Dimensions

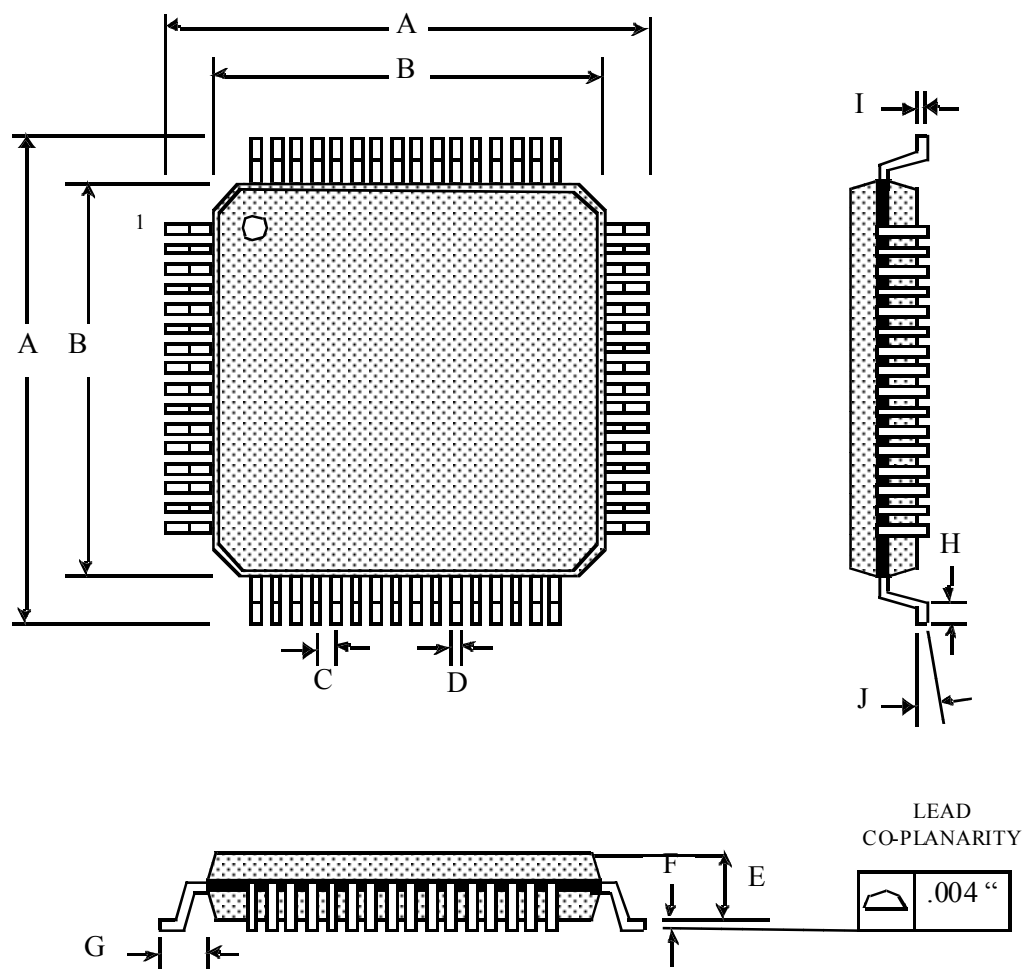


Table of Dimensions

| No. of Leads     |     | SYMBOL |    |      |      |      |      |      |      |      |    |
|------------------|-----|--------|----|------|------|------|------|------|------|------|----|
| 64 (10 X 10 mm)  |     | A      | B  | C    | D    | E    | F    | G    | H    | I    | J  |
| Milli-<br>meters | MIN | 12     | 10 | 0.50 | 0.17 | 1.35 | 0.05 | 1.00 | 0.45 | 0.09 | 0° |
|                  | MAX |        |    |      | 0.27 | 1.45 | 0.15 |      | 0.75 | 0.20 | 7° |

Figure 3: 64 Pin LQFP Package

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