

# CS3310

## Programmable Convolution Encoder



The CS3310 Programmable Convolutional Encoder is a high performance implementation suitable for a range of Forward Error Correction applications. This highly integrated Application Specific Virtual Components (ASVC) can be used in conjunction with other FEC related cores available from Amphion to rapidly construct complete FEC solutions. The CS3310 programmable convolutional encoder operates in Viterbi or Trellis modes and provides a wide range of coding rates. The CS3310 is available in both ASIC and programmable logic versions that have been handcrafted by Amphion to deliver high performance while minimizing power consumption and silicon area.

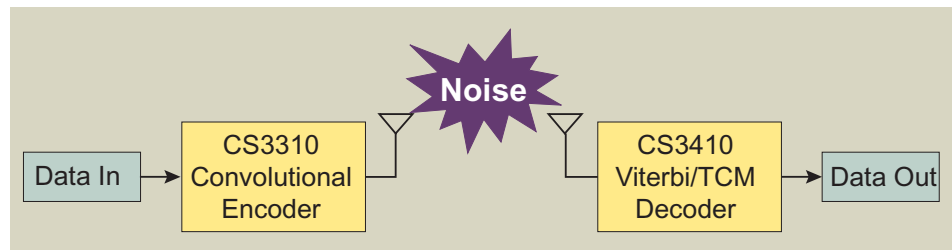


Figure 1: Typical Transmission System Model

### ENCODER FEATURES

- ◆ **Programmable convolutional encoder (k=7)**
- ◆ **Supports block and continuous mode operations**
- ◆ **Generator polynomials**
  - G0 = 171 (octal)
  - G1 = 133 (octal)
  - G2 = 165 (octal) Viterbi  $\frac{1}{3}$  mode
- ◆ **Viterbi mode**
  - Fully compliant with:
    - INTELSAT IESS-308/ 309
    - DVB ETS 300-421
    - DVB-T ETSI 300-744
  - Coding rates: 1/2, 1/3, 2/3, 3/4, 5/6, 7/8
- ◆ **Trellis mode:**
  - Coding rates: 2/3 (8-PSK encoding), 3/4 (16-PSK encoding)
- ◆ **Byte-wide microprocessor interface**
- ◆ **Simple core interface for easy integration into other systems**

### KEY METRICS

- ◆ **Size:** 956 Gates (STD Cells)
- ◆ **Input clock:** 100 MHz

### APPLICATIONS

- ◆ **Wireless LANs**
- ◆ **Digital cellular phones**
- ◆ **Satellite communications**



# CS3310 Programmable Convolution Encoder

## PIN / PORT DESCRIPTION

Table 1 and Table 2 represent the descriptions of the input and output ports of the CS3310 in Viterbi and Trellis mode

respectively. Unless otherwise stated, all signals are active high and bit (0) is the least significant bit.

**Table 1: CS3310 - Viterbi Mode Interface Signal Definitions**

Section	Name	Type	Function
Encoder I/O Pins	DIN0	I	Data Input
	DIN1	I	N/C
	DIN2	I	N/C
	CLK	I	Clock
	RST	I	Asynchronous Reset (Active High)
	DVALI	I	Data Valid In
	BLKSTARTI	I	Block Start (Block Mode Only)
	BLKENDI	I	Block End (Block Mode Only)
	PSK0	O	N/C
Encoder I/O Pins	PSK1	O	N/C
	DOUT0	O	Data Output Bit 0
	DOUT1	O	Data Output Bit 1
	DOUT2	O	Data Output Bit 2
	DVOUT0	O	Punctured Data Valid Output Bit 0
	DVOUT1	O	Punctured Data Valid Output Bit 1
	DVOUT2	O	Punctured Data Valid Output Bit 2
	DVALO	O	Data Valid Out
Processor Bus Interface Pins	UP_DIN[7:0]	I	Processor Interface Input Data Bus
	UP_DOUT[7:0]	O	Processor Interface Output Data Bus
	WR	I	Processor Interface Write Strobe (Active High)
	RD	I	Processor Interface Read Strobe (Active High)
	ADD	I	Processor Interface Address Bus Bit

**Table 2: CS3310 - Trellis Mode Interface Signal Definitions**

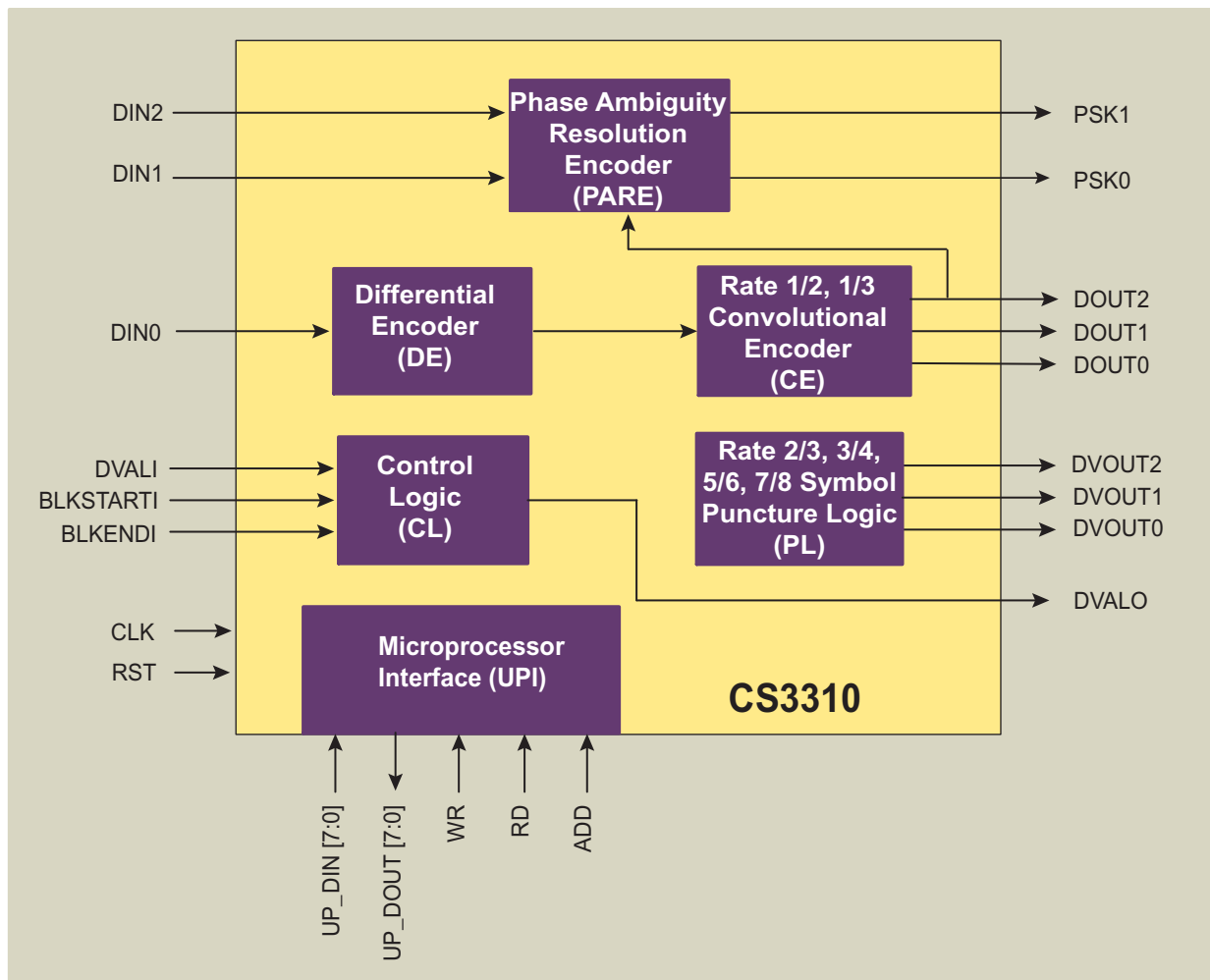
Section	Name	Type	Function
Encoder I/O Pins	DIN0	I	Data Input Bit 0
	DIN1	I	Data Input Bit 1
	DIN2	I	Data Input Bit 2
	CLK	I	Clock
	RST	I	Asynchronous Reset (Active High)
	DVALI	I	Data Valid In
	BLKSTARTI	I	Block Start (Block Mode Only)
	BLKENDI	I	Block End (Block Mode Only)
	PSK0	O	PSK Output Bit 0
	PSK1	O	PSK Output Bit 1
	DOUT0	O	Data Output Bit 0
	DOUT1	O	Data Output Bit 1
	DOUT2	O	N/C
	DVOUT0	O	N/C
	DVOUT1	O	N/C
	DVOUT2	O	N/C
	DVALO	O	Data Valid Out
Processor Bus Interface Pins	UP_DIN[7:0]	I	Processor Interface Input Data Bus
	UP_DOUT[7:0]	O	Processor Interface Output Data Bus
	WR	I	Processor Interface Write Strobe (Active High)
	RD	I	Processor Interface Read Strobe (Active High)
	ADD	I	Processor Interface Address Bus Bit

## CS3310 FUNCTIONAL DESCRIPTION

The CS3310 ASVC is a highly integrated Programmable Convolutional Encoder suitable for a wide range of reliable communication applications. The CS3310 Encoder operates in both Viterbi and Trellis mode. The Viterbi mode can be used in power limited systems and the Trellis mode can be used in power and bandwidth limited systems. The block diagram in Figure 2 shows the main functional blocks and interfaces that have been identified for the Programmable Convolutional Encoder. Internally the encoder is comprised of individual blocks: the Differential Encoder (DE), Convolutional Encoder (CE), Phase Ambiguity Resolution Encoder (PARE), Symbol Puncture Logic (PL) and the Data Valid controller (DV). A Microprocessor Interface (UPI) is also included.

## CONVOLUTIONAL CODES FOR ERROR CORRECTION

Convolutional error-correction capabilities result from outputs that depend on past data values. Each coded bit is generated by convolving the input bit with the previous uncoded bits. Convolving a signal with itself adds a level of dependence on the past values. This mechanism provides the ability to correct (to a certain level) a signal that has been corrupted with noise such as Additive White Gaussian Noise (AWGN). Data that is convolutionally encoded can be decoded through knowledge of the possible state transitions, created from the dependence of the current symbol on past data



**Figure 2: CS3310 Overview Diagram**

## DE: DIFFERENTIAL ENCODER BLOCK

This block will toggle an output signal when the input signal changes. The differential encoder block may be bypassed if desired.

## CE: CONVOLUTIONAL ENCODER BLOCK

Figure 3 shows a block diagram of an industry standard  $k = 7$  convolutional encoder.

- Rate 1/2: Generator polynomials  $G(0) = 171$  (octal),  $G(1) = 133$  (Octal)
- Rate 1/3: Generator polynomials  $G(0) = 171$  (octal),  $G(1) = 133$  (Octal),  $G(2) = 165$  (Octal)

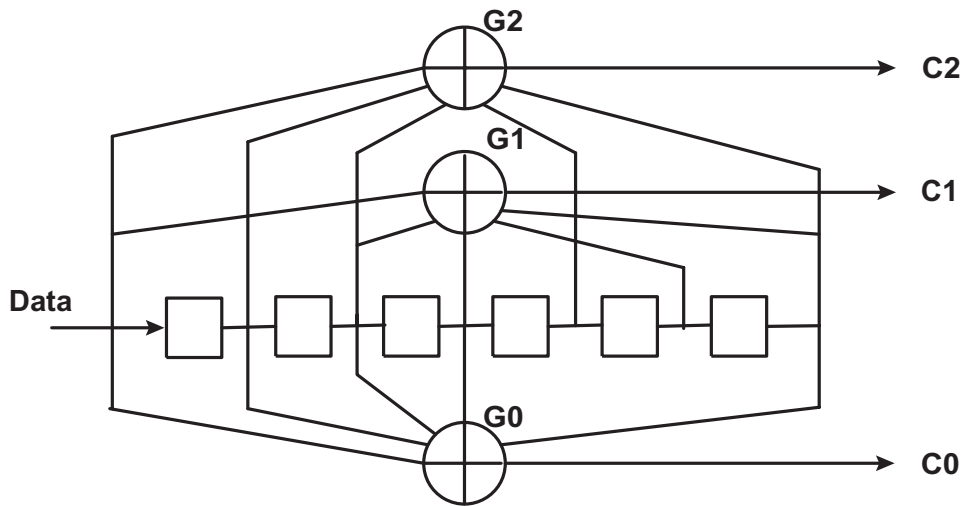
## PH: PHASE AMBIGUITY RESOLUTION ENCODER BLOCK

This block contains two 4-phase differential encoders whose output is multiplexed by the DOUT1 signal of the convolutional encoder. Rate 2/3 (8-PSK) outputs and rate 3/4 (16-PSK) outputs are both obtained from this block.

## PL: SYMBOL PUNCTURE LOGIC BLOCK

Table 3 illustrates the puncture patterns describing the DVOUT0, DVOUT1 and DVOUT2 signals generated by this block for rates: 1/2, 1/3, 2/3, 3/4, 5/6 and 7/8:

(1 = bit marked as valid, 0 = bit marked as invalid)



**Figure 3: Block Diagram of Implementation of Convolutional Encoder**

**Table 3: Coding Rates and Corresponding Puncture Patterns**

Coding Rate	DVOUT2	DVOUT1	DVOUT0
1/2	0	1	1
1/3	1	1	1
2/3	0 0	1 1	1 0
3/4	0 0 0	1 1 0	1 0 1
5/6	0 0 0 0 0	1 1 0 1 0	1 0 1 0 1
7/8	0 0 0 0 0 0 0	1 1 1 1 0 1 0	1 0 0 0 1 0 1

## CL: CONTROL LOGIC BLOCK

This block controls the operation of the core depending on whether it is configured in Continuous Mode or Block Mode and on the value of DVALI, BSTARTI and BLKENDI. It also sets DVALO accordingly.

### Continuous Mode

In Continuous Mode the DVALI input is used to enable / disable the core in addition to setting the value of the DVALO. When a high DVALI signal is clocked into the core then the core will be enabled. One clock cycle later DVALO will be set high and the output data (PSKx, DVOUTx and DOUTx) will be valid. When a low DVALI is clocked into the core the core will be disabled and one clock cycle later DVALO together with PSKx, DOUTx and DVOUTx will go low to indicate that the output data is now invalid. The core is enabled once DVALI goes high again.

### Block Mode

In Block Mode the BLKSTARTI, BLKENDI and DVALI inputs are used to enable / disable the core in addition to setting the value of DVALO. BLKSTARTI and BLKENDI signals are only recognised if they are accompanied by a high signal value on the DVALI input. A further condition on the BLKENDI signal is that it can only be associated with a valid BLKSTARTI signal i.e. BLKENDI will only take effect if a valid BLKSTARTI signal has previously been clocked into the core. When BLKSTARTI is asserted high and clocked into the core, accompanied by a high signal on DVALI, then this is interpreted by the core as the beginning of a new block. The core will be enabled and prepared for fresh input data. One clock cycle later DVALO will be set high. When a valid BLKENDI signal is subsequently clocked into the core this is interpreted by the core as the end of a block. Six zeros are placed on the internal data lines to flush the CE block such that it is forced into the all-zero state. This “force-to-zero” mechanism is utilised by the decoder. Nine clock cycles after the BLENDI signal DVALO is cleared. PSKx, DOUTx and



# CS3310 Programmable Convolution Encoder

DVOUTx will be low when DVALO goes low. If DVALI input goes low while the core is being flushed the core will remain enabled until the CE block is completely flushed. A valid BLKSTARTI signal will at any time clear the core. If DVALI goes low during a block (apart from the case where the core is being flushed) then the core will be disabled and DVALO, PSKx, DOUTx and DVOUTx will go low one clock cycle later. The core will be enabled once DVALI goes high again.

## UPI: Microprocessor Interface

This byte-wide interface allows the configuration of the core to be set by a microprocessor. Two 8-bit Control Registers are available although configuration of the core only requires control bits to be loaded into one register. A default core configuration is loaded on reset. To write to the Control Registers the WR signal must be set to high with the associated address value on the ADD line to indicate which set of Control Registers are being written to. On the next positive clock edge after WR has been asserted high the core is configured. The Control Registers may be read by asserting the RD line high with the address line ADD being set to the address of the Control Register to be read.

## CORE OPERATION

The CS3310 operates in Viterbi or Trellis Mode. Each of these modes can support data being transmitted in Block Mode or Continuous Mode. All registers are updated on a positive clock edge and the reset is active high.

## VITERBI MODE

In Viterbi Mode the DIN0 signal is the only data input required. Rate 1/2 and rate 1/3 are obtained directly from the CE block and these outputs are available on the DOUTx lines. Rate 2/3, rate 3/4, rate 5/6 and rate 7/8 may be obtained by puncturing the DOUTx lines. The PL block generates two output signals that toggle to mark valid and invalid bits on the DVOUTx lines. The DVOUT0 signal describes the validity of data on the DOUT0 line and correspondingly DVOUT1 describes the DOUT1 line. The DE block may be bypassed in Viterbi Mode.

## TRELLIS MODE

Trellis Mode supports rate 2/3 (8-PSK) and rate 3/4 (16-PSK). When rate 2/3 is selected DIN0 and DIN1 are the input signals and DOUT0, DOUT1 and PSK0 are the corresponding output signals. In rate 3/4 operation DIN0, DIN1 and DIN2 are the input signals with DOUT0, DOUT1, PSK0 and PSK1 being output signals. All differential encoding in the DE block and the PARE block may be bypassed in Trellis Mode.

## CONTINUOUS AND BLOCK MODE

Continuous or Block Mode operation may be applied when the core is configured in Viterbi or Trellis Mode. In Continuous Mode a high value on DVALI indicates valid input data. DVALO will go high one clock cycle after DVALI has been clocked into the core. If DVALI goes low the core is disabled until DVALI goes high again. DVALO will indicate when data at the output is valid. In Block Mode a high value on BLKSTARTI indicates the beginning of a block of data. This will clear the core and cause it to operate as in Continuous Mode until BLKENDI goes high to indicate the end of a block. When an end of block is detected zeros are sequentially inserted into the CE block to flush it. DVALO goes low once the CE block is clear.

## CORE CONFIGURATION

Two 8-bit Control Registers, CONT\_REG0 and CONT\_REG1 are situated in the microprocessor interface. Table 4 shows the address map for these control registers.

The core is configured by writing values to CONT\_REG1. Table 5 describes the values that can configure the CS3310 to different modes.

Resetting the core will cause the Control Registers to be set to their initial values shown in the Table 6.

**Table 4: Control Registers' Address Map**

Address	D7	D6	D5	D4	D3	D2	D1	D0
0	CONT_REG0							
	-	-	-	-	-	-	-	-
1	CONT_REG1							
	MODE1	VRATE2	VRATE1	VRATE0	MODE0	TRATE	-	DE

**Table 5: CONT\_REG 1**

Bit(s)	Name	Description
D7	MODE1	1: Viterbi Mode 0: Trellis Mode
D[6:4]	VRATE	Viterbi Mode Rates 000: Rate 1/2 001: Rate 1/3 010: Rate 2/3 011: Rate 3/4 100: Rate 5/6 101: Rate 7/8
D3	MODE0	1: Continuous Mode 0: Block Mode
D2	TRATE	Trellis Mode Rates 1: Rate 2/3 (8-PSK) 0: Rate 3/4 (16-PSK)
D1	NOT USED	NOT USED
D0	DE	1: Differential Encoding ON 0: Differential Encoding OFF

**Table 6: Control Register Bit Values at Reset**

Address	D7	D6	D5	D4	D3	D2	D1	D0
0	CONT_REG0							
	0	0	0	0	0	0	0	0
1	CONT_REG1							
	1	0	0	0	1	0	0	1



## CS3310 I/O TIMING DIAGRAMS

The following diagrams illustrate typical waveforms for three core configurations.

Continuous Mode  
Viterbi Mode  
Rate 3/4  
Differential Encoding

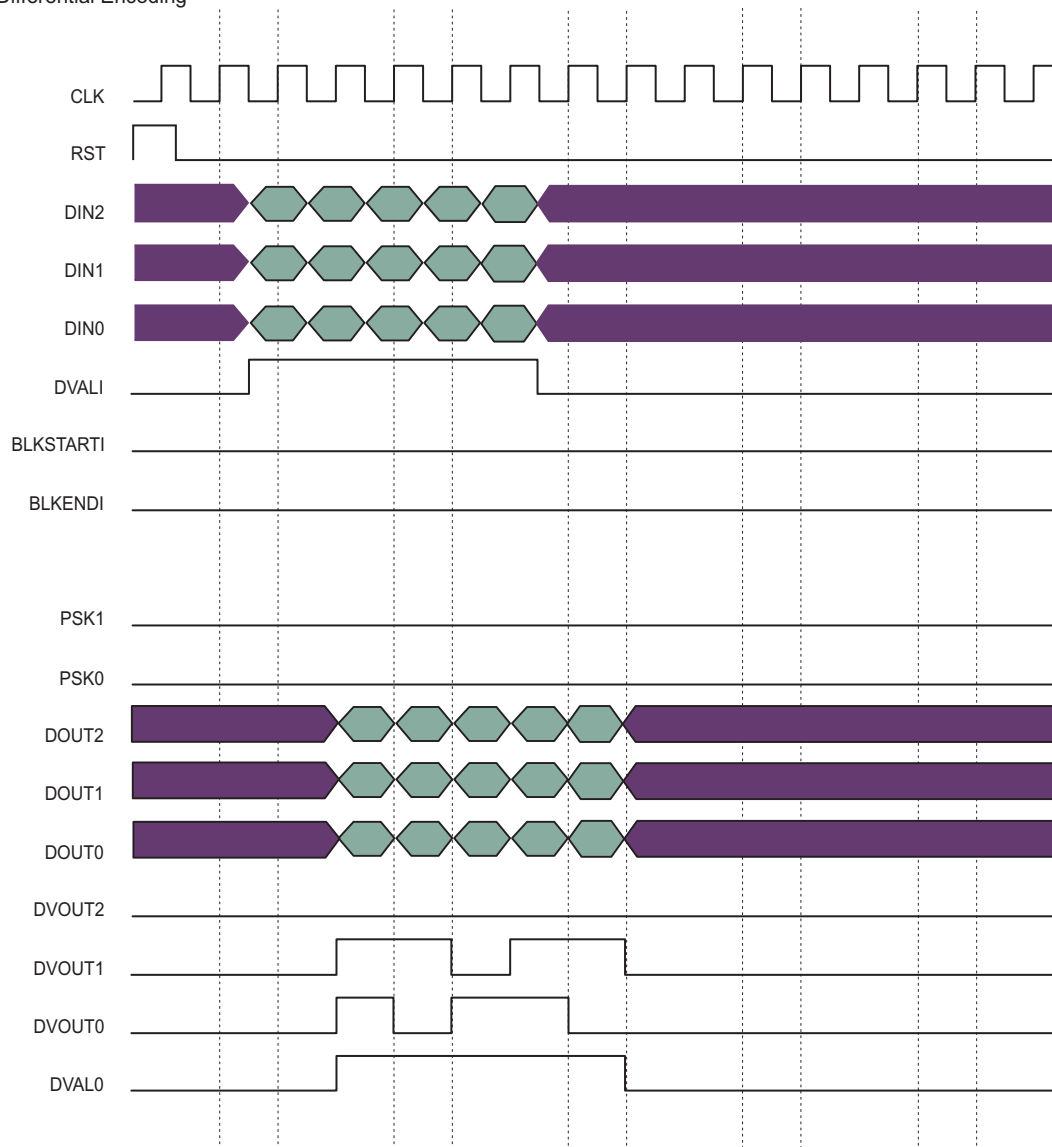
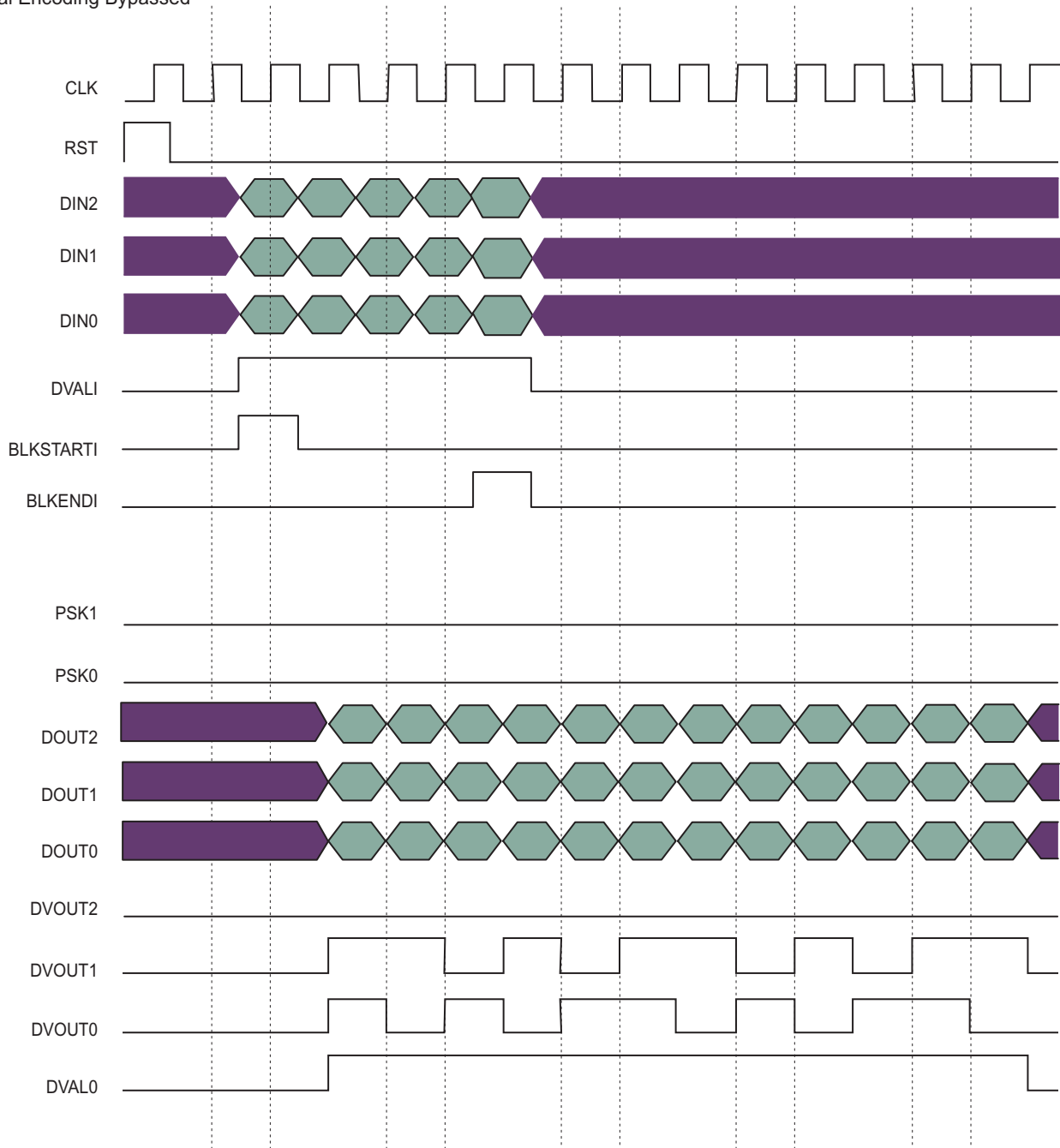


Figure 4: CS3310 Functional Timing Characteristics in Continuous Viterbi Mode

Block Mode  
Viterbi Mode  
Rate 5/6  
Differential Encoding Bypassed

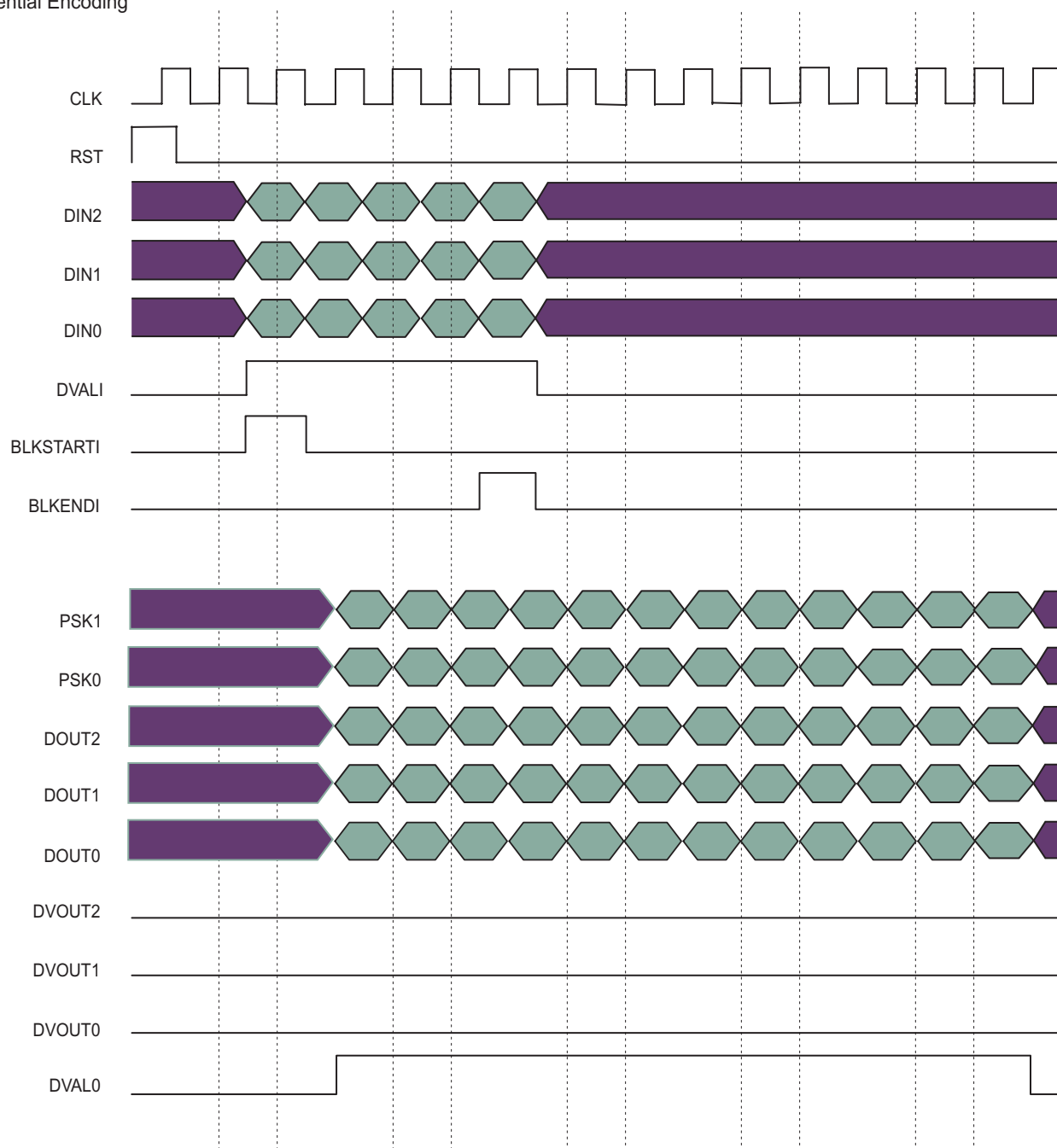


**Figure 5: CS3310 Functional Timing Characteristics in Block Viterbi Mode**



# CS3310 Programmable Convolution Encoder

Block Mode  
Trellis Mode  
Rate 3/4  
Differential Encoding



**Figure 6: CS3310 Functional Timing Characteristics in Block Trellis Mode**

## AVAILABILITY AND IMPLEMENTATION INFORMATION

### ASIC CORES

For applications that require the high performance, low cost and high integration of an ASIC, Amphion delivers the ASIC Core series of multimedia ASVCs that are pre-optimized to a targeted silicon technology by Amphion experts. Choose from off-the-shelf versions of the CS3310 available for many popular ASIC and foundry silicon supplier technologies or Amphion can port the CS3310 to a technology of your choice.

**Table 7: CS3310 ASIC Cores**

PRODUCT ID	SILICON VENDOR	PROCESS TECHNOLOGY	PERFORMANCE* (MSAMPLES/SEC)	LOGIC GATES**	AVAILABILITY
CS3310TK	TSMC	180nm using Artisan standard cell libraries	100	956	NOW

\*Performance figures based on silicon vendor design kit information. ASIC design is pre-layout using vendor-provided statistical wire loading information, under the following condition: ( $T_J = 125^{\circ}\text{C}$ ,  $V_{CC} -10\%$ )

\*\*Logic gates do not include clock circuitry

Consult your local Amphion representative for product specific performance information, current availability of individual products, and lead times on Optima core porting.

### PROGRAMMABLE LOGIC CORES

For ASIC prototyping or for projects requiring the fast time-to-market of a programmable logic solution, Amphion provides programmable logic core solutions that offer the silicon-aware performance tuning found in all Amphion products, combined with the rapid design times offered by today's leading programmable logic solutions.

**Table 8: CS3310 Programmable Logic Cores**

PRODUCT ID	SILICON VENDOR	PROGRAMMABLE LOGIC PRODUCT	PERFORMANCE* (MSAMPLES/SEC)	DEVICE RESOURCES USED (LOGIC)	AVAILABILITY
CS3310AA	Altera	Apex 20KE	50	158 LEs	NOW
CS3310XE	Xilinx	Virtex II	50	73 Slices	NOW

\*Performance represents core only under worst case commercial condition. Does not include timing effect of external logic and I/O circuitry.



# CS3310 Programmable Convolution Encoder



## ABOUT AMPHION

Amphion (formerly Integrated Silicon Systems) is the leading supplier of speech coding, video/image processing and channel coding ASVCs for system-on-a-chip (SoC) solutions in the telecommunications/Internet, consumer / communications and wireless markets.

Web: [www.amphion.com](http://www.amphion.com)

Email: [info@amphion.com](mailto:info@amphion.com)

## CORPORATE HEADQUARTERS

Amphion Semiconductor Ltd  
50 Malone Road  
Belfast BT9 5BS  
Northern Ireland, UK

Tel: +44 28 9050 4000

Fax: +44 28 9050 4001

## EUROPEAN SALES

Amphion Semiconductor Ltd  
CBXII, West Wing  
382-390 Midsummer Boulevard  
Central Milton Keynes  
MK9 2RG England, UK

Tel: +44 1908 847109

Fax: +44 1908 847580

## WORLDWIDE SALES & MARKETING

Amphion Semiconductor, Inc  
2001 Gateway Place, Suite 130W  
San Jose, CA 95110

Tel: (408) 441 1248

Fax: (408) 441 1239

## CANADA & EAST COAST US SALES

Amphion Semiconductor, Inc  
Montreal  
Quebec  
Canada

Tel: (450) 455 5544

Fax: (450) 455 5543

---

## SALES AGENTS

### Voyageur Technical Sales Inc

1 Rue Holiday  
Tour Est, Suite 501  
Point Claire, Quebec  
Canada H9R 5N3

Tel: (514) 693 5009

Fax: (514) 693 5007

### JASONTECH, INC

Hansang Building, Suite 300  
Bangyidong 181-3, Songpaku  
Seoul Korea 138-050

Tel: +82 2 420 6700

Fax: +82 2 420 8600

### Phoenix Technologies Ltd

3 Gavish Street  
Kfar-Saba, 44424  
Israel

Tel: +972 9 7644 800

Fax: +972 9 7644 801

### SPS-DA PTE LTD

21 Science Park Rd  
#03-19 The Aquarius  
Singapore Science Park II  
Singapore 117628

Tel: +65 774 9070

Fax: +65 774 9071

### SPINNAKER SYSTEMS INC

Hatchobori SF Bldg. 5F 3-12-8  
Hatchobori, Chuo-ku  
Tokyo 104-0033 Japan

Tel: +81 3 3551 2275

Fax: +81 3 3351 2614