CYD04S72V
CYD09S72V
CYD18S72V

FLEx72™ 3.3V 64K/128K/256K x 72 Synchronous Dual-Port RAM

Features

- True dual-ported memory cells that allow simultaneous access of the same memory location
- Synchronous pipelined operation
- Family of 4-Mbit, 9-Mbit and 18-Mbit devices
- Pipelined output mode allows fast operation
- 0.18-micron CMOS for optimum speed and power
- High-speed clock to data access
- 3.3V low power
  - Active as low as 225 mA (typ)
  - Standby as low as 55 mA (typ)
- Mailbox function for message passing
- Global master reset
- Separate byte enables on both ports
- Commercial and industrial temperature ranges
- IEEE 1149.1-compatible JTAG boundary scan
- 484-ball FBGA (1 mm pitch)
- Counter wrap around control
  - Internal mask register controls counter wrap-around
  - Counter-interrupt flags to indicate wrap-around
  - Memory block retransmit operation
- Counter readback on address lines
- Mask register readback on address lines
- Dual Chip Enables on both ports for easy depth expansion
- Seamless Migration to Next Generation Dual Port Family

Functional Description

The FLEx72 family includes 4-Mbit, 9-Mbit and 18-Mbit pipelined, synchronous, true dual-port static RAMs that are high-speed, low-power 3.3V CMOS. Two ports are provided, permitting independent, simultaneous access to any location in memory. The result of writing to the same location by more than one port at the same time is undefined. Registers on control, address, and data lines allow for minimal set-up and hold time.

During a Read operation, data is registered for decreased cycle time. Each port contains a burst counter on the input address register. After externally loading the counter with the initial address, the counter will increment the address internally (more details to follow). The internal write pulse width is independent of the duration of the R/W input signal. The internal write pulse is self-timed to allow the shortest possible cycle times.

A HIGH on $\overline{CE0}$ or LOW on CE1 for one clock cycle will power down the internal circuitry to reduce the static power consumption. One cycle with chip enables asserted is required to reactivate the outputs.

Additional features include: readback of burst-counter internal address value on address lines, counter-mask registers to control the counter wrap-around, counter interrupt (CNTINT) flags, readback of mask register value on address lines, retransmit functionality, interrupt flags for message passing, JTAG for boundary scan, and asynchronous Master Reset (MRST).

The CYD18S72V device have limited features. Please see “Address Counter and Mask Register Operations[16]” on page 6 for details.

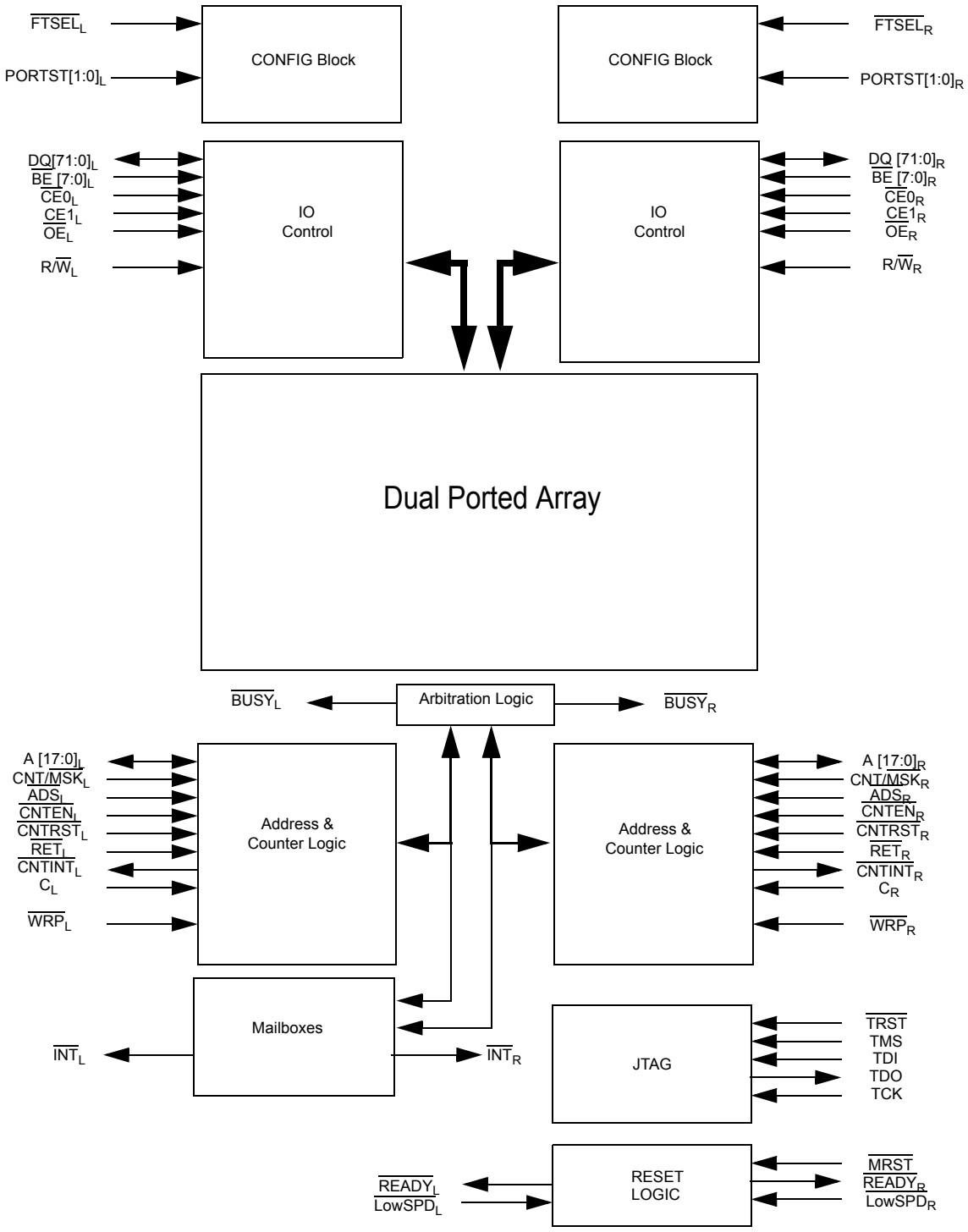
Seamless Migration to Next Generation Dual Port Family

Cypress offers a migration path for all devices to the next-generation devices in the Dual-Port family with a compatible footprint. Please contact Cypress Sales for more details

Table 1. Product Selection Guide

Density	4-Mbit (64K x 72)	9-Mbit (128K x 72)	18-Mbit (256K x 72)
Part Number	CYD04S72V	CYD09S72V	CYD18S72V
Max. Speed (MHz)	167	167	133
Max. Access Time - clock to Data (ns)	4.0	4.0	5.0
Typical operating current (mA)	225	270	410
Package	484-ball FBGA 23mm x 23mm	484-ball FBGA 23mm x 23mm	484-ball FBGA 23mm x 23mm

Logic Block Diagram[1]



Note:
1. CYD04S72V have 16 address bits, CYD09S72V have 17 address bits and CYD18S72V have 18 bits.

Pin Configuration

484-ball BGA
Top View
CYD04S72V / CYD09S72V / CYD18S72V

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	NC	DQ6 1L	DQ5 9L	DQ5 7L	DQ5 4L	DQ5 1L	DQ4 8L	DQ4 5L	DQ4 2L	DQ3 9L	DQ3 6L	DQ3 6R	DQ3 9R	DQ4 2R	DQ4 5R	DQ4 8R	DQ5 1R	DQ5 4R	DQ5 7R	DQ5 9R	DQ6 1R	NC
B	DQ6 3L	DQ6 2L	DQ6 0L	DQ5 8L	DQ5 5L	DQ5 2L	DQ4 9L	DQ4 6L	DQ4 3L	DQ4 0L	DQ3 7L	DQ3 7R	DQ4 0R	DQ4 3R	DQ4 6R	DQ4 9R	DQ5 2R	DQ5 5R	DQ5 8R	DQ6 0R	DQ6 2R	DQ6 3R
C	DQ6 5L	DQ6 4L	VSS	VSS	DQ5 6L	DQ5 3L	DQ5 0L	DQ4 7L	DQ4 4L	DQ4 1L	DQ3 8L	DQ3 8R	DQ4 1R	DQ4 4R	DQ4 7R	DQ5 0R	DQ5 3R	DQ5 6R	VSS	VSS	DQ6 4R	DQ6 5R
D	DQ6 7L	DQ6 6L	VSS	VSS	VSS	NC [2, 5]	NC [2, 5]	REV L[2,4]	LOW SPD L[2,4]	POR TST D0L [2,4]	NC [2, 5]	BUS YL [2, 5]	CNTI NTL [10]	POR TST D1L [2, 5]	REV R[2,4]	NC [2, 5]	NC [2, 5]	VSS	VSS	VSS	DQ6 6R	DQ6 7R
E	DQ6 9L	DQ6 8L	VDD IOL	VSS	VSS	VDD IOL	VDD IOL	VDD IOL	VDDI OL	VDDI OL	VTT L	VTT L	VTTL	VDDI OR	VDD IOR	VDD IOR	VDD IOR	NC	VSS	VDD IOR	DQ6 8R	DQ6 9R
F	DQ7 1L	DQ7 0L	CE1 L[8]	CE0 L [9]	VDD IOL	VDD IOL	VDD IOL	VDD IOL	VDDI OL	VCO RE	VCO RE	VCO RE	VCO RE	VDDI OR	VDD IOR	VDD IOR	VDD IOR	VDD IOR	CE0 R [9]	CE1 R[8]	DQ7 0R	DQ7 1R
G	A0L	A1L	RET L[2,3]	BE4 L	VDD IOL	VDD IOL	VRE FL [2, 4]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VRE FR [2, 4]	VDD IOR	VDD IOR	BE4 R	RET R[2,3]	A1R	A0R
H	A2L	A3L	WRP L[2,3]	BE5 L	VDD IOL	VDD IOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD IOR	VDD IOR	BE5 R	WRP R[2,3]	A3R	A2R
J	A4L	A5L	REA DYL [2, 5]	BE6 L	VDD IOL	VDD IOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD IOR	VDD IOR	BE6 R	REA DYR [2, 5]	A5R	A4R
K	A6L	A7L	NC	BE7 L	VTT L	VCO RE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCO RE	VDD IOR	BE7 R	NC	A7R	A6R
L	A8L	A9L	CL	OEL	VTT L	VCO RE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCO RE	VTT L	OER	CR	A9R	A8R
M	A10L	A11L	REV L [2,4]	BE3 L	VTT L	VCO RE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCO RE	VTT L	BE3 R	REV R[2,4]	A11 R	A10 R
N	A12L	A13L	ADS L [9]	BE2 L	VDD IOL	VCO RE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCO RE	VTT L	BE2 R	ADS R [9]	A13 R	A12 R
P	A14L	A15L	CNT/ MSK L[8]	BE1 L	VDD IOL	VDD IOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD IOR	VDD IOR	BE1 R	CNT/ MSK R[8]	A15 R	A14 R
R	A16L [6]	A17L [7]	CNT ENL [9]	BE0 L	VDD IOL	VDD IOL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD IOR	VDD IOR	BE0 R	CNT ENR [9]	A17 R [7]	A16 R [6]
T	A18L [2,5]	NC	CNT RST L [8]	INTL	VDD IOL	VDD IOL	VRE FL [2, 4]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VRE FR [2, 4]	VDD IOR	VDD IOR	INTR	CNT RST R[8]	NC	A18 R [2,5]
U	DQ3 5L	DQ3 4L	R/W L	REV L [2,4]	VDD IOL	VDD IOL	VDD IOL	VDD IOL	VDDI OL	VCO RE	VCO RE	VCO RE	VCO RE	VDDI OR	VDD IOR	VDD IOR	VDD IOR	VDD IOR	REV R[2,4]	R/W R	DQ3 4R	DQ3 5R
V	DQ3 3L	DQ3 2L	ETS ELL [2,3]	VDD IOL	NC	VDD IOL	VDD IOL	VDD IOL	VDDI OL	VTTL	VTT L	VTT L	VDDI OR	VDDI OR	VDD IOR	VDD IOR	VDD IOR	TRS T[2, 5]	VDD IOR	ETS ELR [2,3]	DQ3 2R	DQ3 3R
W	DQ3 1L	DQ3 0L	VSS	MBS T	VSS	NC [2, 5]	NC [2, 5]	REV L[2,4]	POR TST D1R [2, 5]	CNTI NTR [10]	BUS YR [2, 5]	NC [2, 5]	POR TST D0R [2,4]	LOW SPD R[2,4]	REV R[2,4]	NC [2, 5]	NC [2, 5]	VSS	TDI	TDO	DQ3 0R	DQ3 1R
Y	DQ2 9L	DQ2 8L	VSS	VSS	DQ2 0L	DQ1 7L	DQ1 4L	DQ1 1L	DQ8 L	DQ5 L	DQ2 L	DQ2 R	DQ5 R	DQ8 R	DQ1 1R	DQ1 4R	DQ1 7R	DQ2 0R	TMS	TCK	DQ2 8R	DQ2 9R
AA	DQ2 7L	DQ2 6L	DQ2 4L	DQ2 2L	DQ1 9L	DQ1 6L	DQ1 3L	DQ1 0L	DQ7 L	DQ4 L	DQ1 L	DQ1 R	DQ4 R	DQ7 R	DQ1 0R	DQ1 3R	DQ1 6R	DQ1 9R	DQ2 2R	DQ2 4R	DQ2 6R	DQ2 7R
AB	NC	DQ2 5L	DQ2 3L	DQ2 1L	DQ1 8L	DQ1 5L	DQ1 2L	DQ9 L	DQ6 L	DQ3 L	DQ0 L	DQ0 R	DQ3 R	DQ6 R	DQ9 R	DQ1 2R	DQ1 5R	DQ1 8R	DQ2 1R	DQ2 3R	DQ2 5R	NC

2. This ball will represent a next generation Dual-Port feature. For more information about this feature, contact Cypress Sales
3. Connect this ball to VDDIO. For more information about this next generation Dual-Port feature contact Cypress Sales.
4. Connect this ball to VSS. For more information about this next generation Dual-Port feature, contact Cypress Sales.
5. Leave this ball unconnected. For more information about this feature, contact Cypress Sales.
6. Leave this ball unconnected for a 64K x 72 configuration.
7. Leave this ball unconnected for 128K x 72 and 64K x72 configurations.
8. These balls are not applicable for CYD18S72V device. They need to be tied to VDDIO.
9. These balls are not applicable for CYD18S72V device. They need to be tied to VSS.
10. These balls are not applicable for CYD18S72V device. They need to be no connected.

Pin Definitions

Left Port	Right Port	Description
A_{0L}–A_{17L}	A_{0R}–A_{17R}	**Address Inputs**.
$\overline{BE}_{0L}$–$\overline{BE}_{7L}$	$\overline{BE}_{0R}$–$\overline{BE}_{7R}$	**Byte Enable Inputs**. Asserting these signals enables Read and Write operations to the corresponding bytes of the memory array.
$\overline{BUSY}_L$[2,5]	$\overline{BUSY}_R$[2,5]	**Port Busy Output**. When the collision is detected, a $\overline{BUSY}$ is asserted.
C_L	C_R	**Input Clock Signal**.
$\overline{CE0}_L$[9]	$\overline{CE0}_R$[9]	**Active Low Chip Enable Input**.
$CE1_L$[8]	$CE1_R$[8]	**Active High Chip Enable Input**.
DQ_{0L}–DQ_{71L}	DQ_{0R}–DQ_{71R}	**Data Bus Input/Output**.
$\overline{OE}_L$	$\overline{OE}_R$	**Output Enable Input**. This asynchronous signal must be asserted LOW to enable the DQ data pins during Read operations.
$\overline{INT}_L$	$\overline{INT}_R$	**Mailbox Interrupt Flag Output**. The mailbox permits communications between ports. The upper two memory locations can be used for message passing. $\overline{INT}_L$ is asserted LOW when the right port writes to the mailbox location of the left port, and vice versa. An interrupt to a port is deasserted HIGH when it reads the contents of its mailbox.
$\overline{LowSPD}_L$[2,4]	$\overline{LowSPD}_R$[2,4]	**Port Low Speed Select Input**. When operating at less than 100 MHz, the LowSPD disables the port DLL.
$PORTSTD[1:0]_L$[2,4,5]	$PORTSTD[1:0]_R$[2,4,5]	**Port Address/Control/Data I/O Standard Select Input**.
$R/\overline{W}_L$	$R/\overline{W}_R$	**Read/Write Enable Input**. Assert this pin LOW to write to, or HIGH to Read from the dual port memory array.
$\overline{READY}_L$[2,5]	$\overline{READY}_R$[2,5]	**Port Ready Output**. This signal will be asserted when a port is ready for normal operation.
$CNT/\overline{MSK}_L$[8]	$CNT/\overline{MSK}_R$[8]	**Port Counter/Mask Select Input**. Counter control input.
$\overline{ADS}_L$[9]	$\overline{ADS}_R$[9]	**Port Counter Address Load Strobe Input**. Counter control input.
$\overline{CNTEN}_L$[9]	$\overline{CNTEN}_R$[9]	**Port Counter Enable Input**. Counter control input.
$\overline{CNTRST}_L$[8]	$\overline{CNTRST}_R$[8]	**Port Counter Reset Input**. Counter control input.
$\overline{CNTINT}_L$[10]	$\overline{CNTINT}_R$[10]	**Port Counter Interrupt Output**. This pin is asserted LOW when the unmasked portion of the counter is incremented to all “1s”.
$\overline{WRP}_L$[2,3]	$\overline{WRP}_R$[2,3]	**Port Counter Wrap Input**. After the burst counter reaches the maximum count, if $\overline{WRP}$ is low, the unmasked counter bits will be set to 0. If high, the counter will be loaded with the value stored in the mirror register.
$\overline{RET}_L$[2,3]	$\overline{RET}_R$[2,3]	**Port Counter Retransmit Input**. Counter control input.
$\overline{FTSEL}_L$[2,3]	$\overline{FTSEL}_R$[2,3]	**Flow-Through Select**. Use this pin to select Flow-Through mode. When is de-asserted, the device is in pipelined mode.
$VREF_L$[2,5]	$VREF_R$[2,5]	**Port External High-Speed IO Reference Input**.
$VDDIO_L$	$VDDIO_R$	**Port IO Power Supply**.
$REV^{[2,4]}_L$	$REV^{[2,4]}_R$	**Reserved pins for future features**.
$\overline{MRST}$		**Master Reset Input**. $\overline{MRST}$ is an asynchronous input signal and affects both ports. A master reset operation is required at power-up.
$\overline{TRST}$[2,5]		**JTAG Reset Input**.
TMS		**JTAG Test Mode Select Input**. It controls the advance of JTAG TAP state machine. State machine transitions occur on the rising edge of TCK.

Pin Definitions (continued)

Left Port	Right Port	Description
TDI		**JTAG Test Data Input**. Data on the TDI input will be shifted serially into selected registers.
TCK		**JTAG Test Clock Input**.
TDO		**JTAG Test Data Output**. TDO transitions occur on the falling edge of TCK. TDO is normally three-stated except when captured data is shifted out of the JTAG TAP.
V_{SS}		**Ground Inputs**.
V_{CORE}		**Core Power Supply**.
V_{TTL}		**LVTTL Power Supply**.

Master Reset

The FLEx72 family devices undergo a complete reset by taking the MRST input LOW. MRST input can switch asynchronously to the clocks. MRST initializes the internal burst counters to zero, and the counter mask registers to all ones (completely unmasked). MRST also forces the mailbox interrupt (INT) flags and the Counter Interrupt (CNTINT) flags HIGH. MRST must be performed on the FLEx72 family devices after power-up.

Mailbox Interrupts

The upper two memory locations may be used for message passing and permit communications between ports. *Table 2* shows the interrupt operation for both ports using 18Mbit device as an example. The highest memory location, 3FFFF is the mailbox for the right port and 3FFFE is the mailbox for the left port. *Table 2.*shows that in order to set the $\overline{INT}_R$ flag, a write operation by the left port to address 3FFFF will assert $\overline{INT}_R$ LOW. At least one byte has to be active for a write to generate an interrupt. A valid Read of the 3FFFF location by the right port will reset $\overline{INT}_R$ HIGH. At least one byte has to be active in order for a read to reset the interrupt. When one port writes to the other port's mailbox, the $\overline{INT}$ of the port that the mailbox belongs to is asserted LOW.

The $\overline{INT}$ is reset when the owner (port) of the mailbox reads the contents of the mailbox. The interrupt flag is set in a flow-thru mode (i.e., it follows the clock edge of the writing port). Also, the flag is reset in a flow-thru mode (i.e., it follows the clock edge of the reading port).

Each port can read the other port's mailbox without resetting the interrupt. And each port can write to its own mailbox without setting the interrupt. If an application does not require message passing, $\overline{INT}$ pins should be left open.

Table 2. Interrupt Operation Example [1, 11, 12, 13]

Function	Left Port				Right Port			
	$R/\overline{W}_L$	$\overline{CE}_L$	A_{0L-17L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	A_{0R-17R}	$\overline{INT}_R$
Set Right $\overline{INT}_R$ Flag	L	L	3FFFF	X	X	X	X	L
Reset Right $\overline{INT}_R$ Flag	X	X	X	X	H	L	3FFFF	H
Set Left $\overline{INT}_L$ Flag	X	X	X	L	L	L	3FFFE	X
Reset Left $\overline{INT}_L$ Flag	H	L	3FFFE	H	X	X	X	X

Note:
11. $\overline{CE}$ is internal signal. $\overline{CE}$ = LOW if $\overline{CE}_0$ = LOW and CE_1 = HIGH. For a single Read operation, CE only needs to be asserted once at the rising edge of the CLK and can be deasserted after that. Data will be out after the following CLK edge and will be three-stated after the next CLK edge.
12. $\overline{OE}$ is "Don't Care" for mailbox operation.
13. At least one of $\overline{BE0}$ or $\overline{BE7}$ must be LOW.

Table 3. Address Counter and Counter Mask Register Control Operation (Any Port) [14,15]

CLK	MRST	CNT/MSK	CNTRST	ADS	CNTEN	Operation	Description
X	L	X	X	X	X	Master Reset	Reset address counter to all 0s and mask register to all 1s.
⎍	H	H	L	X	X	Counter Reset	Reset counter unmasked portion to all 0s.
⎍	H	H	H	L	L	Counter Load	Load counter with external address value presented on address lines.
⎍	H	H	H	L	H	Counter Readback	Read out counter internal value on address lines.
⎍	H	H	H	H	L	Counter Increment	Internally increment address counter value.
⎍	H	H	H	H	H	Counter Hold	Constantly hold the address value for multiple clock cycles.
⎍	H	L	L	X	X	Mask Reset	Reset mask register to all 1s.
⎍	H	L	H	L	L	Mask Load	Load mask register with value presented on the address lines.
⎍	H	L	H	L	H	Mask Readback	Read out mask register value on address lines.
⎍	H	L	H	H	X	Reserved	Operation undefined

Note:
14. X" = "Don't Care," "H" = HIGH, "L" = LOW.
15. Counter operation and mask register operation is independent of chip enables.

Address Counter and Mask Register Operations[16]

This section describes the features only apply to 4Mbit and 9Mbit devices, not to 18Mbit device. Each port have a programmable burst address counter. The burst counter contains three registers: a counter register, a mask register, and a mirror register.

The **counter register** contains the address used to access the RAM array. It is changed only by the Counter Load, Increment, Counter Reset, and by master reset (MRST) operations.

The **mask register** value affects the Increment and Counter Reset operations by preventing the corresponding bits of the counter register from changing. It also affects the counter interrupt output (CNTINT). The mask register is changed only by the Mask Load and Mask Reset operations, and by the MRST. The mask register defines the counting range of the counter register. It divides the counter register into two regions: zero or more "0s" in the most significant bits define the masked region, one or more "1s" in the least significant bits define the unmasked region. Bit 0 may also be "0," masking the least significant counter bit and causing the counter to increment by two instead of one.

The mirror register is used to reload the counter register on increment operations (see "retransmit," below). It always contains the value last loaded into the counter register, and is changed only by the Counter Load, and Counter Reset operations, and by the MRST.

Table 3 summarizes the operation of these registers and the required input control signals. The MRST control signal is asynchronous. All the other control signals in *Table 3* (CNT/MSK, CNTRST, ADS, CNTEN) are synchronized to the port's CLK. All these counter and mask operations are independent of the port's chip enable inputs (CE0 and CE1)

Counter enable (CNTEN) inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for fast, interleaved memory applications. A port's burst counter is loaded when the port's address strobe (ADS) and CNTEN signals are LOW. When the port's CNTEN is asserted and the ADS is deasserted, the address counter will increment on each LOW to HIGH transition of that port's clock signal. This will Read/Write one word from/into each successive address location until CNTEN is deasserted. The counter can address the entire memory array, and will loop back to the start. Counter reset (CNTRST) is used to reset the unmasked portion of the burst counter to 0s. A counter-mask register is used to control the counter wrap.

Counter Reset Operation

All unmasked bits of the counter and mirror registers are reset to "0." All masked bits remain unchanged. A Mask Reset followed by a Counter Reset will reset the counter and mirror registers to 00000, as will master reset (MRST).

Counter Load Operation

The address counter and mirror registers are both loaded with the address value presented at the address lines.

Counter Increment Operation

Once the address counter register is initially loaded with an external address, the counter can internally increment the address value, potentially addressing the entire memory array. Only the unmasked bits of the counter register are incremented. The corresponding bit in the mask register must be a "1" for a counter bit to change. The counter register is incremented by 1 if the least significant bit is unmasked, and by 2 if it is masked. If all unmasked bits are "1," the next increment

will wrap the counter back to the initially loaded value. If an Increment results in all the unmasked bits of the counter being "1s," a counter interrupt flag (CNTINT) is asserted. The next Increment will return the counter register to its initial value, which was stored in the mirror register. The counter address can instead be forced to loop to 00000 by externally connecting CNTINT to CNTRST.[17] An increment that results in one or more of the unmasked bits of the counter being "0" will de-assert the counter interrupt flag. The example in *Figure 2* shows the counter mask register loaded with a mask value of 0003Fh unmasking the first 6 bits with bit "0" as the LSB and bit "16" as the MSB. The maximum value the mask register can be loaded with is 1FFFFh. Setting the mask register to this value allows the counter to access the entire memory space. The address counter is then loaded with an initial value of 8h. The base address bits (in this case, the 6th address through the 16th address) are loaded with an address value but do not increment once the counter is configured for increment operation. The counter address will start at address 8h. The counter will increment its internal address value till it reaches the mask register value of 3Fh. The counter wraps around the memory block to location 8h at the next count. CNTINT is issued when the counter reaches its maximum value.

Counter Hold Operation

The value of all three registers can be constantly maintained unchanged for an unlimited number of clock cycles. Such operation is useful in applications where wait states are needed, or when address is available a few cycles ahead of data in a shared bus interface.

Counter Interrupt

The counter interrupt ($\overline{\text{CNTINT}}$) is asserted LOW when an increment operation results in the unmasked portion of the counter register being all "1s." It is deasserted HIGH when an Increment operation results in any other value. It is also de-asserted by Counter Reset, Counter Load, Mask Reset and Mask Load operations, and by $\overline{\text{MRST}}$.

Counter Readback Operation

The internal value of the counter register can be read out on the address lines. Readback is pipelined; the address will be valid t_{CA2} after the next rising edge of the port's clock. If address readback occurs while the port is enabled ($\overline{\text{CE0}}$ LOW and CE1 HIGH), the data lines (DQs) will be three-stated. *Figure 1* shows a block diagram of the operation.

Retransmit

Retransmit is a feature that allows the Read of a block of memory more than once without the need to reload the initial address. This eliminates the need for external logic to store and route data. It also reduces the complexity of the system design and saves board space. An internal "mirror register" is used to store the initially loaded address counter value. When the counter unmasked portion reaches its maximum value set by the mask register, it wraps back to the initial value stored in this "mirror register." If the counter is continuously configured in increment mode, it increments again to its maximum value and wraps back to the value initially stored into the "mirror register." Thus, the repeated access of the same data is allowed without the need for any external logic.

Mask Reset Operation

The mask register is reset to all "1s," which unmasks every bit of the counter. Master reset ($\overline{\text{MRST}}$) also resets the mask register to all "1s."

Mask Load Operation

The mask register is loaded with the address value presented at the address lines. Not all values permit correct increment operations. Permitted values are of the form $2^n - 1$ or $2^n - 2$. From the most significant bit to the least significant bit, permitted values have zero or more "0s," one or more "1s," or one "0." Thus 1FFFF, 003FE, and 00001 are permitted values, but 1F0FF, 003FC, and 00000 are not.

Mask Readback Operation

The internal value of the mask register can be read out on the address lines. Readback is pipelined; the address will be valid t_{CM2} after the next rising edge of the port's clock. If mask readback occurs while the port is enabled ($\overline{\text{CE0}}$ LOW and CE1 HIGH), the data lines (DQs) will be three-stated. *Figure 1* shows a block diagram of the operation.

Counting by Two

When the least significant bit of the mask register is "0," the counter increments by two. This may be used to connect the x72 devices as a 144-bit single port SRAM in which the counter of one port counts even addresses and the counter of the other port counts odd addresses. This even-odd address scheme stores one half of the 144-bit data in even memory locations, and the other half in odd memory locations.

Notes:

16. The CYD04S72V has 16 address bits and a maximum address value of FFFF. The CYD09S72V has 17 address bits and a maximum address value of 1FFFF. The CYD18S72V has 18 address bits and a maximum address value of 3FFFF.
17. CNTINT and CNTRST specs are guaranteed by design to operate properly at speed grade operating frequency when tied together.

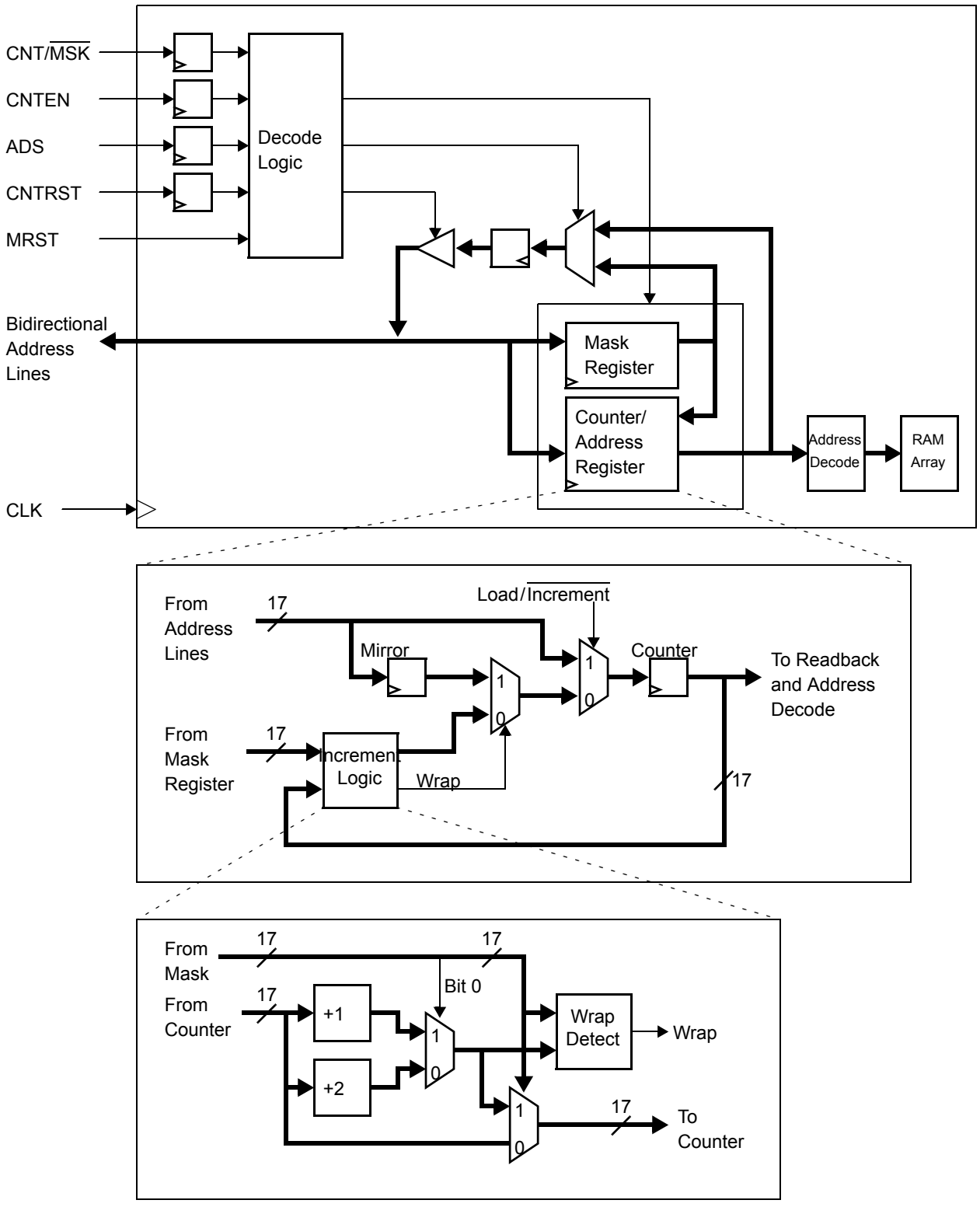


Figure 1. Counter, Mask, and Mirror Logic Block Diagram[1]

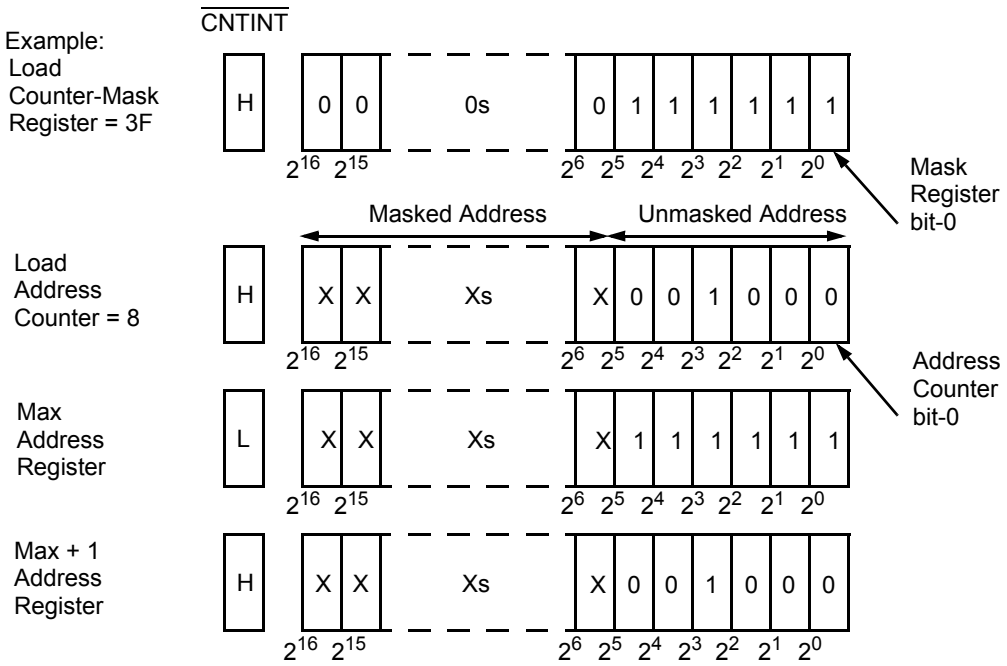


Figure 2. Programmable Counter-Mask Register Operation[1, 18]

IEEE 1149.1 Serial Boundary Scan (JTAG)[19]

The FLEx72 incorporates an IEEE 1149.1 serial boundary scan test access port (TAP). The TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1-compliant TAPs. The TAP operates using JEDEC-standard 3.3V I/O logic levels. It is composed of three input connections and one output connection required by the test logic defined by the standard.

Performing a TAP Reset

A reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This reset does not affect the operation of the FLEx72 family and may be performed while the device is operating. An MRST must be performed on the FLEx72 after power-up.

Performing a Pause/Restart

When a SHIFT-DR PAUSE-DR SHIFT-DR is performed the scan chain will output the next bit in the chain twice. For example, if the value expected from the chain is 1010101, the device will output a 11010101. This extra bit will cause some testers to report an erroneous failure for the FLEx72 in a scan test. Therefore the tester should be configured to never enter the PAUSE-DR state.

Boundary Scan Hierarchy for FLEx72 Family

Internally, the CYD04S72V and CYD09S72V have two DIEs while CYD18S72V have four DIEs. Each DIE contains all the circuitry required to support boundary scan testing. The circuitry includes the TAP, TAP controller, instruction register, and data registers. The circuity and operation of the DIE boundary scan are described in detail below. The scan chain of each DIE is connected serially to form the scan chain of the FLEx72 family as shown in *Figure 3*. TMS and TCK are connected in parallel to each DIE to drive all 4 TAP controllers in unison. In many cases, each DIE will be supplied with the same instruction. In other cases, it might be useful to supply different instructions to each DIE. One example would be testing the device ID of one DIE while bypassing the others.

Each pin of FLEx72 family is typically connected to multiple DIEs. For connectivity testing with the EXTEST instruction, it is desirable to check the internal connections between DIEs as well as the external connections to the package. This can be accomplished by merging the netlist of the devices with the netlist of the user's circuit board. To facilitate boundary scan testing of the devices, Cypress provides the BSDL file for each DIE, the internal netlist of the device, and a description of the device scan chain. The user can use these materials to easily integrate the devices into the board's boundary scan environment. Further information can be found in the Cypress application note *Using JTAG Boundary Scan For System In a Package (SIP) Dual-Port SRAMs*.

Notes:
18. The "X" in this diagram represents the counter upper bits.
19. Boundary scan is IEEE 1149.1-compatible. See "Performing a Pause/Restart" for deviation from strict 1149.1 compliance.

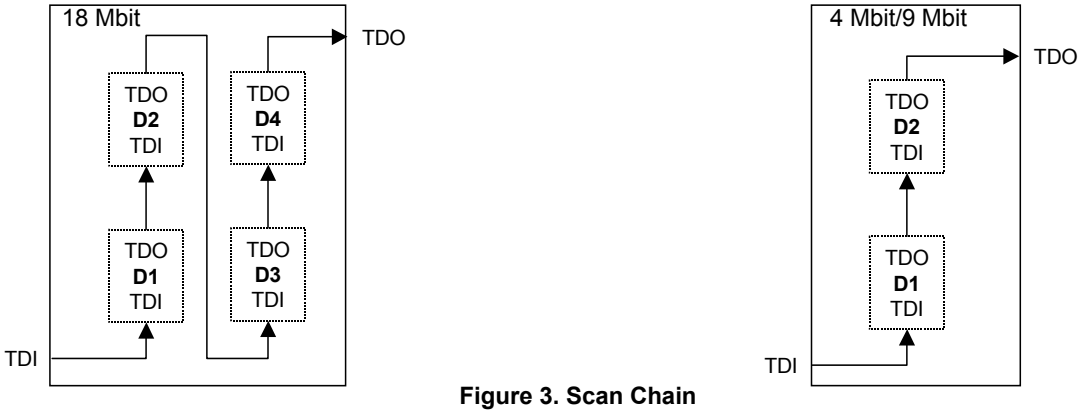


Figure 3. Scan Chain

Table 4. Identification Register Definitions

Instruction Field	Value	Description
Revision Number(31:28)	0h	Reserved for version number
Cypress Device(27:12)	C002h	Defines Cypress DIE number for CYD18S72V and CYD09S72V.
	C001h	Defines Cypress DIE number for CYD04S72V
Cypress JDEC ID(11:1)	034h	Allows unique identification of FLEx72 family device vendor
ID Register Presence (0)	1	Indicates the presence of an ID register

Table 5. Scan Registers Sizes

Register Name	Bit Size
Instruction	4
Bypass	1
Identification	32
Boundary Scan	n [20]

Table 6. Instruction Identification Codes

Instruction	Code	Description
EXTEST	0000	Captures the Input/Output ring contents. Places the BSR between the TDI and TDO.
BYPASS	1111	Places the BYR between TDI and TDO.
IDCODE	1011	Loads the IDR with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0111	Places BYR between TDI and TDO. Forces all FLEx72 output drivers to a High-Z state.
CLAMP	0100	Controls boundary to 1/0. Places BYR between TDI and TDO.
SAMPLE/PRELOAD	1000	Captures the input/output ring contents. Places BSR between TDI and TDO.
NBSRST	1100	Resets the non-boundary scan logic. Places BYR between TDI and TDO.
RESERVED	All other codes	Other combinations are reserved. Do not use other than the above.

Note:
20. See details in the device BSDL files

Maximum Ratings [21]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to + 150°C

Ambient Temperature with Power Applied.....–55°C to + 125°C

Supply Voltage to Ground Potential ..... –0.5V to + 4.6V

DC Voltage Applied to Outputs in High-Z State.....–0.5V to V_{DD} + 0.5V

DC Input Voltage ..... –0.5V to V_{DD} + 0.5V[22]

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2000V (JEDEC JESD22-A114-2000B)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{CORE}
Commercial	0°C to +70°C	3.3V ± 165 mV	1.8V ± 100 mV
Industrial	–40°C to +85°C	3.3V ± 165 mV	1.8V ± 100mV

Electrical Characteristics Over the Operating Range

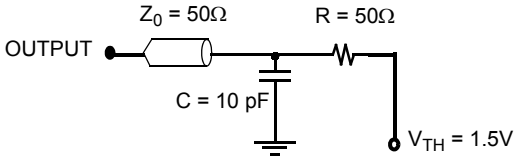
Parameter	Description	Part No.	-167			-133			-100			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ	Max	
V_{OH}	Output HIGH Voltage (V_{DD} = Min., I_{OH}= –4.0 mA)		2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage (V_{DD} = Min., I_{OL}= +4.0 mA)				0.4			0.4			0.4	V
V_{IH}	Input HIGH Voltage		2.0			2.0			2.0			V
V_{IL}	Input LOW Voltage				0.8			0.8			0.8	V
I_{OZ}	Output Leakage Current		–10		10	–10		10	-10		10	µA
I_{IX1}	Input Leakage Current Except TDI, TMS, MRST		–10		10	–10		10	-10		10	µA
I_{IX2}	Input Leakage Current TDI, TMS, MRST		–0.1		1.0	–0.1		1.0	-0.1		1.0	mA
I_{CC}	Operating Current (V_{DD} = Max.,I_{OUT} = 0 mA), Outputs Disabled	CYD04S72V CYD09S72V		225	300		225	300				mA
		CYD18S72V					410	580		315	450	mA
I_{SB1}	Standby Current (Both Ports TTL Level) CE_L and $CE_R \geq V_{IH}$, f = f_{MAX}	CYD04S72V CYD09S72V		90	115		90	115				mA
I_{SB2}	Standby Current (One Port TTL Level) CE_L | $CE_R \geq V_{IH}$, f = f_{MAX}	CYD04S72V CYD09S72V		160	210		160	210				mA
I_{SB3}	Standby Current (Both Ports CMOS Level) CE_L and $CE_R \geq$ V_{DD} – 0.2V, f = 0	CYD04S72V CYD09S72V		55	75		55	75				mA
I_{SB4}	Standby Current (One Port CMOS Level) CE_L | $CE_R \geq V_{IH}$, f = f_{MAX}	CYD04S72V CYD09S72V		160	210		160	210				mA
I_{SB5}	Operating Current (VDDIO = Max,Iout=0mA,f=0) Outputs Disabled	CYD18S72V						75			75	mA
I_{CORE}	Core Operating Current for (V_{DD} = Max.,I_{OUT} = 0 mA), Outputs Disabled			0	0		0	0		0	0	mA

Capacitance [23]

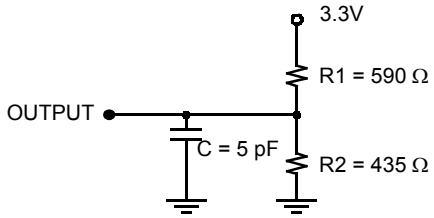
Part#	Parameter	Description	Test Conditions	Max.	Unit
CYD04S72V CYD09S72V	C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V	20	pF
	C_{OUT}	Output Capacitance		10[24]	pF
CYD18S72V	C_{IN}	Input Capacitance		40	pF
	C_{OUT}	Output Capacitance		20	pF

Note:
21. The voltage on any input or I/O pin can not exceed the power pin during power-up.
22. Pulse width < 20 ns.
23. C_{OUT} also references $C_{I/O}$

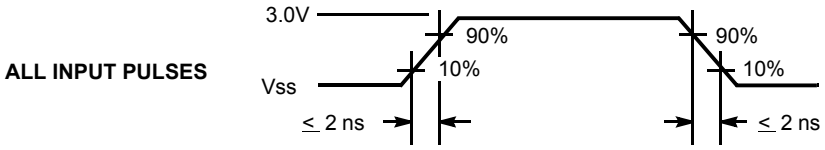
AC Test Load and Waveforms



(a) Normal Load (Load 1)



(b) Three-state Delay (Load 2)



Switching Characteristics Over the Operating Range

Parameter	Description	-167		-133				-100		Unit
		CYD04S72V CYD09S72V		CYD04S72V CYD09S72V		CYD18S72V		CYD18S72V		
		Min.	Max.	Min.	Max.	Min.	Max	Min.	Max	
f_{MAX2}	Maximum Operating Frequency		167		133		133		100	MHz
t_{CYC2}	Clock Cycle Time	6.0		7.5		7.5		10		ns
t_{CH2}	Clock HIGH Time	2.7		3.0		3.4		4.5		ns
t_{CL2}	Clock LOW Time	2.7		3.0		3.4		4.5		ns
t_R[25]	Clock Rise Time		2.0		2.0		2.0		3.0	ns
t_F[25]	Clock Fall Time		2.0		2.0		2.0		3.0	ns
t_{SA}	Address Set-up Time	2.3		2.5		2.2		2.7		ns
t_{HA}	Address Hold Time	0.6		0.6		1.0		1.0		ns
t_{SB}	Byte Select Set-up Time	2.3		2.5		2.2		2.7		ns
t_{HB}	Byte Select Hold Time	0.6		0.6		1.0		1.0		ns
t_{SC}	Chip Enable Set-up Time	2.3		2.5		NA		NA		ns
t_{HC}	Chip Enable Hold Time	0.6		0.6		NA		NA		ns
t_{SW}	R/$\overline{W}$ Set-up Time	2.3		2.5		2.2		2.7		ns
t_{HW}	R/$\overline{W}$ Hold Time	0.6		0.6		1.0		1.0		ns
t_{SD}	Input Data Set-up Time	2.3		2.5		2.2		2.7		ns
t_{HD}	Input Data Hold Time	0.6		0.6		1.0		1.0		ns
t_{SAD}	$\overline{ADS}$ Set-up Time	2.3		2.5		NA		NA		ns
t_{HAD}	$\overline{ADS}$ Hold Time	0.6		0.6		NA		NA		ns
t_{SCN}	$\overline{CNTEN}$ Set-up Time	2.3		2.5		NA		NA		ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0.6		0.6		NA		NA		ns
t_{SRST}	$\overline{CNTRST}$ Set-up Time	2.3		2.5		NA		NA		ns

Switching Characteristics Over the Operating Range (continued)

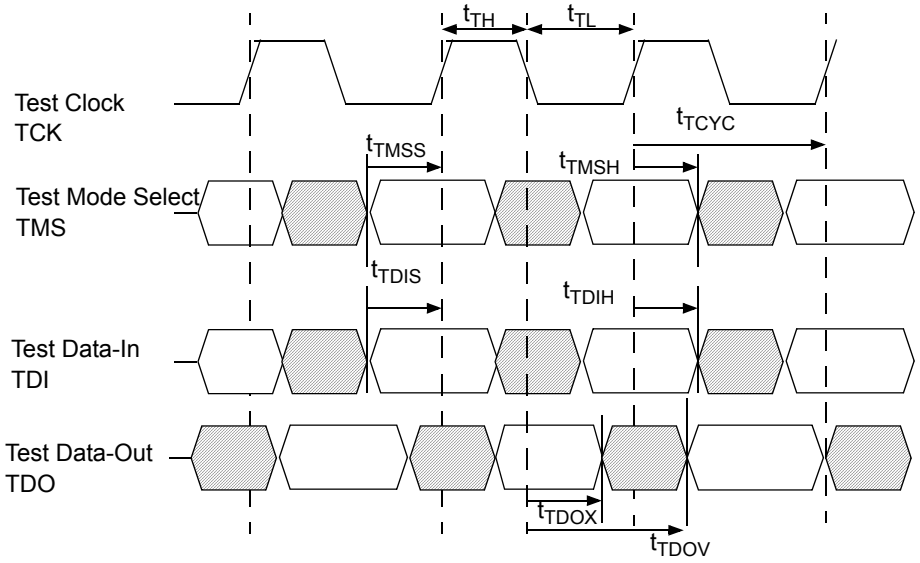
Parameter	Description	-167		-133				-100		Unit
		CYD04S72V CYD09S72V		CYD04S72V CYD09S72V		CYD18S72V		CYD18S72V		
		Min.	Max.	Min.	Max.	Min.	Max	Min.	Max	
t_{HRST}	$\overline{CNTRST}$ Hold Time	0.6		0.6		NA		NA		ns
t_{SCM}	CNT/$\overline{MSK}$ Set-up Time	2.3		2.5		NA		NA		ns
t_{HCM}	CNT/$\overline{MSK}$ Hold Time	0.6		0.6		NA		NA		ns
t_{OE}	Output Enable to Data Valid		4.0		4.4		5.5		5.5	ns
t_{OLZ}[26, 27]	$\overline{OE}$ to Low Z	0		0		0		0		ns
t_{OHZ}[26, 27]	$\overline{OE}$ to High Z	0	4.0	0	4.4	0	5.5	0	5.5	ns
t_{CD2}	Clock to Data Valid		4.0		4.4		5.0		5.2	ns
t_{CA2}	Clock to Counter Address Valid		4.0		4.4		NA		NA	ns
t_{CM2}	Clock to Mask Register Readback Valid		4.0		4.4		NA		NA	ns
t_{DC}	Data Output Hold After Clock HIGH	1.0		1.0		1.0		1.0		ns
t_{CKHZ}[26, 27]	Clock HIGH to Output High Z	0	4.0	0	4.4	0	4.7	0	5.0	ns
t_{CKLZ}[26, 27]	Clock HIGH to Output Low Z	1.0	4.0	1.0	4.4	1.0	4.7	1.0	5.0	ns
t_{SINT}	Clock to $\overline{INT}$ Set Time	0.5	6.7	0.5	7.5	0.5	7.5	0.5	10	ns
t_{RINT}	Clock to $\overline{INT}$ Reset Time	0.5	6.7	0.5	7.5	0.5	7.5	0.5	10	ns
t_{SCINT}	Clock to $\overline{CNTINT}$ Set Time	0.5	5.0	0.5	5.7	NA	NA	NA	NA	ns
t_{RCINT}	Clock to $\overline{CNTINT}$ Reset time	0.5	5.0	0.5	5.7	NA	NA	NA	NA	ns
Port to Port Delays										
t_{CCS}	Clock to Clock Skew	5.2		6.0		5.7		8.0		ns
Master Reset Timing										
t_{RS}	Master Reset Pulse Width	5.0		5.0		5.0		5.0		cycles
t_{RSS}	Master Reset Set-up Time	6.0		6.0		6.0		8.5		ns
t_{RSR}	Master Reset Recovery Time	5.0		5.0		5.0		5.0		cycles
t_{RSF}	Master Reset to Outputs Inactive		10.0		10.0		10.0		10.0	ns
$t_{RSCNTINT}$	Master Reset to Counter Interrupt Flag Reset Time		10.0		10.0		NA		NA	ns

Notes:
24. Except $\overline{INT}$ and $\overline{CNTINT}$ which are 20pF
25. Except JTAG signal (tr and tf < 10ns max)
26. This parameter is guaranteed by design, but is not production tested
27. Test conditions used are Load 2

JTAG Timing Characteristics

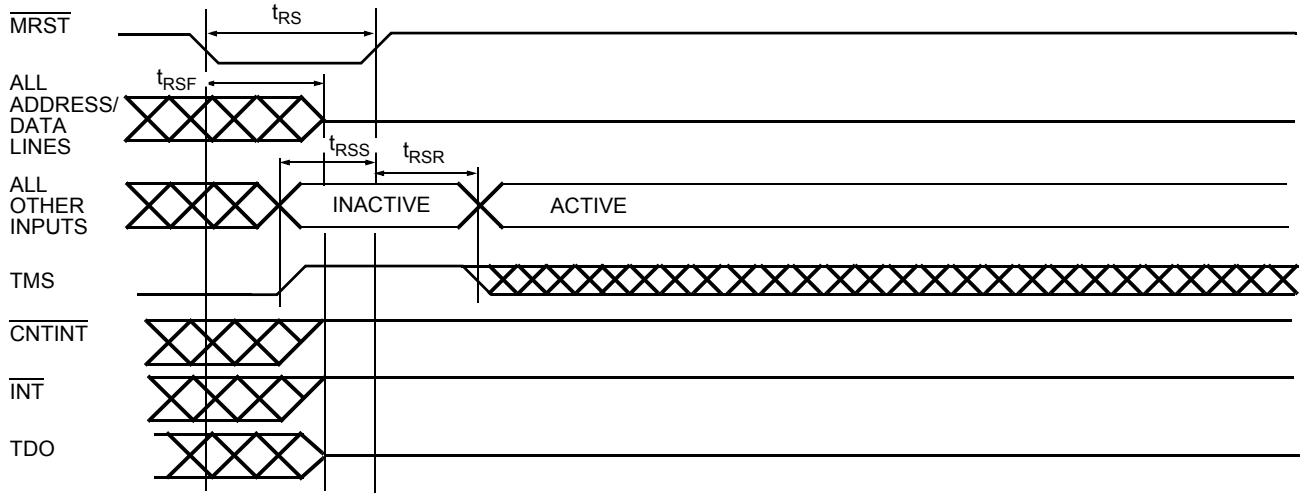
Parameter	Description	CYD04S72V CYD09S72V CYD18S72V -167/-133/-100 Min.	Max.	Unit
f_{JTAG}	Maximum JTAG TAP Controller Frequency		10	MHz
t_{TCYC}	TCK Clock Cycle Time	100		ns
t_{TH}	TCK Clock HIGH Time	40		ns
t_{TL}	TCK Clock LOW Time	40		ns
t_{TMSS}	TMS Set-up to TCK Clock Rise	10		ns
t_{TMSH}	TMS Hold After TCK Clock Rise	10		ns
t_{TDIS}	TDI Set-up to TCK Clock Rise	10		ns
t_{TDIH}	TDI Hold After TCK Clock Rise	10		ns
t_{TDOV}	TCK Clock LOW to TDO Valid		30	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

Switching Waveforms

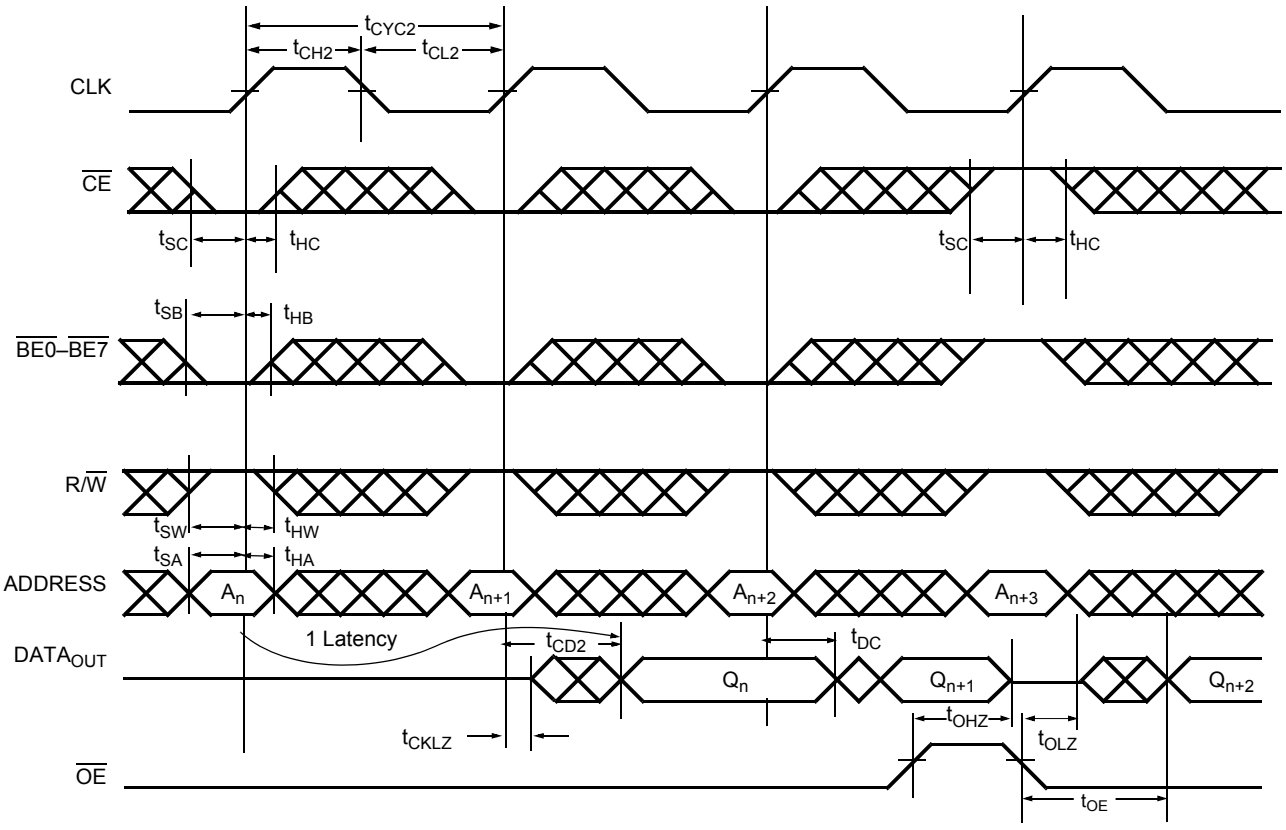


Switching Waveforms (continued)

Master Reset



Read Cycle[11, 28, 29, 30, 31]

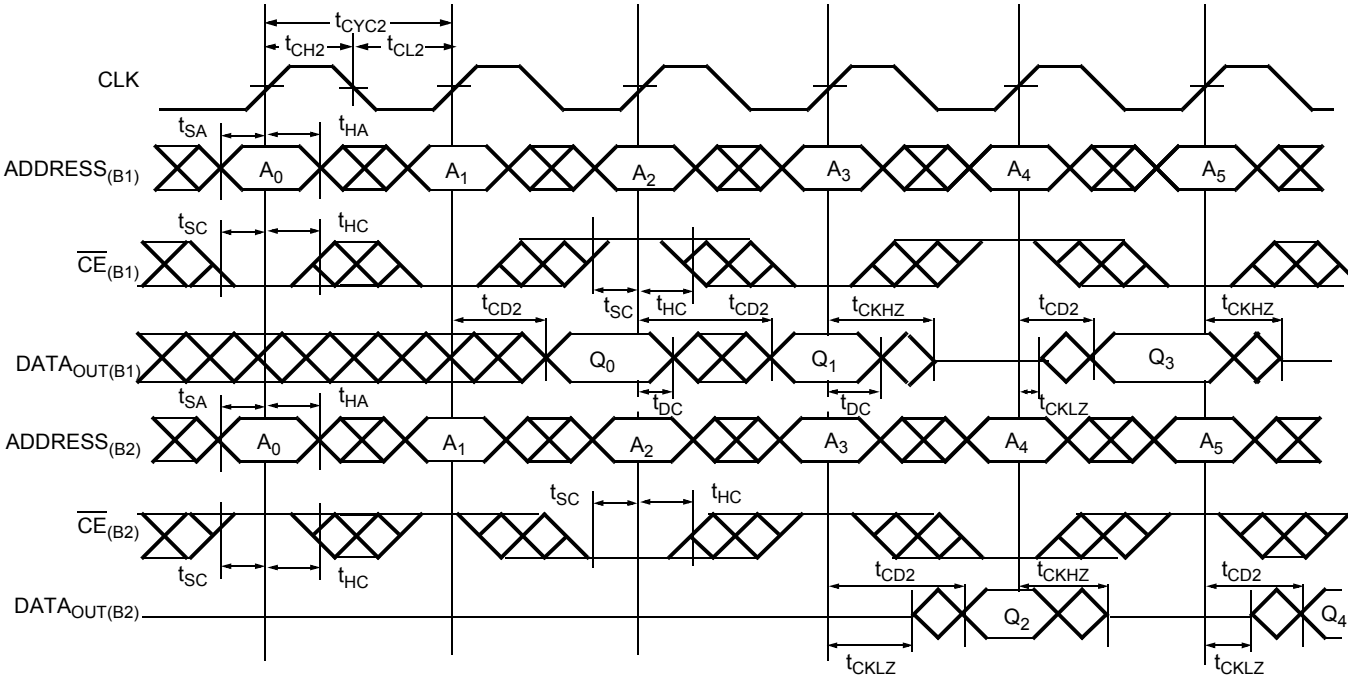


Notes:

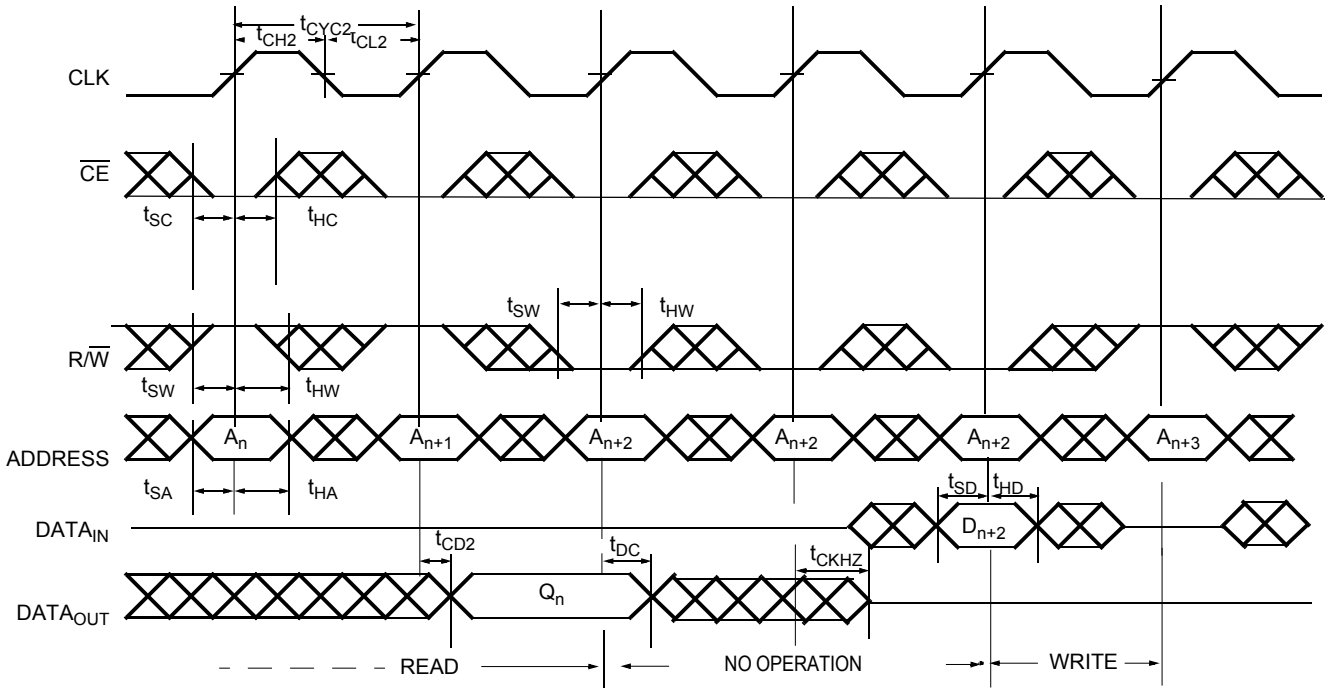
28. OE is asynchronously controlled; all other inputs (excluding MRST and JTAG) are synchronous to the rising clock edge.
29. ADS = CNTEN = LOW, and MRST = CNTRST = CNT/MSK = HIGH.
30. The output is disabled (high-impedance state) by CE = V_{IH} following the next rising edge of the clock.
31. Addresses do not have to be accessed sequentially since ADS = CNTEN = V_{IL} with CNT/MSK = V_{IH} constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

Switching Waveforms (continued)

Bank Select Read[32, 33]



Read-to-Write-to-Read ($\overline{OE}$ = LOW)[31, 34, 35, 36, 37]

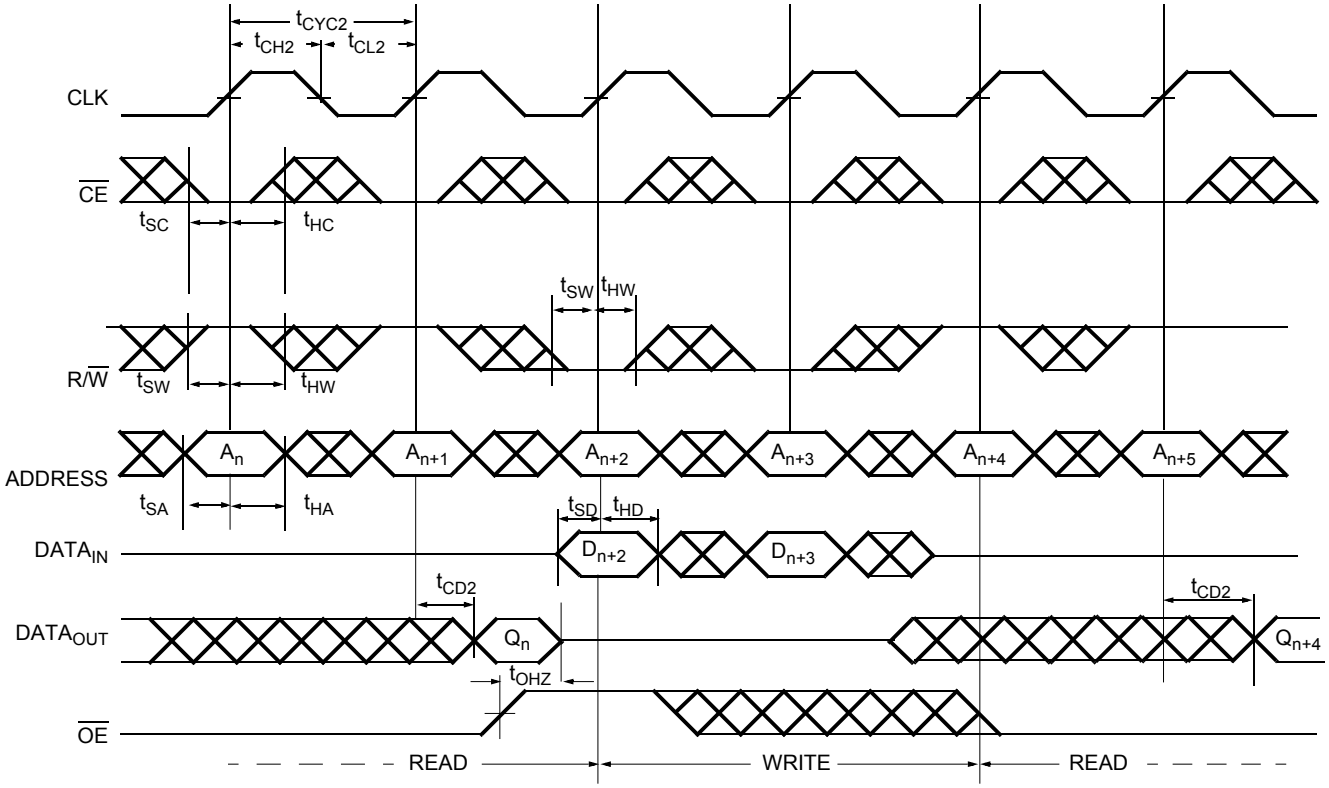


Notes:

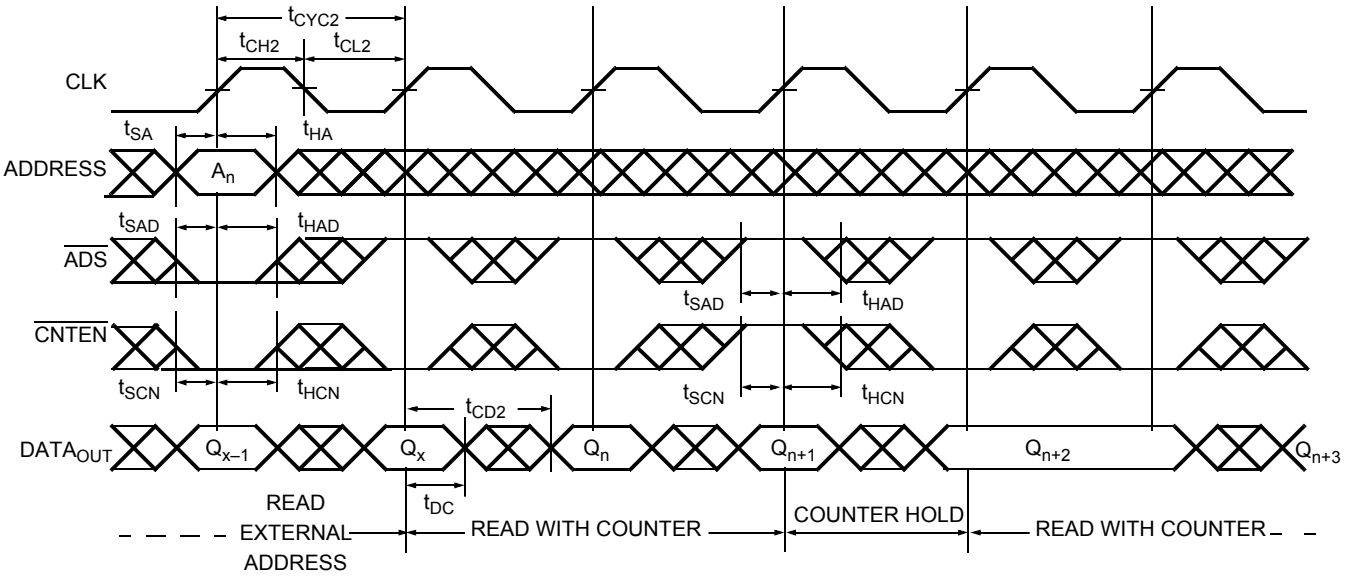
32. In this depth-expansion example, B1 represents Bank #1 and B2 is Bank #2; each bank consists of one Cypress FLEx72 device from this data sheet. $ADDRESS_{(B1)} = ADDRESS_{(B2)}$.
33. $\overline{ADS}$ = $\overline{CNTEN}$= $\overline{BE0}$ – $\overline{BE7}$ = $\overline{OE}$ = LOW; $\overline{MRST}$ = $\overline{CNTRST}$ = CNT/$\overline{MSK}$ = HIGH.
34. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
35. During "No Operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.
36. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{BE0}$ – $\overline{BE7}$ = LOW; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = HIGH.
37. $\overline{CE_0}$ = $\overline{BE0}$ – $\overline{BE7}$ = R/$\overline{W}$ = LOW; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH. When R/$\overline{W}$ first switches low, since OE = LOW, the Write operation cannot be completed (labelled as no operation). One clock cycle is required to three-state the I/O for the Write operation on the next rising edge of CLK.

Switching Waveforms (continued)

Read-to-Write-to-Read ($\overline{OE}$ Controlled)[31, 34, 36, 37]

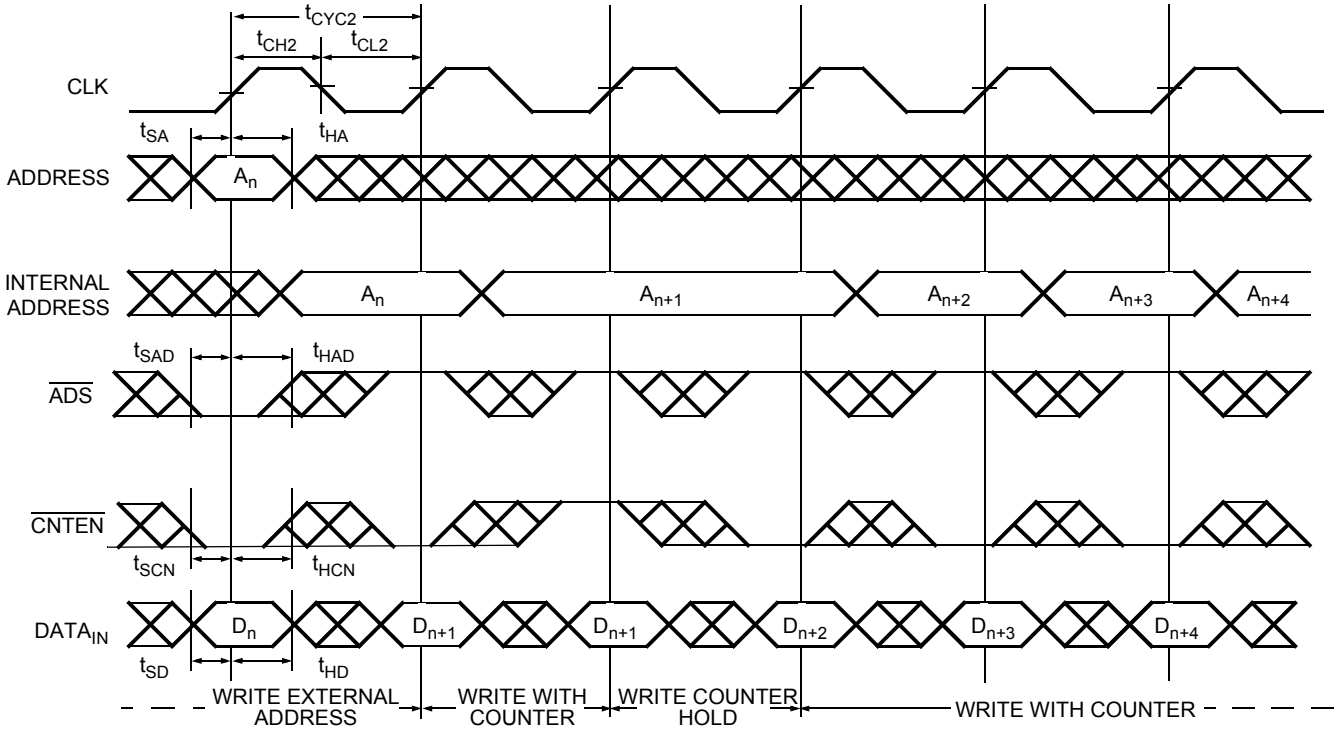


Read with Address Counter Advance[36]



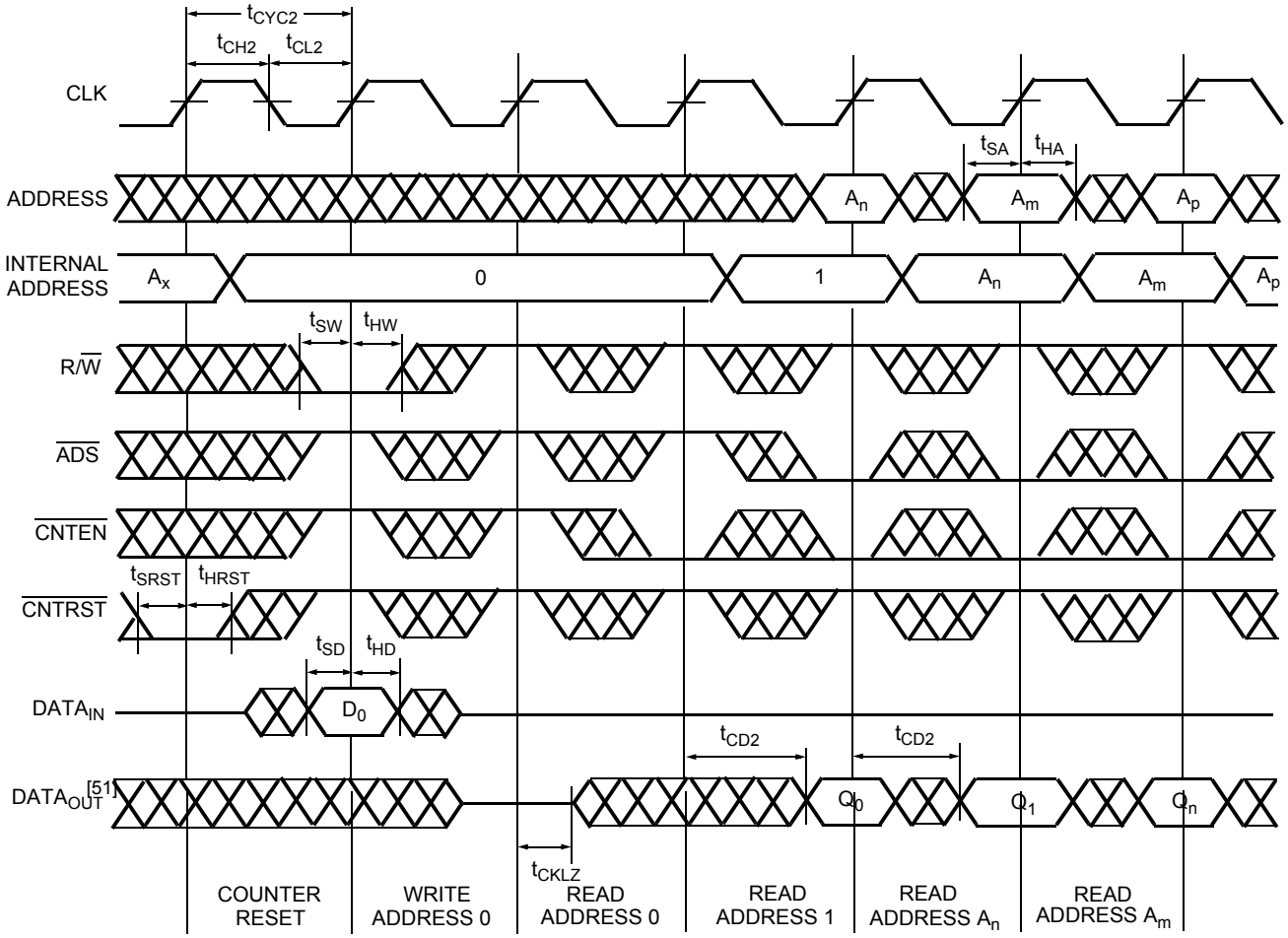
Switching Waveforms (continued)

Write with Address Counter Advance [37]



Switching Waveforms (continued)

Counter Reset [38, 39]

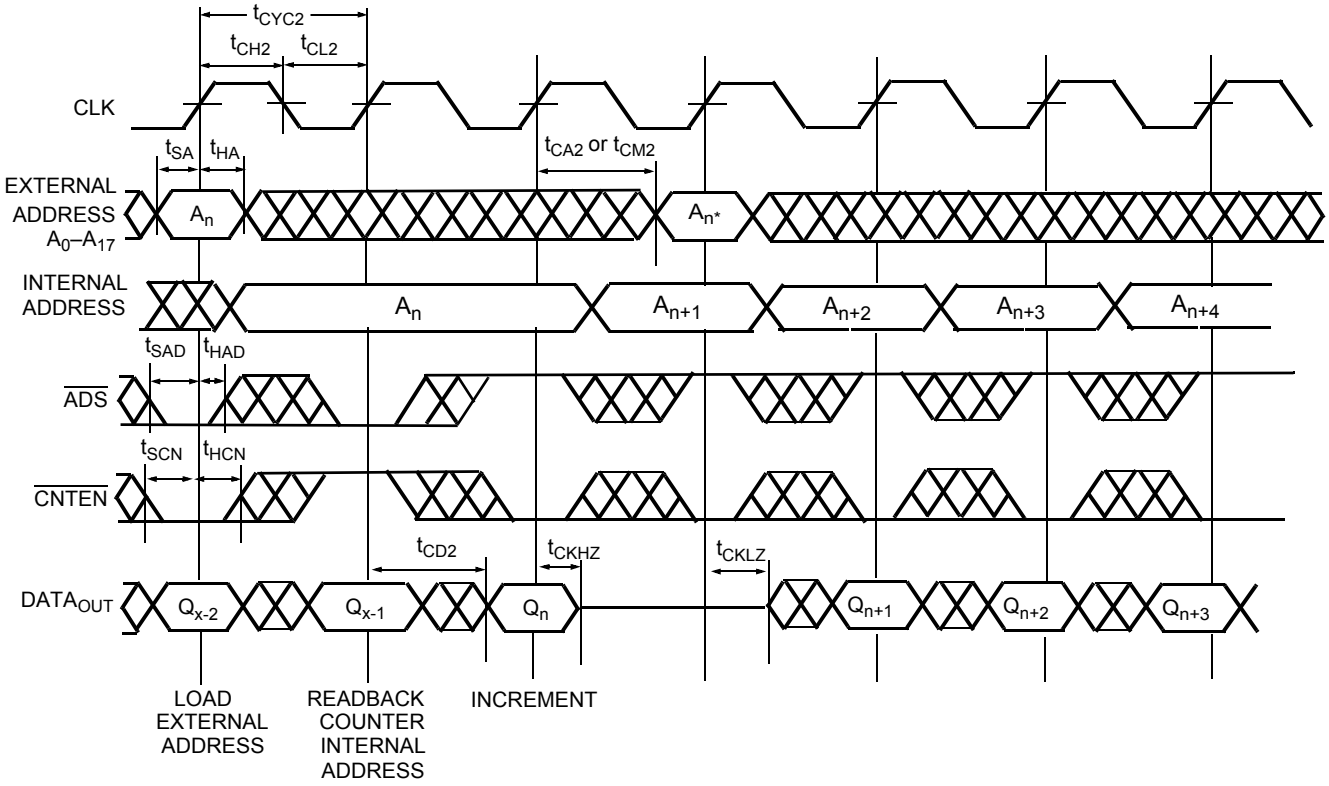


Notes:

38. $\overline{CE_0}$ = $\overline{BE0}$ – $\overline{BE7}$= LOW; CE_1 = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH.
39. No dead cycle exists during counter reset. A Read or Write cycle may be coincidental with the counter reset.

Switching Waveforms (continued)

Readback State of Address Counter or Mask Register[40, 41, 42, 43]

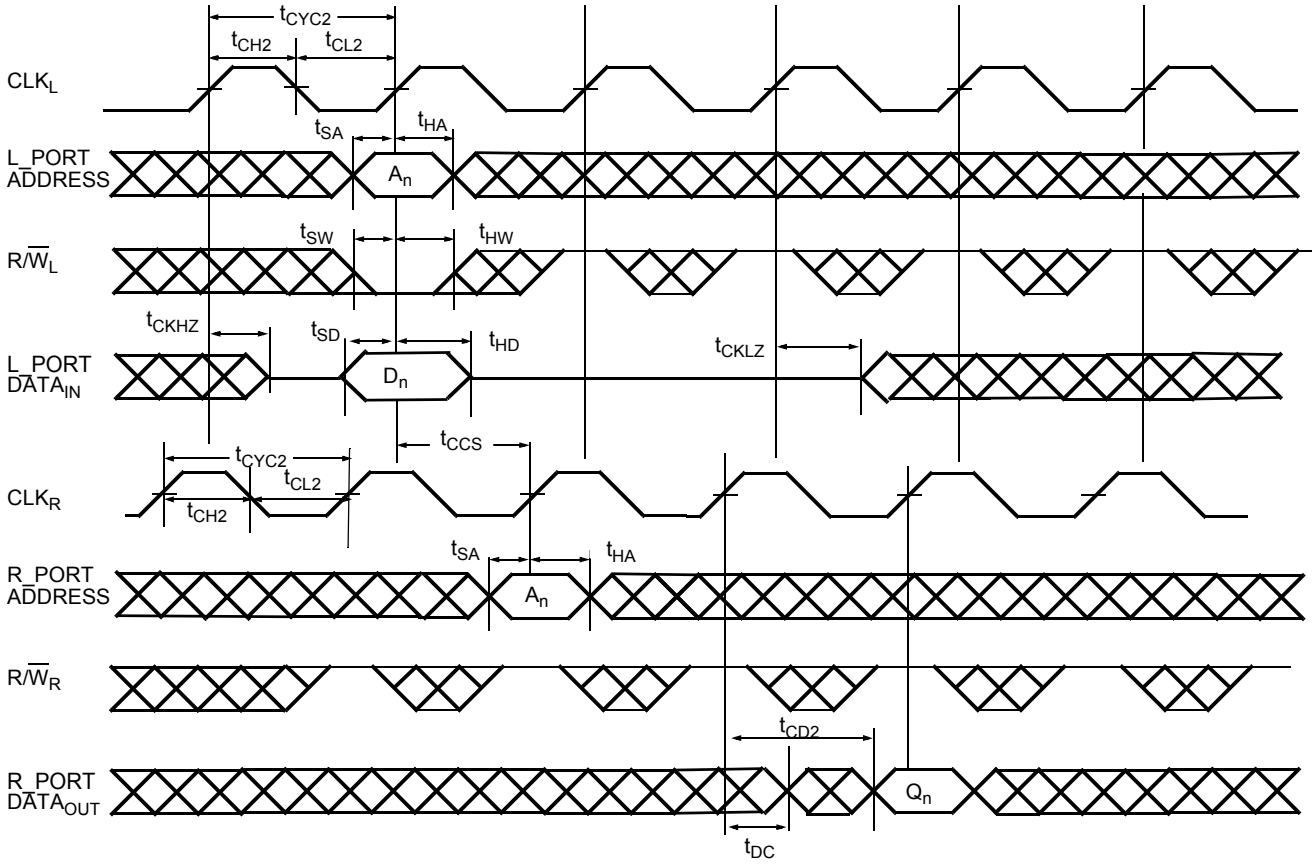


Notes:

40. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{BE0}$ – $\overline{BE7}$ = LOW; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = HIGH.
41. Address in output mode. Host must not be driving address bus after t_{CKLZ} in next clock cycle.
42. Address in input mode. Host can drive address bus after t_{CKHZ}.
43. An * is the internal value of the address counter (or the mask register depending on the CNT/$\overline{MSK}$ level) being Read out on the address lines.

Switching Waveforms (continued)

Left_Port (L_Port) Write to Right_Port (R_Port) Read[44, 45, 46]

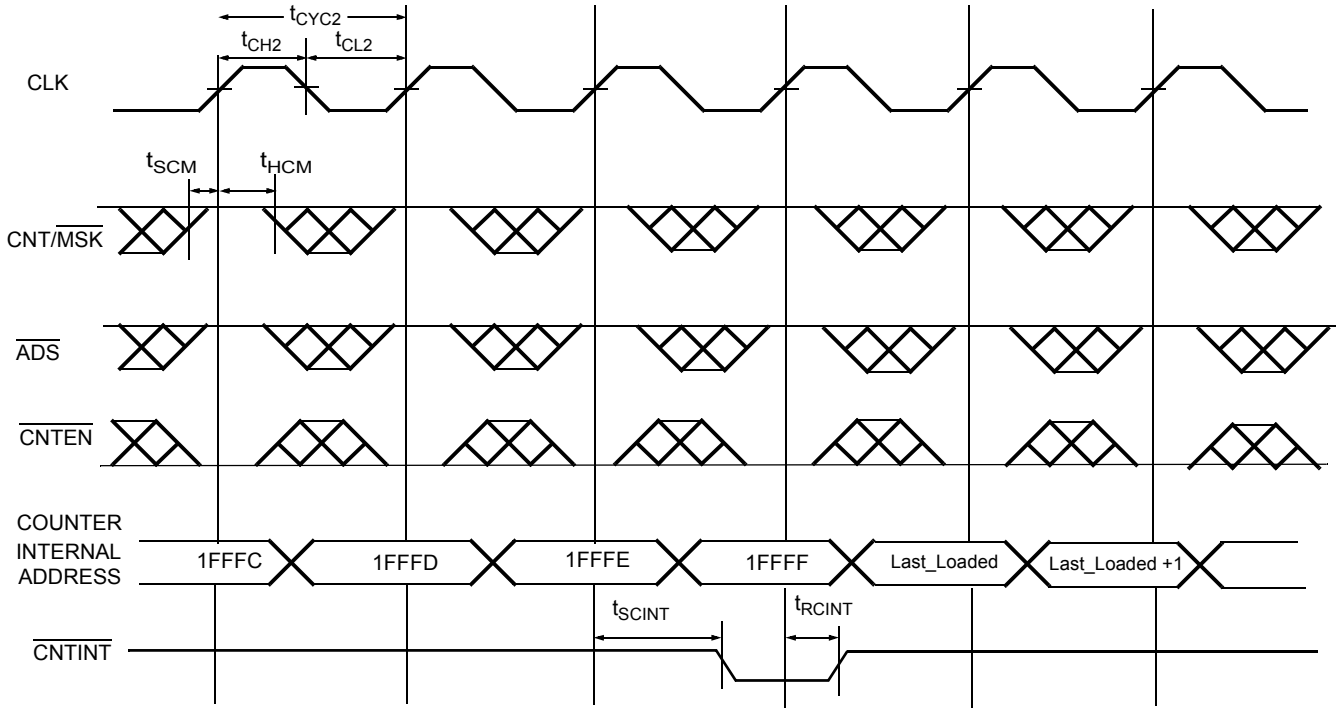


Notes:

44. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{ADS}$ = $\overline{CNTEN}$ = $\overline{BE0}$ – $\overline{BE7}$ = LOW; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH.
45. This timing is valid when one port is writing, and other port is reading the same location at the same time. If t_{CCS} is violated, indeterminate data will be Read out.
46. If t_{CCS} < minimum specified value, then R_Port will Read the most recent data (written by L_Port) only (2 * t_{CYC2} + t_{CD2}) after the rising edge of R_Port's clock. If $t_{CCS} \geq$ minimum specified value, then R_Port will Read the most recent data (written by L_Port) (t_{CYC2} + t_{CD2}) after the rising edge of R_Port's clock.

Switching Waveforms (continued)

Counter Interrupt and Retransmit[47, 48, 49, 50, 51]



Notes:
47. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{BE0}$ – $\overline{BE7}$ = LOW; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = HIGH.
48. $\overline{CNTINT}$ is always driven.
49. $\overline{CNTINT}$ goes LOW when the unmasked portion of the address counter is incremented to the maximum value.
50. The mask register assumed to have the value of 1FFFFh.
51. Retransmit happens if the counter remains in increment mode after it wraps to initially loaded value.

Mailbox Interrupt Timing[52,53,54,55,56]

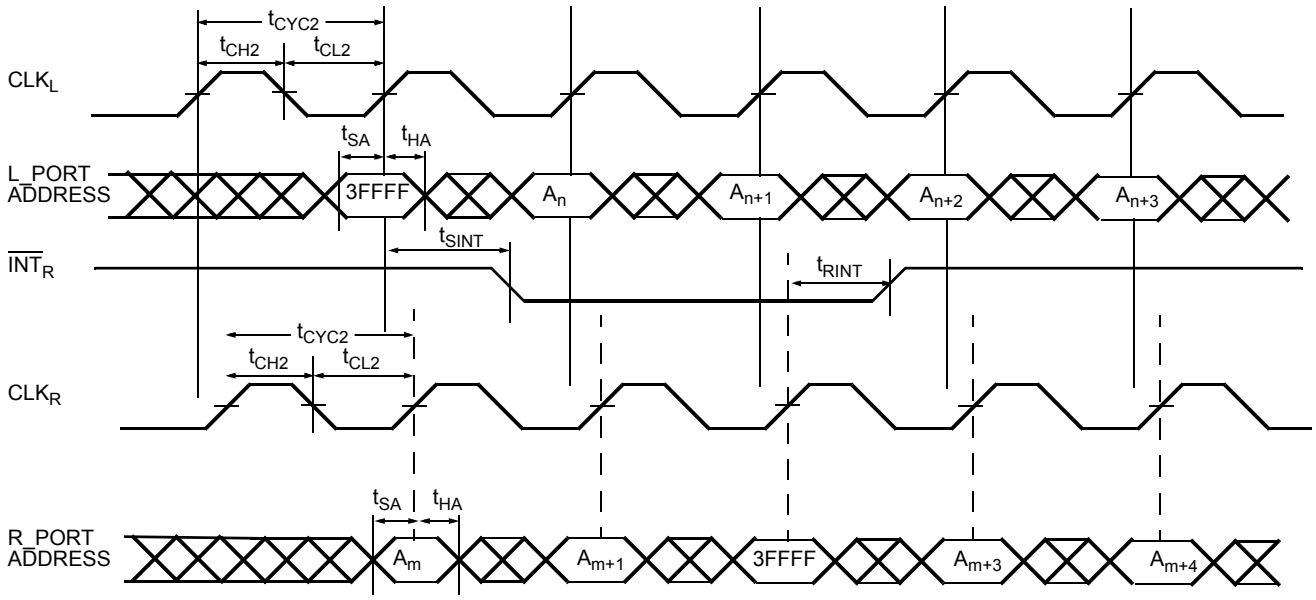


Table 7. Read / Write and Enable Operation (Any Port) [1,14,57,58,59]

Inputs					Outputs	
$\overline{OE}$	CLK	$\overline{CE_0}$	CE_1	R/$\overline{W}$	$DQ_0 - DQ_{71}$	Operation
X	↑	H	X	X	High-Z	Deselected
X	↑	X	L	X	High-Z	Deselected
X	↑	L	H	L	D_{IN}	Write
L	↑	L	H	H	D_{OUT}	Read
H	X	L	H	X	High-Z	Outputs Disabled

Notes:
52. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{ADS}$ = $\overline{CNTEN}$ = LOW; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH.
53. Address “1FFFF” is the mailbox location for R_Port.
54. L_Port is configured for Write operation, and R_Port is configured for Read operation.
55. At least one byte enable (B0 – B3) is required to be active during interrupt operations.
56. Interrupt flag is set with respect to the rising edge of the Write clock, and is reset with respect to the rising edge of the Read clock.
57. $\overline{OE}$ is an asynchronous input signal.
58. When $\overline{CE}$ changes state, deselection and Read happen after one cycle of latency.
59. $\overline{CE_0}$ = $\overline{OE}$ = LOW; CE_1 = R/$\overline{W}$ = HIGH.

Ordering Information

256K × 72 (18Mb) 3.3V Synchronous CYD18S72V Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
133	CYD18S72V-133BBC	BB484	484-ball Grid Array 23mm x 23mm with 1.0mm pitch (FBGA)	Commercial
100	CYD18S72V-100BBC	BB484	484-ball Grid Array 23mm x 23mm with 1.0mm pitch (FBGA)	Commercial
	CYD18S72V-100BBI	BB484	484-ball Grid Array 23mm x 23mm with 1.0mm pitch (FBGA)	Industrial

128K × 72 (9Mb) 3.3V Synchronous CYD09S72V Dual-Port SRAM

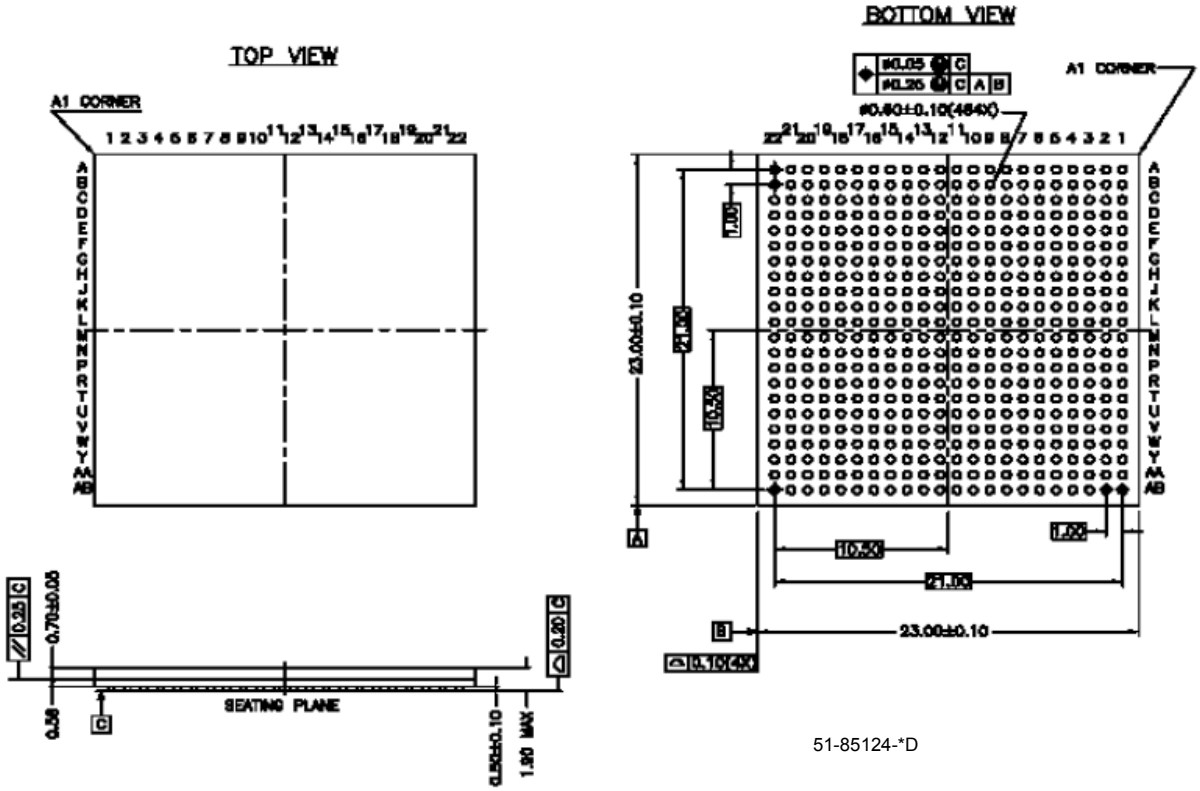
167	CYD09S72V-167BBC	BB484	484-ball Grid Array 23mm x 23mm with 1.0mm pitch (FBGA)	Commercial
133	CYD09S72V-133BBC	BB484	484-ball Grid Array 23mm x 23mm with 1.0mm pitch (FBGA)	Commercial
	CYD09S72V-133BBI	BB484	484-ball Grid Array 23mm x 23mm with 1.0mm pitch (FBGA)	Industrial

64K x 72 (4Mb) 3.3 Synchronous CYD04S72V Dual-Port SRAM

167	CYD04S72V-167BBC	BB484	484-ball Grid Array 23mm x 23mm with 1.0mm pitch (FBGA)	Commercial
133	CYD04S72V-133BBC	BB484	484-ball Grid Array 23mm x 23mm with 1.0mm pitch (FBGA)	Commercial
	CYD04S72V-133BBI	BB484	484-ball Grid Array 23mm x 23mm with 1.0mm pitch (FBGA)	Industrial

Package Diagram

484-ball FBGA (23 mm × 23 mm × 1.9 mm) BB484



Document History Page

Document Title: FLEx72™ 3.3V 64K/128K/256K x 72 Synchronous Dual-Port RAM Document Number: 38-06069				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	125859	06/17/03	SPN	New Data Sheet
*A	128707	08/01/03	SPN	Added -133 speed bin Updated spec values for I_{CC}, t_{HA}, t_{HB}, t_{HW}, t_{HD} Added new parameter I_{CC1} Added bank select read and read to write to read ($\overline{OE}$=low) timing diagrams
*B	128997	09/18/03	SPN	Updated spec values for t_{OE}, t_{OHZ}, t_{CH2}, t_{CL2}, t_{HA}, t_{HB}, t_{HW}, t_{HD}, I_{CC}, I_{SB5}, t_{SA}, t_{SB},t_{SW},t_{SD}, t_{CD2} Updated read to write ($\overline{OE}$=low) timing diagram Updated Master Reset values for t_{RS}, t_{RSR}, t_{RSF} Updated pinout Updated V_{CORE} voltage range
*C	129936	09/30/03	SPN	Updated Package Diagram Updated t_{CD2} value on first page Removed Preliminary Status
*D	233830	See ECN	WWZ	Added 4M and 9M x72 devices into the datasheet with updated pinout, pin description table, power table, and timing table. Changed the title and Added back Preliminary status to reflect the addition of 4M and 9M devices. Removed FLEX72-E word from the document. Added counter related functions for 4M and 9M. Removed standard JTAG description. Updated block diagram. Updated pinout with $\overline{FTSEL}$ and one more PORTSTD pins per port. Updated tRSF of CYD18S72V value.