CYM1465A

512K x 8 PDIP Static RAM

Features

- **4.5V–5.5V operation**
- **CMOS SRAM for optimum speed and power**
- **Low active power (165 mW max.)**
- **Low standby power (L Version)—(110 μW max)**
- **2V data retention (L Version)**
- **JEDEC-compatible pinout**
- **32-pin, 0.6-inch-wide DIP package**
- **TTL-compatible inputs and outputs**

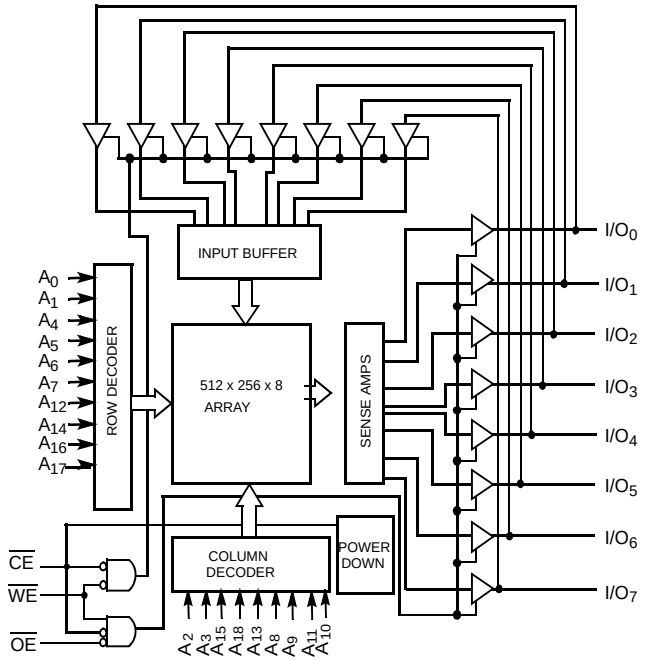
Functional Description

The CYM1465A is a high-performance CMOS static RAM organized as 512K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 99% when deselected.

Writing to the SRAM is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is then written into the memory location specified on the address pins (A_0 through A_{18}). Reading from the device is accomplished by taking chip select (CE) and output enable ($\overline{OE}$) LOW while write enable (WE) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{18}) will appear on the eight appropriate data input/output pins (I/O_0 through I/O_7).The eight input/output pins (I/O0 through I/O7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

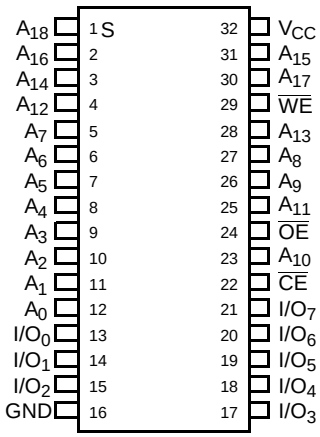
The CYM1465A is available in a 32-pin 600-mil wide body PDIP package.

Logic Block Diagram



Pin Configuration

DIP
Top View



Selection Guide

	CYM1465A-70	CYM1465A-85
Maximum Access Time (ns)	70	85
Maximum Operating Current (mA)	20	20
Maximum Standby Current (μA)	20	20

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... –55°C to +150°C

Ambient Temperature with Power Applied..... –10°C to +85°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... –0.5V to +7.0V

DC Input Voltage .....-0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

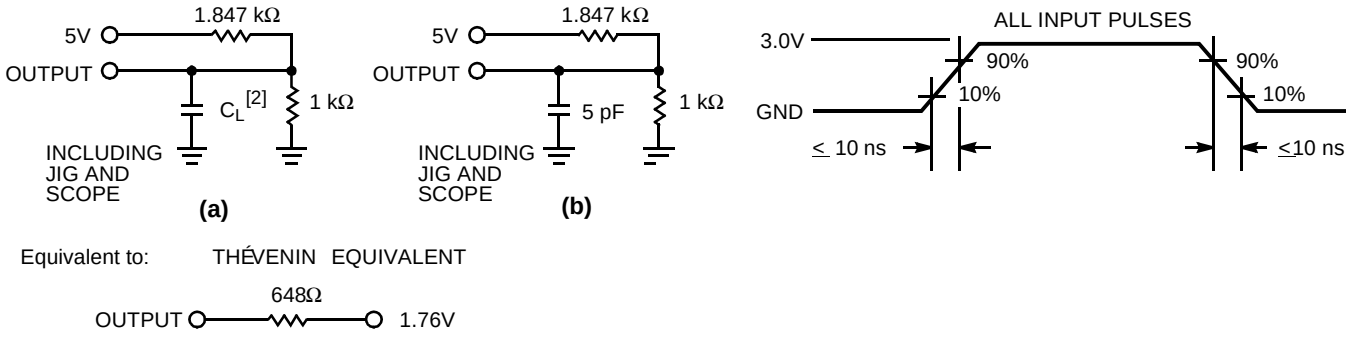
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM1465A		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		20	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, Min. Duty Cycle = 100%		1.5	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ > V_{CC} - 0.3V, V_{IN} > V_{CC} - 0.3V or V_{IN} < 0.3V		20	µA

Capacitance[1]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms



Notes:

1. Tested on a sample basis.
2. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance for 85-, 100-, 120-, and 150-ns speeds. C_L = 30 pF for 70-ns speed.

Switching Characteristics Over the Operating Range[2]

Parameter	Description	CYM1465A-70		CYM1465A-85		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	70		85		ns
t_{AA}	Address to Data Valid		70		85	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		70		85	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35		45	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[3]		25		30	ns
t_{LZCS}	$\overline{CE}$ LOW to Low Z	10		10		ns
t_{HZCS}	$\overline{CE}$ HIGH to High Z[3]		25		30	ns
t_{PU}	$\overline{CE}$ LOW to Power Down	0		0		
t_{PD}	$\overline{CE}$ HIGH to Power Down		70		85	
WRITE CYCLE[4]						
t_{WC}	Write Cycle Time	70		85		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	60		75		ns
t_{AW}	Address Set-Up to Write End	60		75		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	55		65		ns
t_{SD}	Data Set-Up to Write End	30		35		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[3]		25		30	ns

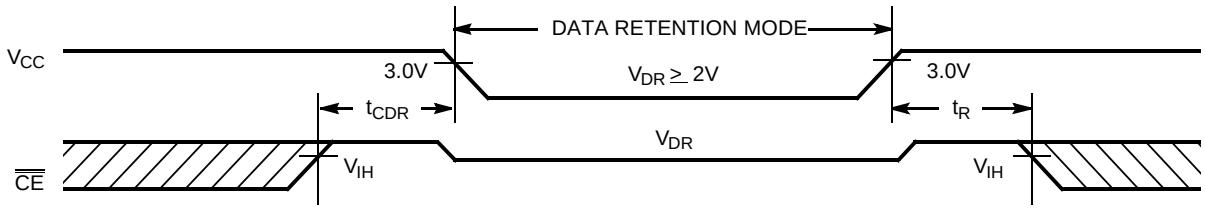
Data Retention Characteristics Over the Operating Range (L Version Only)

Parameter	Description	Test Conditions	Commercial		Industrial		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Retention Data		2		2		V
I_{CCDR3}	Data Retention Current	No Input may exceed Vcc+0.3V V_{DR} = 3.0V, $\overline{CE}$ > V_{CC} – 0.3V, V_{IN} > V_{CC} – 0.3V or V_{IN} < 0.3V		20		20	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

Notes:

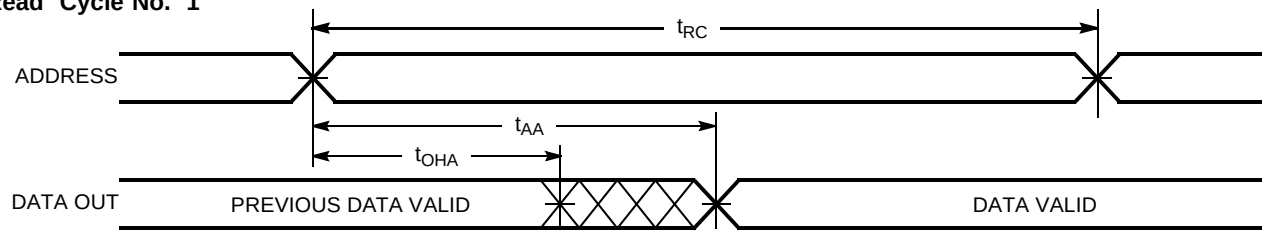
3. C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. Guaranteed, not tested.

Data Retention Waveform

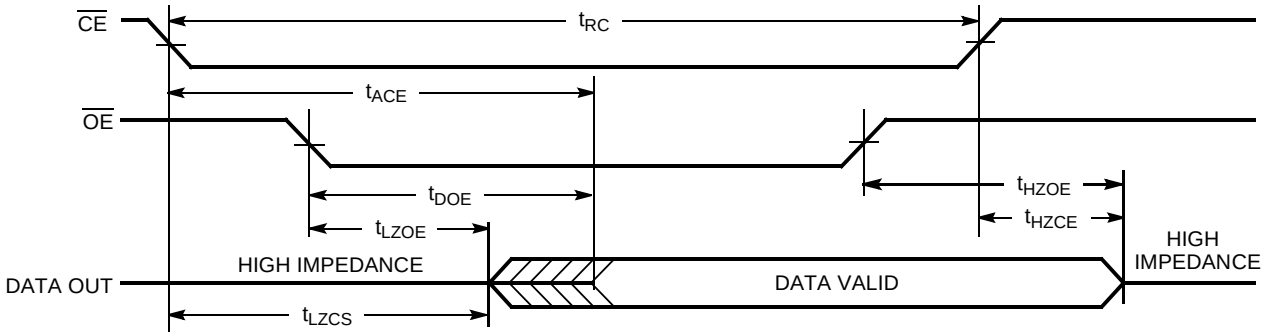


Switching Waveforms

Read Cycle No. 1 [6,7]



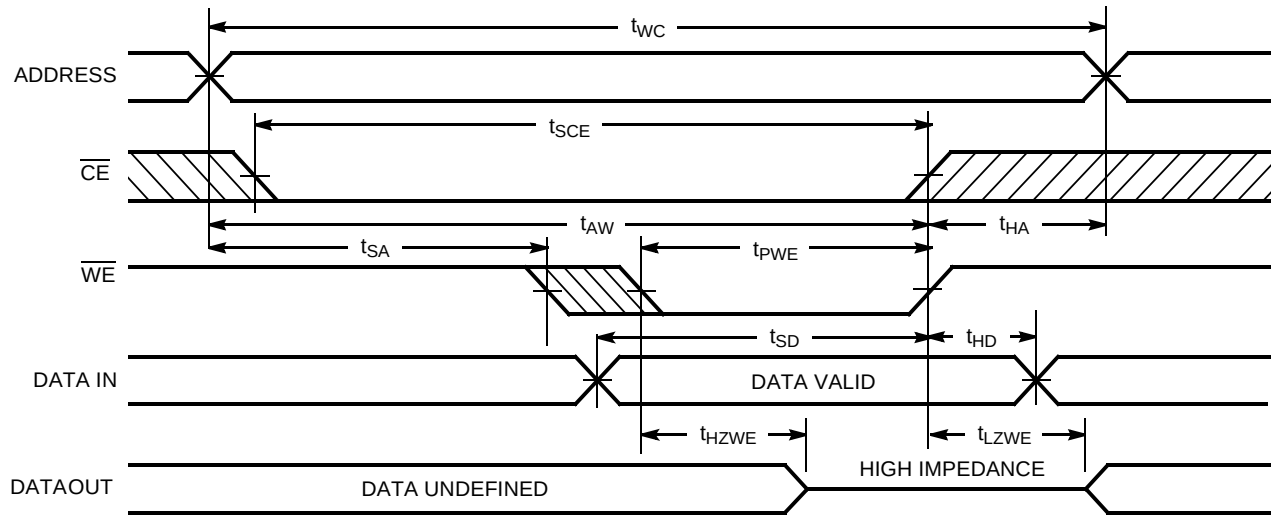
Read Cycle No. 2 [6,8]



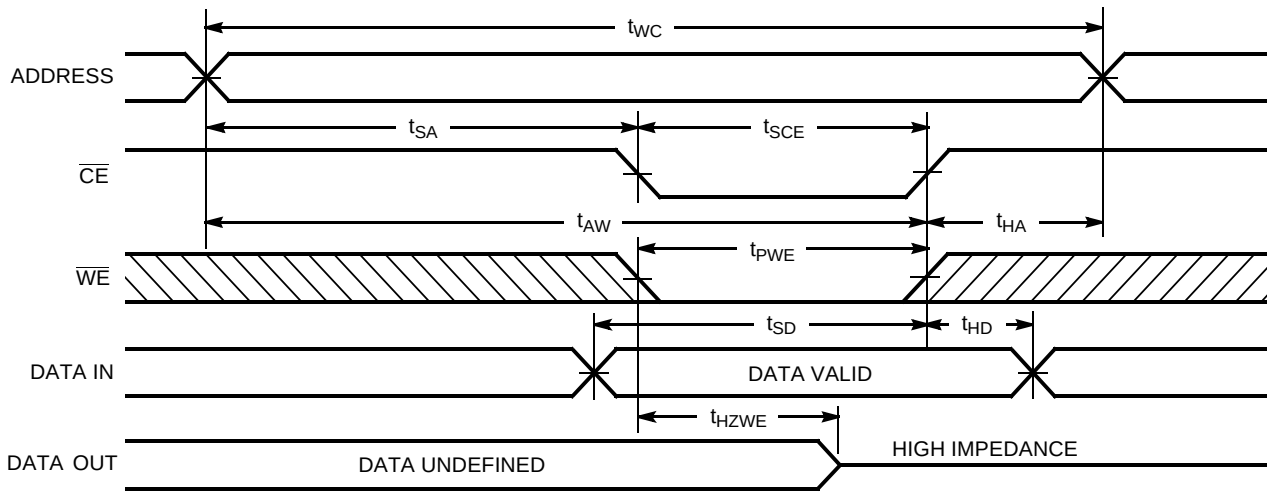
Notes:
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CE}$= V_{IL}.
8. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled) [4]



Write Cycle No. 2 ($\overline{CE}$ Controlled) [4,9]



Note:
9. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

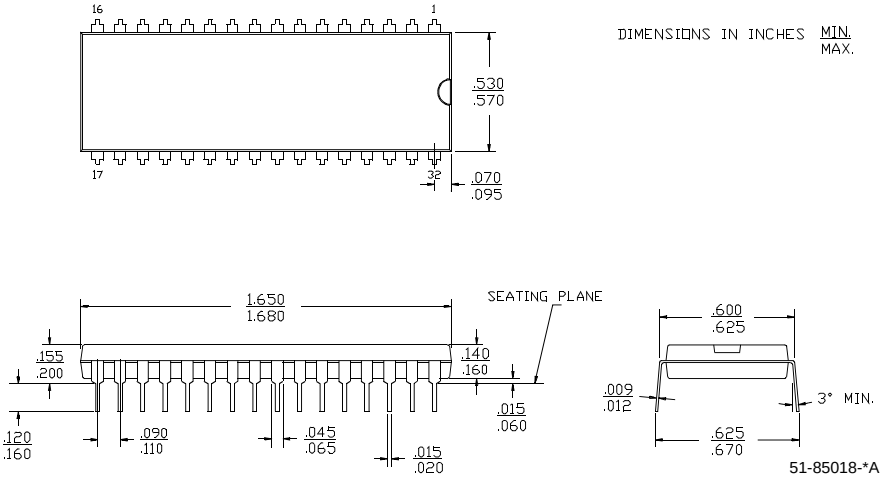
Inputs			Output	Mode
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$		
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CYM1465ALPD-70C	P19	32-Pin DIP Module	Commercial
70	CYM1465ALPD-70I	P19	32-Pin DIP Module	Industrial
85	CYM1465ALPD-85C	P19	32-Pin DIP Module	Commercial
85	CYM1465ALPD-85I	P19	32-Pin DIP Module	Industrial

Package Diagram

32-Lead (600-Mil) Molded DIP P19



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Revision History

Document Title: CYM1465A 512K x 8 PDIP Static RAM Document Number: 38-05269				
REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	114171	3/19/02	DSG	Change from Spec number: 38-M-00036 to 38-05269