



128K x 32 Static RAM Module

Features

- High-density 4-megabit SRAM module
- 32-bit standard footprint supports densities from 16K x 32 through 1M x 32
- High-speed CMOS SRAMs
 - Access time of 15 ns
- Low active power
 - 2.6W (max.) at 20 ns
- SMD technology
- TTL-compatible inputs and outputs
- Low profile
 - Max. height of 0.57 in.
- Small PCB footprint
 - 0.78 sq. in.
- Available in SIMM, ZIP format. SIMM suitable for vertical or angled sockets.

Functional Description

The CYM1836 is a high-performance 4-megabit static RAM module organized as 128K words by 32 bits. This module is

constructed from four 128K x 8 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects (\overline{CS}_1 , \overline{CS}_2 , \overline{CS}_3 , \overline{CS}_4) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

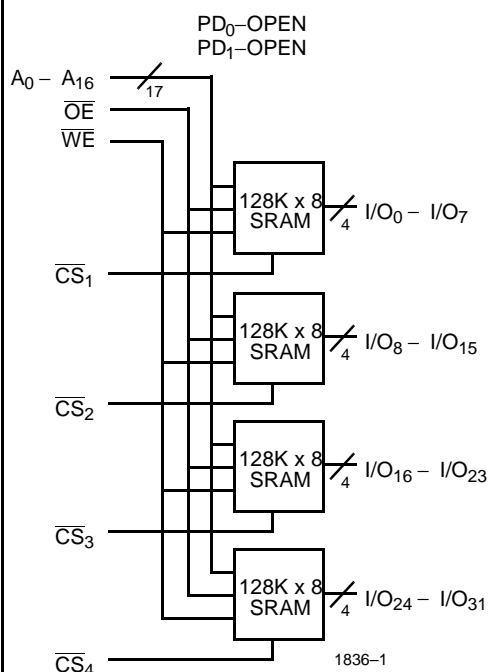
Writing to each byte is accomplished when the appropriate Chip Select (\overline{CS}) and Write Enable (\overline{WE}) inputs are both LOW. Data on the input/output pins (I/O) is written into the memory location specified on the address pins (A_0 through A_{16}).

Reading the device is accomplished by taking the Chip Select (\overline{CS}) LOW while Write Enable (\overline{WE}) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O).

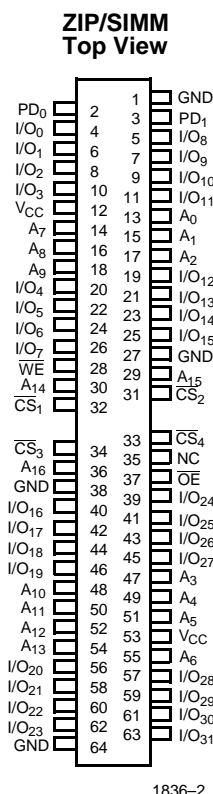
The data input/output pins stay at the high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.

Logic Block Diagram



Pin Configuration



Selection Guide

	1836–15	1836–20	1836–25	1836–30	1836–35	1836–45
Maximum Access Time (ns)	15	20	25	30	35	45
Maximum Operating Current (mA)	760	480	480	480	480	480
Maximum Standby Current (mA)	180	100	100	100	100	100

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –55°C to +125°C

Ambient Temperature with
Power Applied –10°C to +85°C

Supply Voltage to Ground Potential –0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State –0.5V to +7.0V

DC Input Voltage –0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1836–15		1836–20, 25, 30, 35, 45		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = –4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		–0.5	0.8	–0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	–20	+20	–20	+20	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	–20	+20	–20	+20	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, $\overline{CS} \leq V_{IL}$		760		480	mA
I _{SB1}	Automatic \overline{CS} Power-Down Current ^[1]	V _{CC} = Max., $\overline{CS} \geq V_{IH}$, Min. Duty Cycle = 100%		180		100	mA
I _{SB2}	Automatic \overline{CS} Power-Down Current ^[1]	V _{CC} = Max., $\overline{CS} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} – 0.2V or V _{IN} ≤ 0.2V		60		28	mA

Shaded area contains preliminary information.

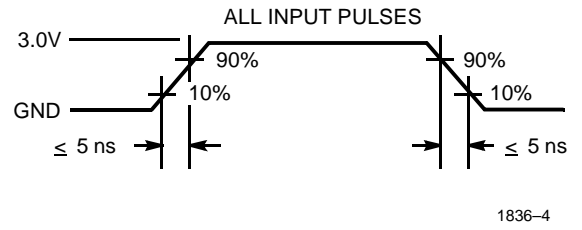
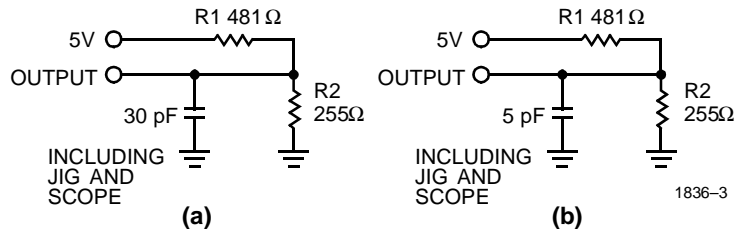
Capacitance^[2]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance ^[3]	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	40/20	pF
C _{OUT}	Output Capacitance		15	pF

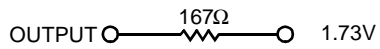
Notes:

1. A pull-up resistor to V_{CC} on the \overline{CS} input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.
3. 20 pF on CS, 40 pF all others.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range^[4]

Parameter	Description	1836–15		1836–20		1836–25		1836–30		1836–35		1836– 45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t _{RC}	Read Cycle Time	15		20		25		30		35		45		ns
t _{AA}	Address to Data Valid		15		20		25		30		35		45	ns
t _{OHA}	Output Hold from Address Change	3		3		3		3		3		3		ns
t _{ACS}	$\overline{\text{CS}}$ LOW to Data Valid		15		20		25		30		35		45	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		7		8		8		10		12		15	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	0		0		0		0		0		0		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z		7		8		10		11		12		15	ns
t _{LZCS}	$\overline{\text{CS}}$ LOW to Low Z ^[5]	3		3		3		3		3		3		ns
t _{HZCS}	$\overline{\text{CS}}$ HIGH to High Z ^[5, 6]		7		10		10		13		15		18	ns
WRITE CYCLE ^[7]														
t _{WC}	Write Cycle Time	15		20		25		30		35		45		ns
t _{SCS}	$\overline{\text{CS}}$ LOW to Write End	12		15		15		18		20		25		ns
t _{AW}	Address Set-Up to Write End	12		15		15		18		20		25		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	12		15		15		18		20		25		ns
t _{SD}	Data Set-Up to Write End	7		10		10		13		15		20		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		0		ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z	3		3		3		3		3		3		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[6]	0	6	0	8	0	10	0	15	0	15	0	18	ns

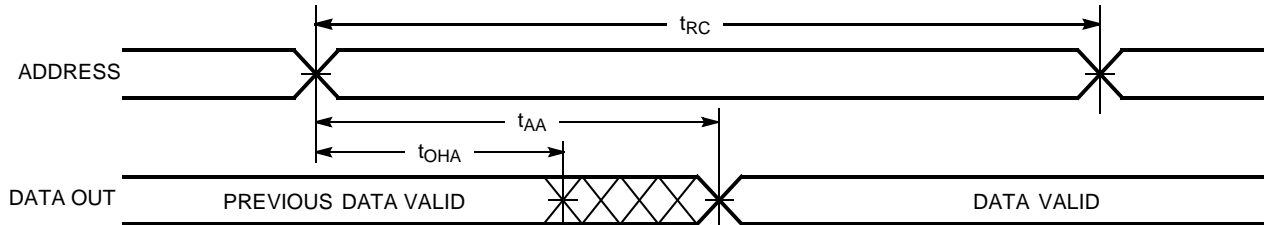
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Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed by design and not 100% tested.
- t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CS} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

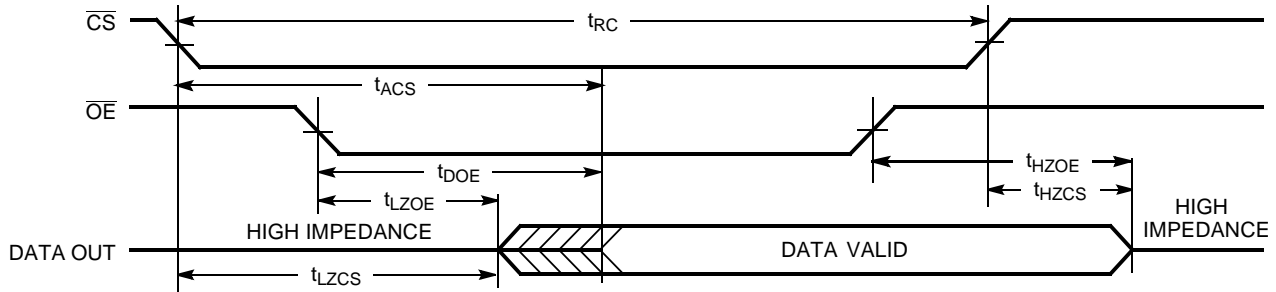
Switching Waveforms

Read Cycle No.1^[8, 9]



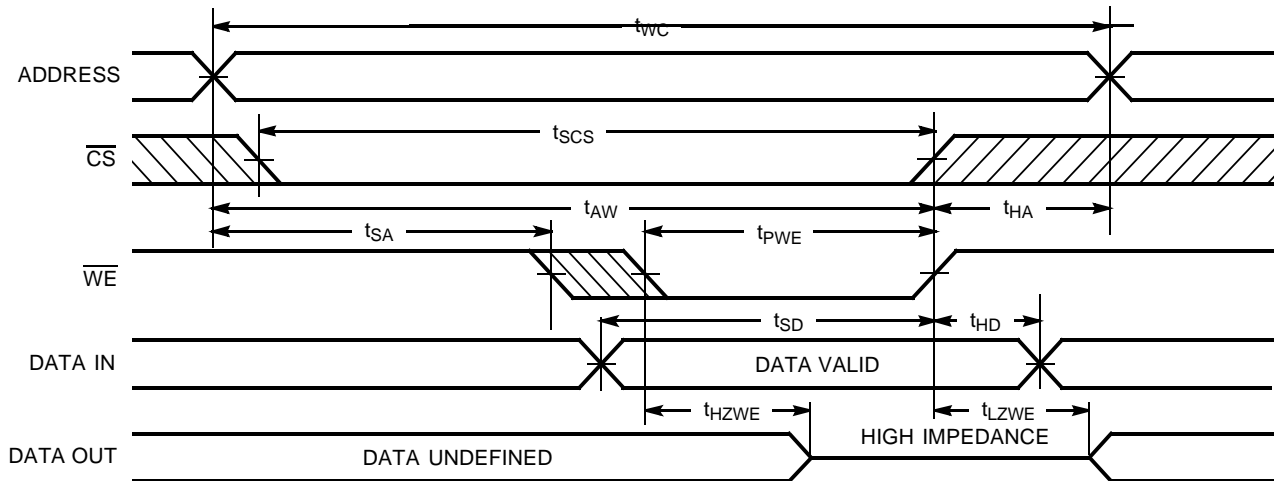
1836-5

Read Cycle No. 2^[8, 10]



1836-6

Write Cycle No.1 (\overline{WE} Controlled)^[7]



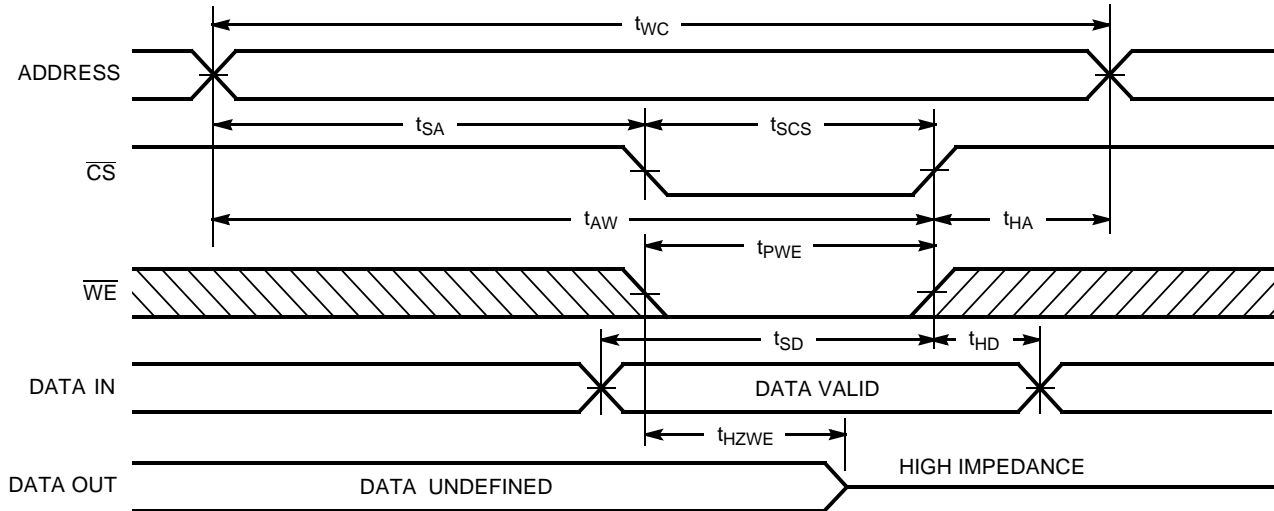
1836-7

Notes:

8. \overline{WE} is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
10. Address valid prior to or coincident with \overline{CS} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{\text{CS}}$ Controlled)^[7, 11]



1836-8

Note:

11. If $\overline{\text{CS}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.

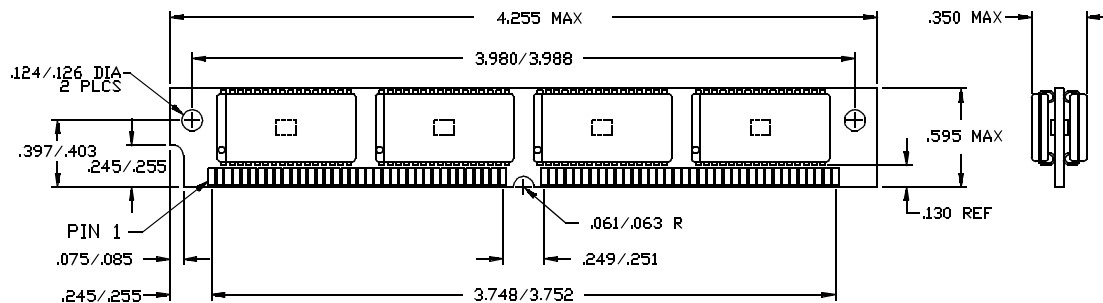
Truth Table

$\overline{\text{CS}}_{\text{N}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect



Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CYM1836PM-15C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-15C	PZ08	64-Pin ZIP Module	
	CYM1836PY-15C	PM08	64-Pin Gold SIMM Module	
	CYM1836P8-15C	PM04	72-Pin Gold SIMM Module	
20	CYM1836PM-20C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-20C	PZ08	64-Pin ZIP Module	
	CYM1836PY-20C	PM08	64-Pin Gold SIMM Module	
	CYM1836P8-20C	PM04	72-Pin Gold SIMM Module	
25	CYM1836PM-25C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-25C	PZ08	64-Pin ZIP Module	
	CYM1836PY-25C	PM08	64-Pin Gold SIMM Module	
	CYM1836P8-25C	PM04	72-Pin Gold SIMM Module	
30	CYM1836PM-30C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-30C	PZ08	64-Pin ZIP Module	
	CYM1836PY-30C	PM03	64-Pin Gold SIMM Module	
	CYM1836P8-30C	PM04	72-Pin Gold SIMM Module	
35	CYM1836PM-35C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-35C	PZ08	64-Pin ZIP Module	
	CYM1836PY-35C	PM03	64-Pin Gold SIMM Module	
	CYM1836P8-35C	PM04	72-Pin Gold SIMM Module	
45	CYM1836PM-45C	PM03	64-Pin SIMM Module	Commercial
	CYM1836PZ-45C	PZ08	64-Pin ZIP Module	
	CYM1836PY-45C	PM03	64-Pin Gold SIMM Module	
	CYM1836P8-45C	PM04	72-Pin Gold SIMM Module	

Package Diagrams (continued)

72-Pin Plastic SIMM Module PM04

64-Pin ZIP Module PZ08
