

## 512K x 24 Static RAM Module

### Features

- High-density 12-Megabit SRAM module
- Access time: 10 ns
- Single 3.3V power supply
- Low active power(1000 W max.)
- TTL-compatible inputs and outputs
- Available in standard 119-ball BGA
- Interface to Motorola digital signal processor (DSP) and analog devices

### Functional Description

The CYM8301BV33 is a 3.3V high-performance 12-Megabit static RAM organized as a 512K words by 24 bits. This module is constructed from three 512K x 8 SRAM dice mounted on a multi layer laminate substrate combined to form a 24 bit SRAM. CYM8301BV33 is a ideal single-chip solution for Motorola's DSP5630X or a two chip solution to Analog Devices ADSP2106XL.

Each data byte is separately controlled by the individual chip selects ( $\overline{CE0}$ ,  $\overline{CE1}$ ,  $\overline{CE2}$ ).  $\overline{CE0}$  controls I/O0–7.  $\overline{CE1}$  controls I/O7–15.  $\overline{CE2}$  controls I/O16–23.

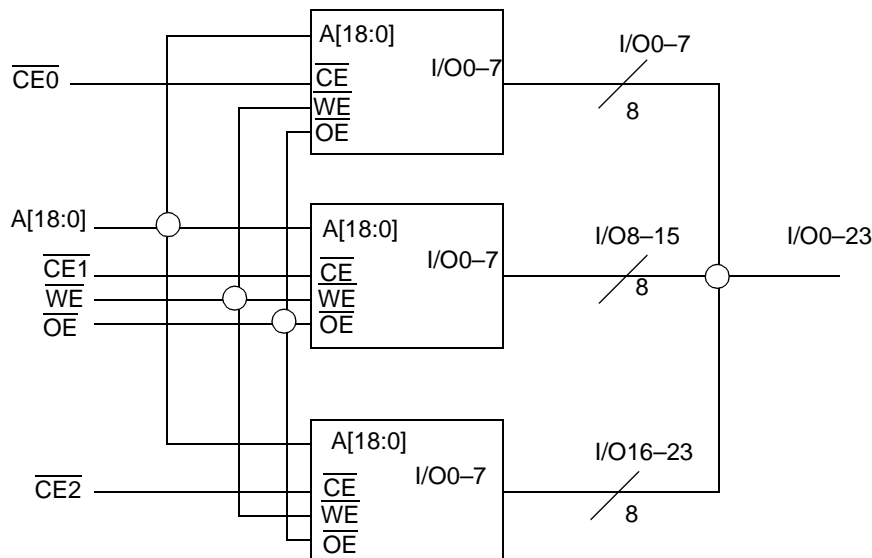
Writing the data bytes into the SRAM is accomplished when the chip select ( $\overline{CSx}$ ) controlling that byte is LOW and Write Enable ( $\overline{WE}$ ) is LOW. Data on the respective input/output pins (I/O) is then written into the memory location specified on the address pins (A0 through A18). Asserting all the ( $\overline{CSx}$ ) LOW and ( $\overline{WE}$ ) LOW will write the entire data (I/O0–23) into the memory. Output Enable ( $\overline{OE}$ ) is a don't care in a write mode.

Reading a byte is accomplished when the chip select ( $\overline{CSx}$ ) controlling that byte is LOW and Write Enable ( $\overline{WE}$ ) is LOW while the Output Enable ( $\overline{OE}$ ) is LOW. Under these conditions the contents of the memory location specified on the address pins will all appear on the specified data input/output pins (I/O). Asserting all the ( $\overline{CSx}$ ) LOW and ( $\overline{WE}$ ) LOW with Output Enable ( $\overline{OE}$ ) LOW will read the entire data (I/O0–23) from the memory.

The data input/output pins (I/O0–23) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$ ) HIGH, the outputs are disabled ( $\overline{OE}$ ) HIGH or during a Write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

For further details on Read and Write conditions, please see the truth table on page 7 of this data sheet.

### Functional Block Diagram



### Selection Guide

		CYM8301BV33-10	CYM8301BV33-12	CYM8301BV33-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Commercial	300	270	255	mA
	Industrial	330	300	285	
Maximum Standby Current	Commercial/Industrial	30	30	30	mA

**Pin Configurations**
**119 BGA**  
**Top View**

	1	2	3	4	5	6	7
<b>A</b>	NC	A	A	A	A	A	NC
<b>B</b>	NC	A	A	$\overline{\text{CE0}}$	A	A	NC
<b>C</b>	I/O12	NC	$\overline{\text{CE1}}$	NC	$\overline{\text{CE2}}$	NC	I/O0
<b>D</b>	I/O13	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O1
<b>E</b>	I/O14	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O2
<b>F</b>	I/O15	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O3
<b>G</b>	I/O16	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O4
<b>H</b>	I/O17	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O5
<b>J</b>	NC	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	NC
<b>K</b>	I/O18	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O6
<b>L</b>	I/O19	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O7
<b>M</b>	I/O20	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O8
<b>N</b>	I/O21	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O9
<b>P</b>	I/O22	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O10
<b>R</b>	I/O23	A	NC	NC	NC	A	I/O11
<b>T</b>	NC	A	A	$\overline{\text{WE}}$	A	A	NC
<b>U</b>	NC	A	A	$\overline{\text{OE}}$	A	A	NC

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[1]</sup> ..... -0.5V to 4.6V

DC Voltage Applied to Outputs

in High-Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
(per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Commercial	0°C to +70°C	3.3V ± 5%
Industrial	-40°C to +85°C	3.3V ± 5%

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions <sup>[2]</sup>	CYM8301BV33-10		CYM8301BV33-12/15		Unit
			Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ , $I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ , $I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	-0.5	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-10	+10	-10	+10	μA
$I_{OZ}$	Output Leakage Current	$GND \leq V_I \leq V_{CC}$ , Output Disabled	-10	+10	-10	+10	μA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}$ , $I_{OUT} = 0 \text{ mA}$ , $f = f_{MAX} = 1/t_{RC}$		300		300	mA
$I_{SB1}$	Automatic CE Power-down Current — TTL Inputs	Max. $V_{CC}$ , $CE \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$		150		150	mA
$I_{SB2}$	Automatic CE Power-down Current — CMOS Inputs	Max. $V_{CC}$ , $CE \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V$ , $f = 0$		30		30	mA

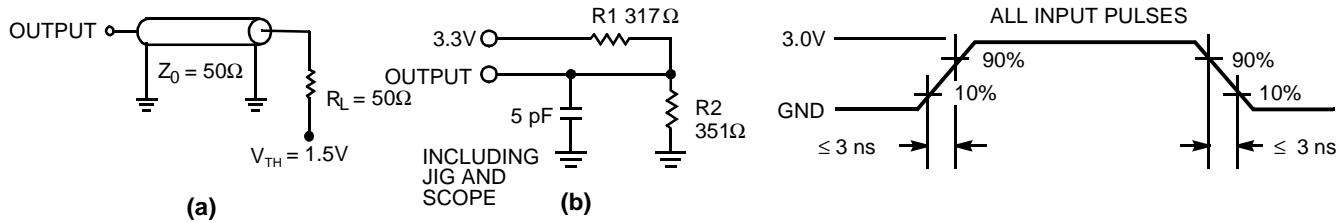
## Capacitance<sup>[3]</sup>

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ , $V_{CC} = 3.3V$	8	pF
$C_{OUT}$	Output Capacitance		8	pF

### Notes:

- $V_{IL}$  (min.) = -2.0V for pulse durations of less than 20 ns.
- CE is a combination of CE1, CE2 and CE3.
- Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



## Switching Characteristics<sup>[4]</sup> Over the Operating Range

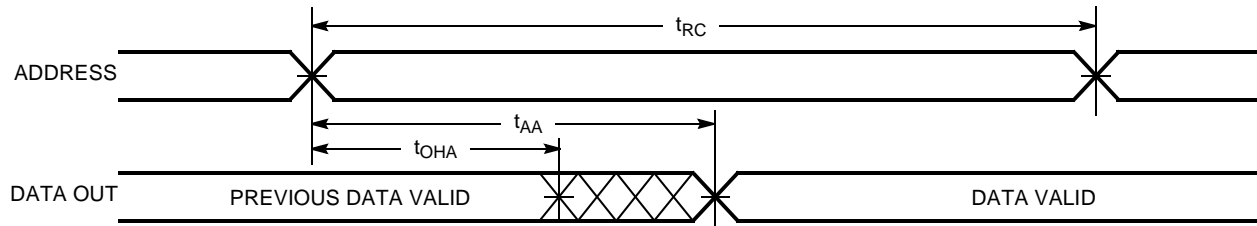
Parameter	Description <sup>[2]</sup>	CYM8301BV-10		CYM8301BV-12		CYM8301BV-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t <sub>RC</sub>	Read Cycle Time	10		12		15		ns
t <sub>AA</sub>	Address to Data Valid		10		12		15	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ active to Data Valid		10		12		15	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		7		7.5		8.5	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low-Z	0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High-Z <sup>[5, 6]</sup>		5		6		7	ns
t <sub>LZCE</sub>	$\overline{CE}$ Active to Low-Z <sup>[6]</sup>	3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ Inactive to High-Z <sup>[5, 6]</sup>		5		6		7	ns
t <sub>PU</sub>	$\overline{CE}$ Active to Power-up	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ Inactive to Power-down		10		12		15	ns
Write Cycle <sup>[7, 8]</sup>								
t <sub>WC</sub>	Write Cycle Time	10		12		15		ns
t <sub>SCE</sub>	$\overline{CE}$ active to Write End	9		9		9		ns
t <sub>AW</sub>	Address Set-up to Write End	9		9		10		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	8		10		11		ns
t <sub>SD</sub>	Data Set-up to Write End	6		6		7		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z <sup>[6]</sup>	3		3		3		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z <sup>[5, 6]</sup>		5		6		7	ns

### Notes:

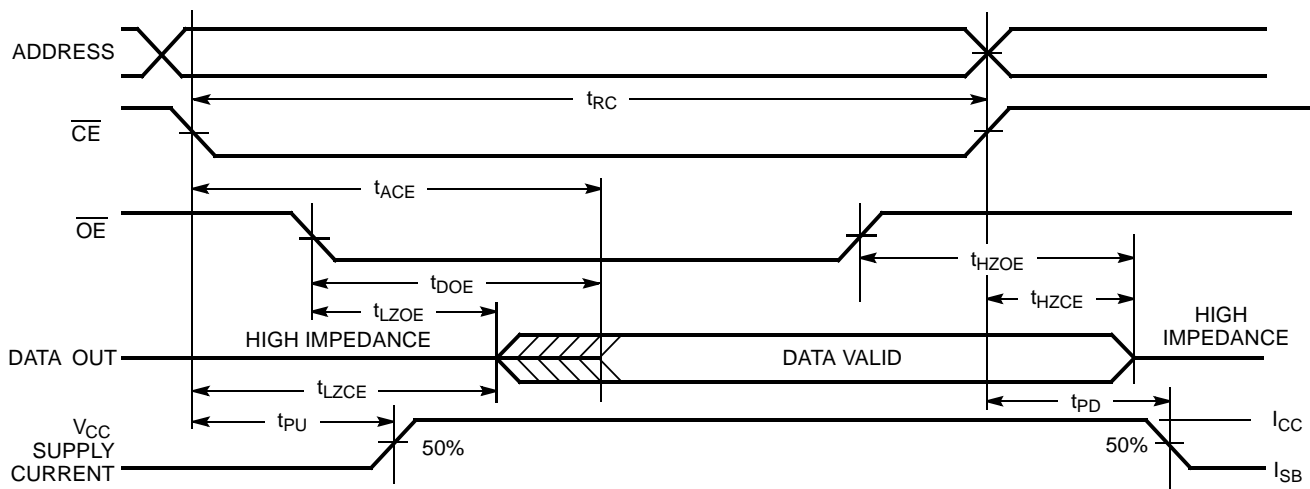
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$ .
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle no. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

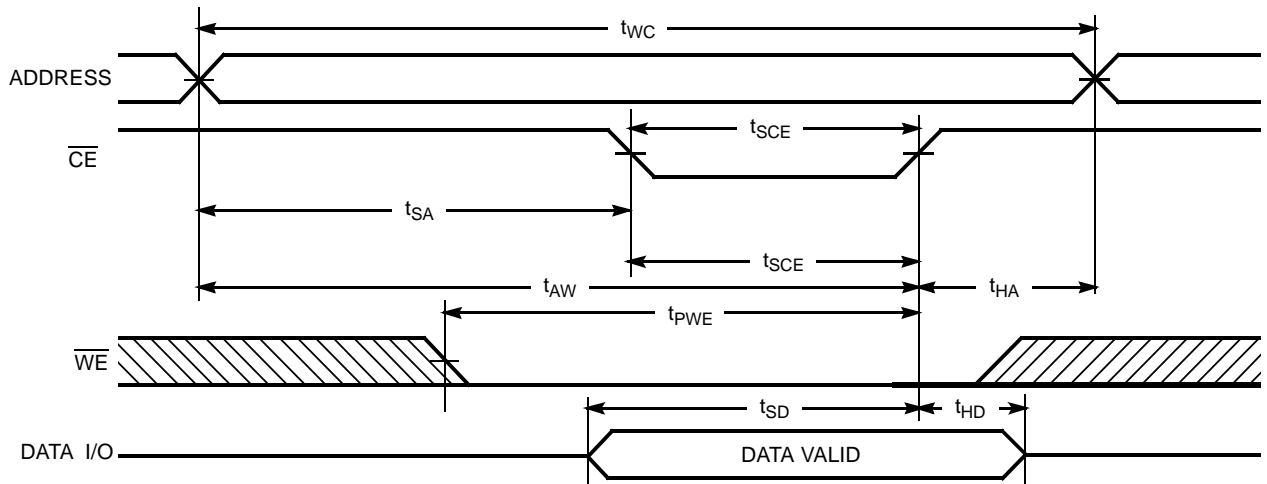
### Read Cycle No. 1<sup>[9, 10]</sup>



### Read Cycle No. 2 ( $\overline{\text{OE}}$ Controlled)<sup>[2, 10, 11]</sup>

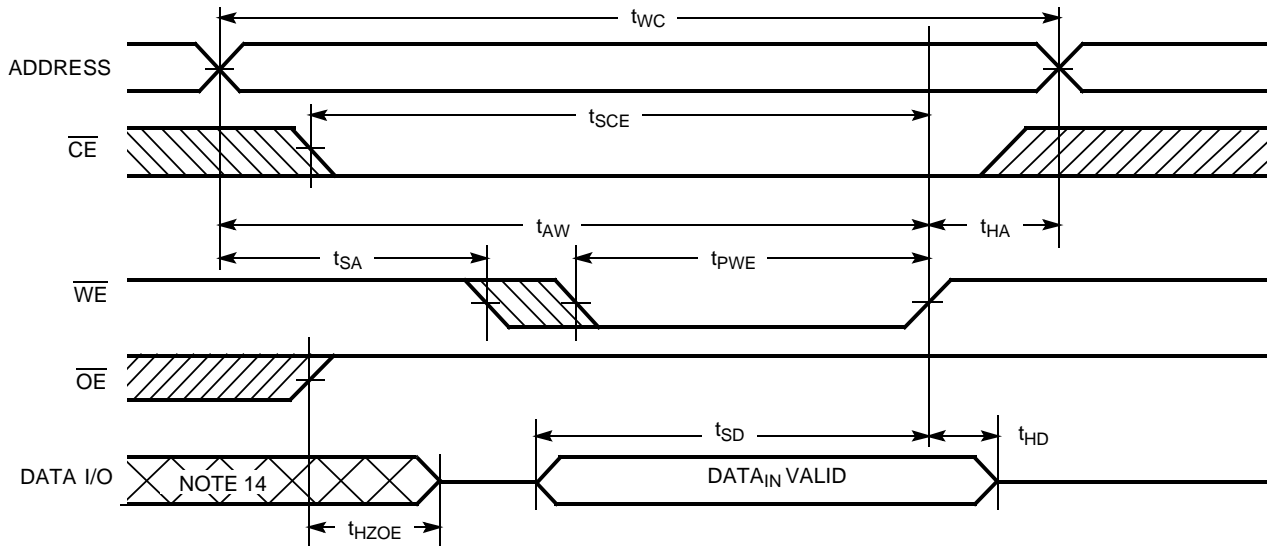
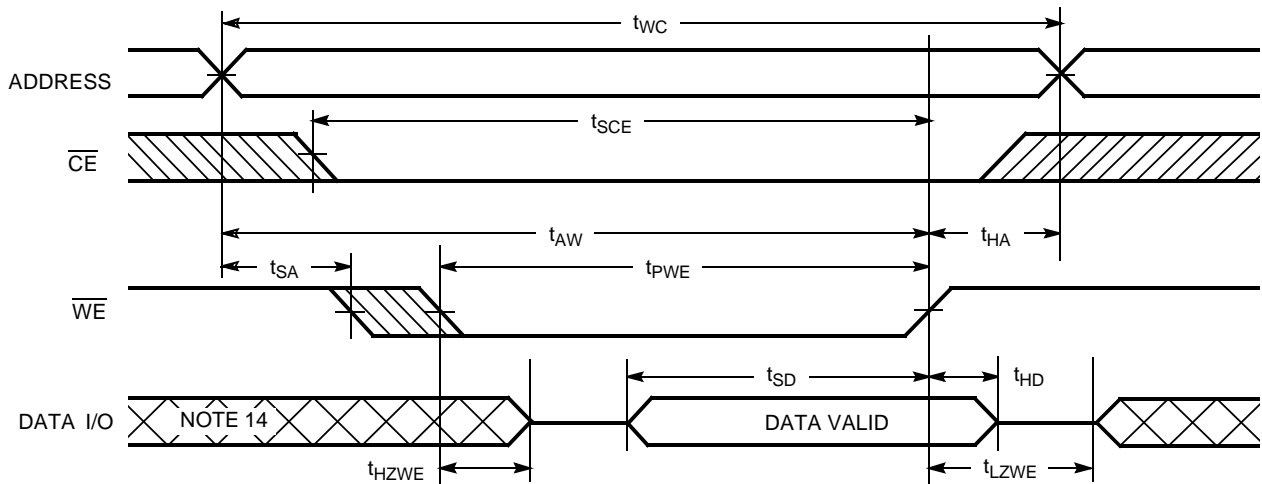


### Write Cycle No. 1 ( $\overline{\text{CE}}$ Controlled)<sup>[2, 12, 13]</sup>



#### Notes:

9. Device is continuously selected.  $\overline{\text{OE}}, \overline{\text{CE}} = V_{\text{IL}}$ .
10.  $\overline{\text{WE}}$  is HIGH for Read cycle.
11. Address valid prior to or coincident with  $\overline{\text{CE}}$  transition LOW.
12. Data I/O is high impedance if  $\text{OE} = V_{\text{IH}}$ .
13. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[12, 13]</sup>**

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[2, 13]</sup>**

**Note:**

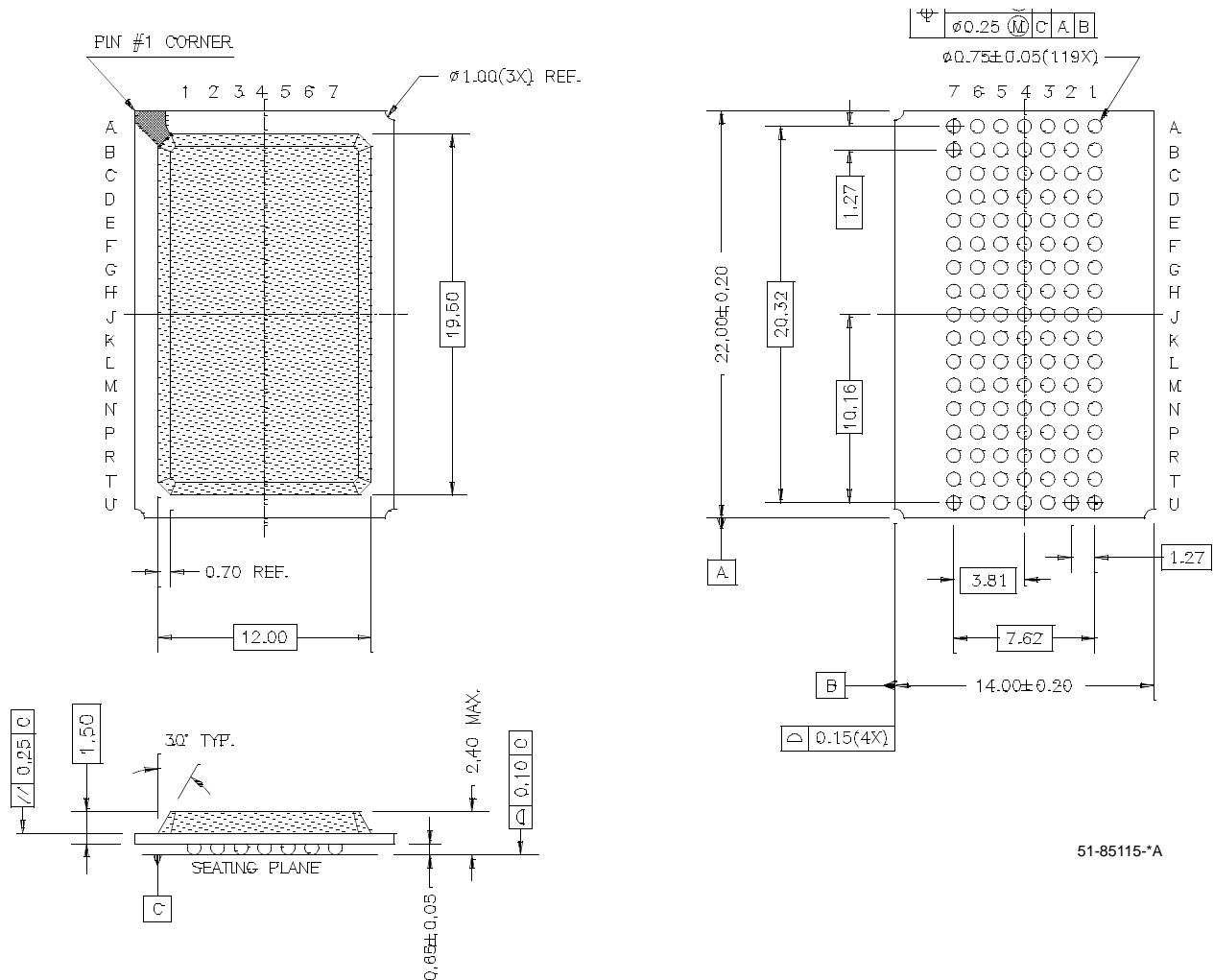
14. During this period the I/Os are in the output state and input signals should not be applied.

**Truth Table**

<b>CE1</b>	<b>CE2</b>	<b>CE3</b>	<b>WE</b>	<b>OE</b>	<b>I/O<sub>0</sub>–I/O<sub>23</sub></b>	<b>Mode</b>
H	H	H	X	X	High-Z	Deselect/Power-down
L	L	L	H	L	Data Out (I/O0–23)	Read
L	L	L	H	H	I/O High-Z	Power-down
L	H	H	H	L	Data Out (I/O0–7) I/O8–23 in High-Z	Read
H	L	H	H	L	Data Out (I/O8–15) I/O0–7 in High-Z I/O16–23 in High-Z	Read
H	H	L	H	L	Data Out (I/O16–23) I/O0–15 in High-Z	Read
L	L	L	L	X	Data In (I/O0–23)	Write
L	H	H	L	X	Data In (I/O0–7)	Write
H	L	H	L	X	Data In (I/O8–15)	Write
H	H	L	L	X	Data In (I/O16–23)	Write

**Ordering Information**

<b>Speed (ns)</b>	<b>Ordering Code</b>	<b>Package Name</b>	<b>Package Type</b>	<b>Operating Range</b>
10	CYM8301BV33 - 10BGC	BG119	119-ball BGA	Commercial
	CYM8301BV33 - 10BGI	BG119	119-ball BGA	Industrial
12	CYM8301BV33 - 12BGC	BG119	119-ball BGA	Commercial
	CYM8301BV33 - 12BGI	BG119	119-ball BGA	Industrial
15	CYM8301BV33 - 15BGC	BG119	119-ball BGA	Commercial
	CYM8301BV33 - 15BGI	BG119	119-ball BGA	Industrial

**Package Diagram**
**119-ball PBGA (14 x 22 x 2.4 mm) BG119**


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**	114945	05/20/02	DFP	New Data Sheet