



Features

- Optional companion part to VIC068A
- Implements master/slave VMEbus interface in conjunction with the VIC068A
- Complete VMEbus and I/O DMA capability for a 32-bit CPU
- Complete local and VMEbus memory map decoding
 - Separate segments on local side available for DRAM, VME subsystem bus (VSB), shared resources, VMEbus, local I/O, and EPROM
 - Separate segments for the VMEbus address decode for slave select 0, slave select 1, and interprocessor communication facilities
 - 64-Kbyte resolution for both local and VMEbus memory maps
- Supports block transfers over 256 byte boundaries
 - Address counters for both VMEbus A(31–8) and local LA(31–8)
 - Supports dual-path mode
 - Supports implementation of VSB interface with DMA capability

- Dual UART channels on board
 - Double-buffered on transmit, quint-buffered on receive
 - Baud rate programmable
- Miscellaneous features
 - Pin grid array or quad flatpack package
 - Supports unaligned transfers
 - Programmable DSACKi for local I/O
 - Programmable timer and interrupt controller
 - Programmable I/O (PIO)
- See the *VIC068A/VAC068A User's Guide* for more information

Functional Description

The VMEbus address controller (VAC068A) is a programmable memory map address controller. In conjunction with the VIC068A (VMEbus interface controller), the VAC068A maximizes the VMEbus interface performance of a master/slave module.

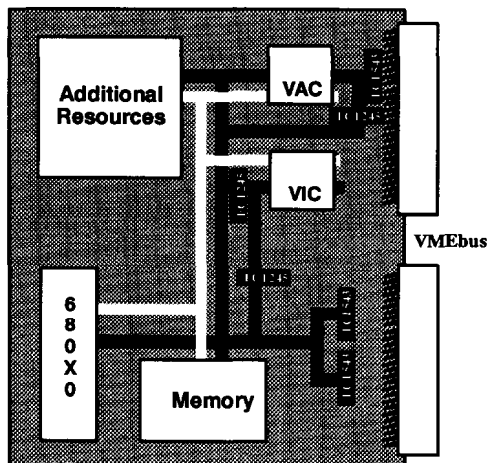
The VAC068A contains programmable registers to allow the user to easily define

memory maps for both the local and VMEbus address regions. The VAC068A also contains the address counters and handshaking signals to allow easy implementation of block-level transfers over 256-byte boundaries. Additional features include dual internal UART channels, redirection control on the local bus to VSB (VME subsystem bus) or shared resource area, data swapping for unaligned transfers, programmable DSACKi, programmable timer and interrupt controller.

The VAC068A connects directly to the local bus and the VIC068A. VMEbus address lines A8 through A31 are driven directly. The VAC068A output drivers feature patented high-drive outputs and TTL-compatible inputs. The VAC068A was designed using high-performance standard cells on an advanced CMOS process.

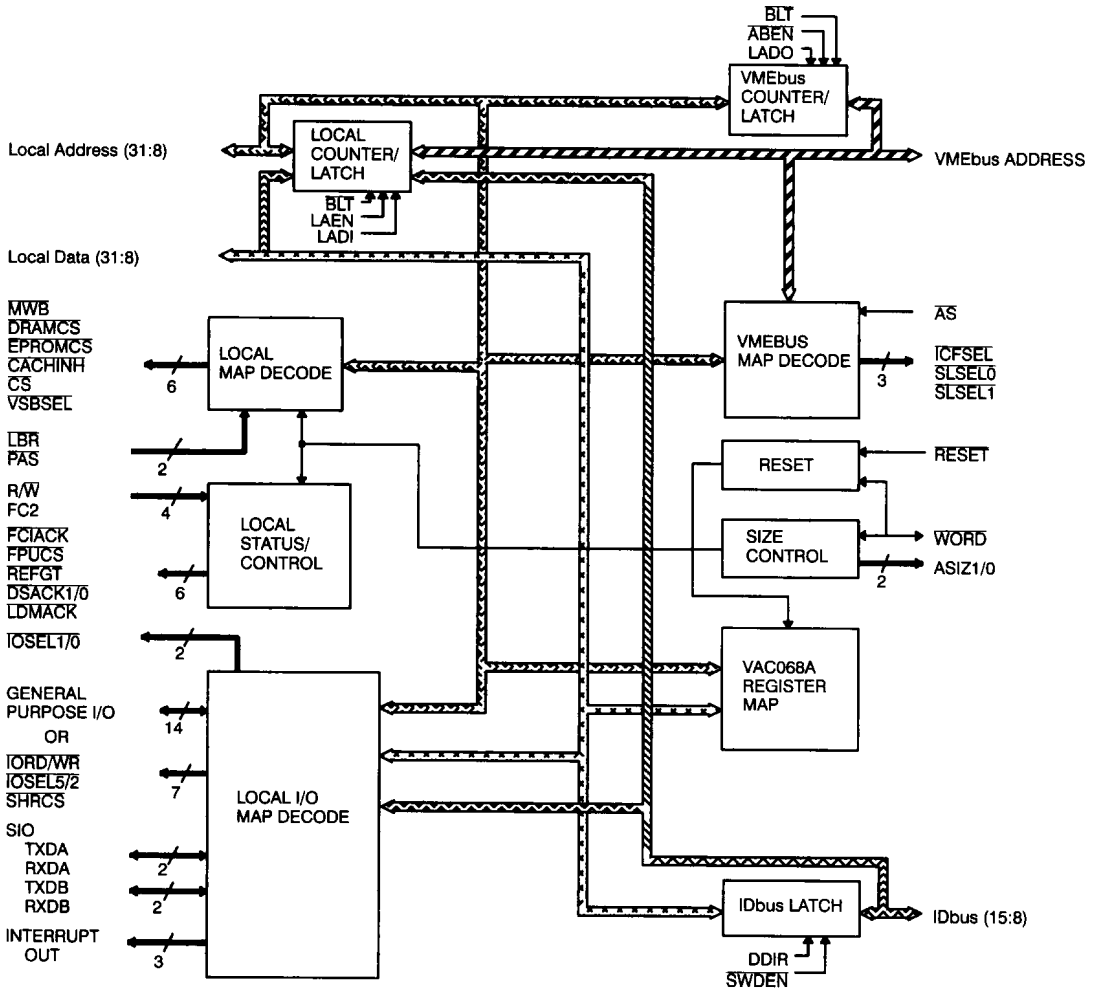
The VAC068A is available in pin grid array (with 122 active signals, 22 power and ground pins, and 1 locator pin) and quad flatpack.

Sample Board Design



VAC068-1

Block Diagram



VAC068-2

Pin Configurations

**Pin Grid Array (PGA)
Bottom View**

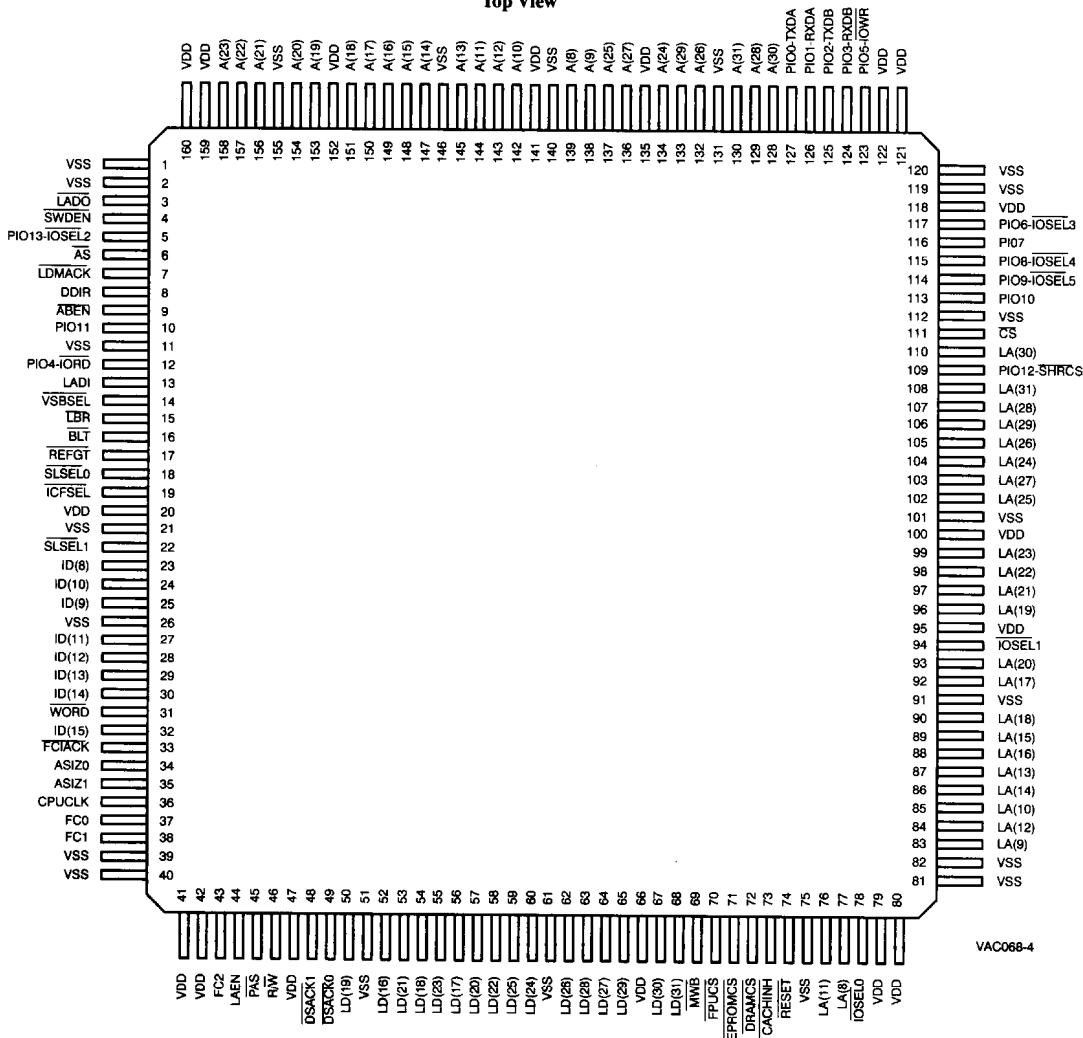
A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
A23	PIO13/ IOSEL2	DDIR	PIO11	LADI	BLT	REFGT*	IOFSEL	SLSELT	ID8	ID11	ID13	ID14	ASIZ0	FC1	1
A20	A22	SWDEN	VAS	ABEN	PIO4/ IORD	VSBSEL	SLSEL0	ID10	ID9	ID12	WORD	FCIACK	FC0	PAS	2
A17	A19	A21	LADO	LDMAK	VSS	LBFR	VDD	VSS	VSS	ID15	ASIZ1	CPUCLK	LAEN	DSACKT	3
A16	A18	VSS	LOCATOR PIN									FC2	R/W	LD19	4
A14	A15	VDD										VDD	DSACK0	LD21	5
A12	A13	VSS										VSS	LD16	LD17	6
A10	A11	VDD										LD23	LD18	LD20	7
A08	A09	VSS										LD24	LD22	LD25	8
A25	A24	VDD										VSS	LD27	LD26	9
A27	A26	VSS										VDD	LD29	LD28	10
A29	A28	PIO0/ TXDA										DRAMCS	LD31	LD30	11
A31	PIO1/ RXDA	PIO5/ IOWR										VSS	EPROMCS	MWB	12
A30	PIO3/ RXDB	PIO7	PIO8/ IOSEL4	VSS	LA29	VSS	VDD	VDD	VSS	LA13	LA9	LA11	CACHINH	FPUCS	13
P102/ TXDB	PIO6/ IOSEL3	PIO10	CS	LA31	LA26	LA24	LA22	IOSELT	LA17	LA15	LA14	LA12	LA8	RESET	14
VDD	PIO9/ IOSEL5	LA30	PIO12/ SHRCS	LA28	LA27	LA25	LA23	LA21	LA19	LA20	LA18	LA16	LA10	IOSEL0	15

VAC068-3

Pin Configurations (continued)

Quad Flatpack (QFP)

Top View





The diagram illustrates the internal architecture of the VAC068 system. Key components include:

- Memory:** Two 512/256K X 36 DRAM modules connected via 32-bit buses through Latching Transceivers to an Address Mux.
- Control & Interface:** A 68030 microprocessor, LA0-LA31 address decoder, 4 JEDEC EPROMS, and Parity Check Logic are interconnected.
- Data Buses:** Multiple Data Function Controller (FCT) units (FCT 543, FCT 245) manage data paths for D24-D31, D16-D23, and D8-D15.
- VIC068A:** The central Video Interface Controller, receiving address inputs (LD0-LD7, LA0-LA7, SCON) and providing video outputs (SYSCLK, D00-D07, AM0-AM5, AS, DS0, DS1, DTACK, WRITE, LWORD, BERR, BGIN, BGOUT, BRI, BBSY, IACK, IACKIN, IACKOUT).
- I/O & Decoding:** A Serial I/O block handles Channel A/B signals. A Map Decoder manages DRAM, I/O, VMEbus, and EPROM access. Latch & Counter blocks manage address ranges LD16-LD31 and LD24-LD31. A Slave Select Decode block manages SLSSEL0, SLSSEL1, and ICFSEL signals.
- Addressing:** Various address ranges are defined, including A(8-31), ID(8-15), and LD15-LD8.

Operating Range

Range	Ambient Temperature	V _{DD}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Related Documents

VIC068A/VAC068A User's Guide

VIC64/CY7C964 Design Notes

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
VAC068A–BC	B144	145-Pin Plastic Pin Grid Array	Commercial
VAC068A–GC	G145	145-Pin Ceramic Pin Grid Array	
VAC068A–NC	N160	160-Lead Plastic Quad Flatpack	
VAC068A–UC	U162	160-Lead Ceramic Quad Flatpack	
VAC068A–GI	G145	145-Pin Ceramic Pin Grid Array	Industrial
VAC068A–UI	U162	160-Lead Ceramic Quad Flatpack	
VAC068A–GM	G145	145-Pin Ceramic Pin Grid Array	Military
VAC068A–GMB	G145	145-Pin Ceramic Pin Grid Array	
VAC068A–UM	U162	160-Lead Ceramic Quad Flatpack	
VAC068A–UMB	U162	160-Lead Ceramic Quad Flatpack	

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